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High-performance multivalued logic circuits based on optically tunable antiambipolar transistors†

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Antiambipolar transistors (AATs) have attracted enormous attention in recent years due to their potential application to multivalued logic circuits (MVLs). A wide variety of materials have been actively investigated for the realization of high-performance AATs and MVLs. Organic semiconductors have emerged as promising candidates in this regard because of their simple fabrication and patterning techniques. In this work, an AAT is developed by adopting these advantageous characteristics and employing 2,7-dioctyl[1]benzothieno[3,2-*b*][1]benzothiophene (C8-BTBT) and PhC_2H_4-benzo[*de*]isoquinolino[1,8-*gh*]quinolone diimide (PhC_2-BQQDI) as p-type and n-type semiconductors, respectively. Due to the high charge carrier mobility of these organic semiconductors, the AATs exhibit a high on/off ratio of 10^6 and the AAT-based ternary inverters show a complete output voltage sweep from drain voltage to ground voltage. Then, an efficient technique of device geometry engineering is demonstrated to further improve the voltage transfer characteristics (VTC) of the ternary inverters. However, the ternary inverter property was still not sufficient for the practical applications because of a low static noise margin (SNM). Finally, the contrasting photoresponsivity of the channel layers under ultraviolet light irradiation overcomes the drawback. The optical tunability of the AATs consequently achieves well-balanced VTC with high SNM of 76%. Our devices, thus, reveal their great potential for future opto-electronic logic applications.

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1. Introduction

Antiambipolar transistors (AATs) have received considerable attention in the last few years due to their unique transfer characteristics.[1–9] Depending on the material properties and device geometries, AATs can produce "Λ" shaped[1–3] or "N" shaped[4–6] transfer curves with one[1–6] or a few[7–9] negative differential transconductance (NDT) regions. These noteworthy transport properties enable us to implement multivalued logic circuits (MVLs), which can handle more than two logic states.[4–6,8,10–14] This MVL concept is expected to greatly reduce the chip area without downscaling individual components due to the increase in the information-processing capability and therefore, facilitates the development of low-power and high-speed integrated circuits.[15–19] A wide variety of two-dimensional (2D) materials and organic semiconductors have already been investigated with a view to further improve the device performance of the AATs and MVLs.[20–35] In most of the studies transition metal dichalcogenides (TMDCs) such as molybdenum disulfide (MoS_2), tungsten diselenide (WSe_2) and tin diselenide ($SnSe_2$) were employed owing to their advantages of dangling bond free surface properties, superior electronic performance metrics and high stability under mechanical stress.[20–25,30–37] However, TMDCs have a fatal disadvantage as regards to their film processing method. Most of the TMDC films and the devices are fabricated through mechanical exfoliation technique using adhesive tapes. Systematic control of film dimensions is not possible in this technique. Moreover, this process is also not compatible for large-scale manufacturing due to poor scalability and low yield. Organic semiconductors possess several advantages in this regard. This class of semiconductors provides the advantages of simple and low-cost fabrication processes.[38] The device dimensions such as channel length, channel width and heterojunction area can be systematically controlled by shadow mask patterning.[3,26] In addition, their optical absorption in broad wavelength range offers the scope of opto-electronic logic applications and their intrinsic mechanical flexibility promotes flexible and wearable electronics.[38–40] Therefore, high data processability and mechanical flexibility can be simultaneously attained in organic MVLs, which makes the devices highly compatible with the next generation Internet of Things (IoT) technology.

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In 2018, we paved the way for organic MVLs by demonstrating a ternary logic circuit based on an antiambipolar transistor. Then, a sexithiophene (α-6T) and a perylene derivative (PTCDI-C8) were employed as the p-type and n-type semiconductors, respectively.[26] The devices showed three distinct logic states. However, the inverters did not exhibit complete modulations in their output voltage (V_{OUT}) from the drain voltage (V_{DD}) to the ground voltage. Kim *et al.* solved this problem by proposing a new device geometry for the AATs that used dinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) and PTCDI-C13 transistor channels.[27] In the transistor, the DNTT layer was connected with both source and drain electrodes whereas the PTCDI-C13 layer was connected to only one electrode. The unique device geometry achieved a complete V_{OUT} swing in the MVL. However, the narrow width of the logic 1/2 state was a major issue as regards these devices because this feature induces a small static noise margin (SNM) in the ternary inverter. Therefore, although these studies significantly stimulated progress on organic MVLs, further investigations are still needed to improve the performance of the organic MVLs.

In this work, we attempted to tackle these issues by fabricating an AAT based on a new combination of organic semiconductors with 2,7-dioctyl[1]benzothieno[3,2-*b*][1]benzothiophene (C8-BTBT) as a p-type semiconductor and PhC_2H_4-benzo[*de*]isoquinolino[1,8-*gh*]quinolone diimide (PhC_2-BQQDI) as an n-type semiconductor. The first advantage of these semiconductors is their high charge carrier mobility for transistor channels. This feature enabled us to realize a full-swing ternary inverter, where the inverter was composed of a series circuit of the proposed AAT and an n-type PhC_2-BQQDI transistor. Besides, the geometry optimization of the AATs improved the voltage balance between input and output signals in the inverter voltage transfer characteristics (VTC). Nevertheless, the VTC of the inverter was still insufficient in regard to the SNM. Hence, we demonstrate a strategy, namely the optical control of the AAT, for the further improvement of the VTC of the ternary inverter. The constituent channel materials exhibited a contrasting photoresponsivity under visible and ultraviolet (UV) light irradiation. The C8-BTBT transistor was found to be sensitive to a UV light signal, whereas the PhC_2-BQQDI transistor was active under visible light irradiation. The distinct photoresponsivity, which originated from their contrasting light absorption wavelength ranges, enabled an optical control over the inverter output. Consequently, the inverters were able to realize a high SNM of 76% under UV light irradiation. Thus, the proposed devices meet all the requirements for organic ternary logic circuits.

2. Results and discussion

Fig. 1(a) shows the transfer characteristics of the PhC_2-BQQDI (red line) and C8-BTBT (blue line) transistors. The chemical structures and the atomic force microscope (AFM) images of these organic semiconductors are shown in Fig. S1 in the ESI.† The PhC_2-BQQDI transistor showed typical n-type transfer characteristics with an electron mobility of 0.4 ± 0.1 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 10^4. On the other hand, the C8-BTBT transistor showed p-type transfer characteristics with a hole mobility of 1.5 ± 0.3 $cm^2\ V^{-1}\ s^{-1}$ and a high on/off ratio of 10^8. The threshold voltages (V_{th}) of the PhC_2-BQQDI and

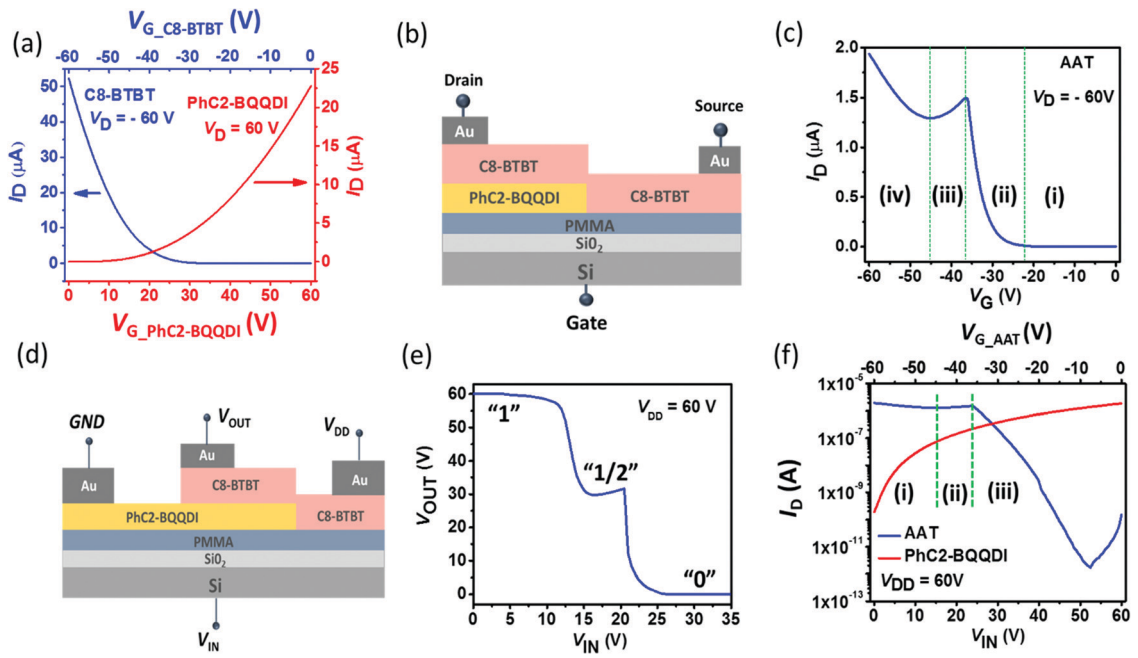

Fig. 1 (a) Transfer characteristics (at V_D = |60| V) of the PhC_2-BQQDI (red line) and C8-BTBT (blue line) transistors. (b) Schematic illustration of the AAT. (c) Transfer curve of the AAT at V_D = −60 V. (d) Schematic illustration of the ternary inverter consisting of the AAT and the PhC_2-BQQDI transistor. (e) Voltage transfer characteristics of the ternary inverter at V_{DD} = 60 V. (f) Transfer characteristics of the AAT and PhC_2-BQQDI transistor measured at V_{DD} = 60 V.

C8-BTBT transistors were 10 V and −35 V, respectively. The n- and p-type characteristics of the respective transistors were also observed from the output characteristics shown in Fig. S2 in the ESI.†

Subsequently, AATs were prepared based on the performances of the two organic transistors. Fig. 1(b) shows a schematic illustration of the AATs. Here, both the source and drain electrodes are placed on the C8-BTBT layer, and a lateral heterojunction of the C8-BTBT and PhC_2-BQQDI layers is formed between the two electrodes. As reported by Kim *et al.*,[27] this transistor structure enhances the hole current in the p-type operation and is advantageous in yielding full-swing ternary inverter operation. Fig. 1(c) shows the transfer curve of the AAT in the p-type operation. The transfer characteristics can be divided into four distinct V_G ranges. In range (i), the source to gate voltage (V_{SG}) was insufficient to form the p-type channel. As a result, the devices remained in the off state. In this range, a minimum drain current (I_{OFF}) of 1 pA was observed at V_G = −7.5 V. In range (ii), I_D started increasing with increasing V_G because of the hole accumulation in the C8-BTBT channel. Namely, both C8-BTBT and PhC_2-BQQDI channels became conductive. Due to the high charge carrier mobilities of these semiconducting layers, I_D increased rapidly and attained a high peak value (I_{peak}) of 1.5 μA at $V_G = V_{peak}$ = −37 V. Then, in range (iii), I_D started decreasing with increasing V_G due to the depletion of the PhC_2-BQQDI channel. I_D fell from 1.5 μA to 1.2 μA at the end of this range (V_G = −45 V), yielding the NDT range. Finally, in range (iv), the device showed a second current enhancement range, where I_D started increasing again in the V_G range above −45 V owing to the presence of the continuous C8-BTBT layer, which provided a conductive path that allowed the holes to reach the drain electrode. At the end of this range (V_G = −60 V), the AATs exhibited the maximum drain current (I_{ON}) of 2 μA. Thus, the proposed AATs achieved a high on/off ratio (I_{ON}/I_{OFF}) of 10^6 owing to the high charge carrier mobility of the constituent organic semiconductors.

The unique transfer characteristics of the AATs, including the NDT range and high on/off ratio, enabled us to obtain a complete V_{DD} to ground voltage sweep in the ternary inverter circuit. The logic circuit was constructed by using a series connection of the AAT and an n-channel PhC_2-BQQDI transistor as illustrated in Fig. 1(d). The supply voltage (V_{DD} = 60 V) and input voltage (V_{IN}) were applied to the drain electrode of the AAT and the common gate electrode, respectively. The source electrode of the PhC_2-BQQDI transistor was grounded and the output voltage (V_{OUT}) was monitored at the middle-shared electrode. Here it is important to note that the V_{OUT} electrode is electrically connected to PhC_2-BQQDI transistor through C8-BTBT layer and the layer doesn't impede the underlying n-type operation of the PhC_2-BQQDI transistor. The optical microscope image of the inverter is shown in Fig. S3 (ESI†). The ternary inverter exhibited three distinct logic states as shown in Fig. 1(e): logic 1 at $V_{OUT} = V_{DD}$ = 60 V, logic 1/2 at $V_{OUT} = V_{DD}/2$ = 30 V and logic 0 at V_{OUT} = ground. The inverter operation can be understood from the transfer characteristics of the constituent AAT and PhC_2-BQQDI transistor as shown in Fig. 1(f). At a low V_{IN} (range (i)), the I_D of the AAT was much higher than that through the PhC_2-BQQDI transistor which formed a conductive path between V_{DD} and the output terminal and thereby yielded $V_{OUT} = V_{DD}$ (logic 1). In the intermediate V_{IN} (range (ii)), where the NDT was induced in the AAT, both transistors showed comparable I_D values. As a consequence, V_{DD} was divided into the two transistors, resulting in a middle logic state (logic 1/2). Importantly, the channel lengths of the AAT (100 μm) and PhC_2-BQQDI transistor (300 μm) were optimized to achieve the ideal V_{OUT} balance between the logic 1 and logic 1/2 states. This is because the V_{OUT} levels of the inverter logic states depend on the resistance balance between the constituent transistors.[41] In the high V_{IN} (range (iii)), the PhC_2-BQQDI transistor exhibited markedly higher I_D values compared with that of the AAT. Therefore, a conducting path between the output terminal and ground was created to result in V_{OUT} = ground logic 0. It should be noted that the complete V_{OUT} sweep from V_{DD} to the ground in the inverter was realized by the following two contributing factors. One is the observed current enhancement in the AAT at a high V_G range (range (iv) in Fig. 1(c)), which originated from the continuous C8-BTBT channel. The enhanced I_D assisted V_{OUT} to attain V_{DD} in the logic 1 operation. The other factor is the large difference in the I_D values of the AAT and PhC_2-BQQDI transistor. The difference of several orders of magnitude in the I_D (ranges (i) and (iii) in Fig. 1(f)) helped V_{OUT} to reach V_{DD} in the logic 1 state and decrease to ground voltage in the logic 0 state, respectively. In most cases, the full V_{DD} to ground sweep in ternary inverters has not been obtained because of the insufficient difference in the I_D values of the constituent transistors.[6,14,21] The use of transistor channels with high carrier mobilities provided an advantage in this regard. High carrier mobility of the semiconductors realized a high on/off ratio in each constituent transistor, resulting in a large difference in I_D at low and high V_{IN} range of the inverter operation. Thus, the synergic effect of device geometry and superior transport properties of the material combination enabled us to achieve a complete V_{DD} to ground modulation in the ternary inverters along with the ideal V_{OUT} ratio of 0.5 between logic 1/2 and logic 1.

However, the obtained VTC was still not suitable for the practical use of the ternary inverter because no SNM for the logic 1/2 state appeared as shown in Fig. S4 (ESI†). The poor SNM of the inverters mainly originated from the narrow width of the logic 1/2 state. Given an ideal ternary inverter, at $V_{IN} = V_{DD}/2$, V_{OUT} should be equal to $V_{DD}/2$.[42,43] In contrast, in our devices, at V_{IN} = 30 V, logic 0 state was obtained instead of logic 1/2 state. Namely, no cross section in the logic 1/2 state was observed in the inverter butterfly curve (Fig. S4, ESI†). Therefore, maximization of the logic 1/2 width was requisite to obtain the enough SNM in the logic 1/2 state.

To overcome the drawback, we adopted a strategy which is geometry optimization of the AATs. Since logic 1/2 width depends on the NDT range of the AATs, we optimized the ratio (R_L) between the length of PhC_2-BQQDI channel ($L_{Phc_2\text{-}BQQDI}$) and the length of C8-BTBT channel ($L_{C8\text{-}BTBT}$) (*i.e.* $R_L = L_{Phc_2\text{-}BQQDI}$: $L_{C8\text{-}BTBT}$) to enhance the NDT range in the AATs.

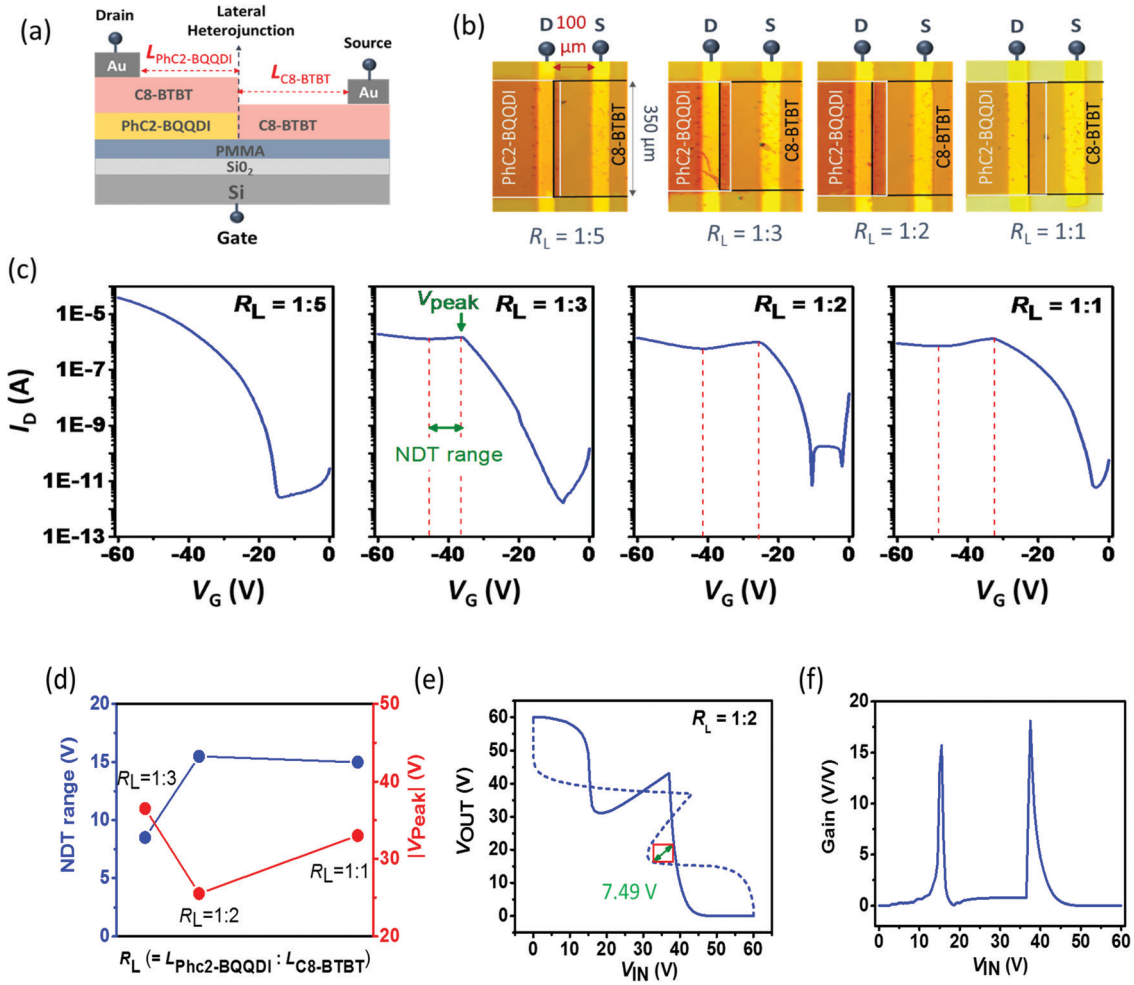

Fig. 2 (a) Schematic illustration of the AAT demonstrating the channel lengths, $L_{Phc_2\text{-}BQQDI}$ and $L_{C8\text{-}BTBT}$. (b) Different geometries of the AATs. (c) Geometry dependent transfer characteristics (at V_D = −60 V) of the AATs. (d) V_{peak} and NDT ranges of the AATs as a function of PhC_2-BQQDI to C8-BTBT channel length ratio (R_L). (e) Butterfly curve of the ternary inverter at V_{DD} = 60 V for R_L = 1 : 2 with the estimated SNM. (f) Gain values of the inverter as a function of applied input voltage.

A schematic illustration of the AAT structure is shown in Fig. 2(a) to define the two parameters, $L_{Phc_2\text{-}BQQDI}$ and $L_{C8\text{-}BTBT}$. $L_{Phc_2\text{-}BQQDI}$ indicates the length of PhC_2-BQQDI channel from the lateral edge of the heterojunction to the drain electrode (D), whereas $L_{C8\text{-}BTBT}$ signifies the length of C8-BTBT channel from the lateral edge of the heterojunction to the source electrode (S). Fig. 2(b) and (c) show the optical microscope images with the different R_L values and the transfer characteristics of the corresponding devices. In the transistor with R_L = 1 : 5, namely with the shortest $L_{Phc_2\text{-}BQQDI}$, no NDT range was observed. The AATs only showed a normal p-type transistor operation because the charge carriers flow only through the continuous C8-BTBT layer. Then, with varying R_L from 1 : 5 to 1 : 2, NDT range appeared as guided by the red dashed line in Fig. 2(c) and the NDT range gradually increased from 0 V to 16 V. This is because the electrons and holes start flowing across the lateral heterojunction and the effect of electron depletion becomes more pronounced with the increasing $L_{Phc_2\text{-}BQQDI}$. Finally, at R_L = 1 : 1, no further enhancement of NDT range was observed. Along with the variation in the NDT range, a shift in V_{peak} was also observed towards positive V_G from −36 V to −25 V when R_L was varied from 1 : 3 to 1 : 2. Nevertheless, at R_L = 1 : 1, V_{peak} returned again towards a negative V_G of −32 V. It is noted that V_{peak} determines the transition input voltage from logic 1/2 to logic 0 in the ternary inverter. Besides, the NDT range coincides with the logic 1/2 width. From these points of view, R_L = 1 : 2 emerged as the optimized AAT geometry to achieve a long logic 1/2 width (~16 V) and a suitable transition voltage from logic 1/2 to logic 0 (V_{IN} ~ 35 V for V_{peak} ~ −25 V) in the ternary inverter.

Fig. 2(e) shows the butterfly curve of the ternary inverter with the optimized AAT geometry. In accordance with the transfer characteristics of the AAT, the inverter exhibited an improved VTC with logic 1 at V_{OUT} = 60 V (0 V < V_{IN} < 12.5 V), logic 1/2 at V_{OUT} = 35 V (19 V < V_{IN} < 36 V) and logic 0 at V_{OUT} = ground (45 V < V_{IN} < 60 V). The enhanced logic 1/2 width induced an SNM of 7.49 V in the ternary inverter, which was 35% of the ideal value ($\sqrt{2}$ V_{DD}/4 = 21.21 V).[33] The gain values obtained at V_{IN} = 15 V (the transition input voltage from logic 1 to logic 1/2) and V_{IN} = 40 V (the transition input voltage from logic 1/2 to logic 0) were 16 V/V and 18 V/V,

respectively, as shown in Fig. 2(f). As described above, the geometry optimization achieved some improvement in the VTC of the ternary inverter. However, the obtained SNM still does not satisfy the requirements in the practical applications.

Finally, we utilized the contrasting optical responses of the C8-BTBT and PhC_2-BQQDI semiconductors to further improve the SNM of the inverters. Fig. 3(a) and (b) show the impact of UV and visible light irradiation on the PhC_2-BQQDI and C8-BTBT transistors, respectively. The visible light irradiation had two major impacts on the transfer characteristics of the PhC_2-BQQDI transistor. One was drain current enhancement, which was induced by the generation of charge carriers. At $V_G = V_D =$ 60 V, I_D was increased from 22 μA in the dark to 27 μA under visible light irradiation (Fig. 3(a)). The other impact was a threshold voltage reduction of 2 V, which was caused by the accumulation of minority charge carriers in the channel region.[44–46] Under light irradiation, a large number of excitons were generated in the PhC_2-BQQDI layer due to its characteristic absorption in the visible light wavelength range (Fig. S5, ESI†). These excitons were then separated into electrons and holes under the applied electric field. After the separation, the majority carriers (electrons in PhC_2-BQQDI) easily flowed towards the drain electrode whereas the minority carriers (holes in PhC_2-BQQDI) remained at the interfaces as well as in the channel region due to their marginal mobility. The accumulated minority charge carriers reduced the potential barrier at the source/channel interface and then promoted charge injection from the source electrode, which led to the reduction in the threshold voltage. In contrast to the result with visible light, the PhC_2-BQQDI transistor properties remained completely invariant under UV light irradiation. On the other hand, the C8-BTBT transistor exhibited photoresponsivity only under UV light irradiation (Fig. 3(b)) because of the characteristic absorption in the UV range (Fig. S5, ESI†). The V_{th} value of the devices decreased by 9 V together with an increase in the I_D value from 52 μA in the dark to 88 μA under UV light irradiation at $V_G = V_D = -60$ V. In marked contrast to the PhC_2-BQQDI transistor, the C8-BTBT transistor did not respond to visible light irradiation. This contrasting light induced variations in the PhC_2-BQQDI and C8-BTBT layers resulted in an opposite shift in the inverter VTC under visible and UV light as shown in Fig. 3(c). The shift in the inverter output characteristics was also supported by the light induced shift in the transfer characteristics of the AATs as shown in Fig. S6 in the ESI.† Under visible light, the VTC was shifted towards a lower V_{IN} due to the V_{th} shift in the PhC_2-BQQDI layer. The suppression of I_D in the AATs under visible light, which is caused by the recombination of holes with the photo-generated electrons, also triggered this shift as observed in Fig. S6 (ESI†). Due to this visible light influenced shift in the VTC, the width of logic 1 state and the driving V_{IN} were reduced, *i.e.*, the ternary logic states were obtained with a lower input voltage. On the other hand, the V_{OUT} level of the logic 1/2 state was enhanced because of the generation of charge carriers in the PhC_2-BQQDI layers, which altered the resistance ratio between the AAT and the PhC_2-BQQDI transistor. These impacts upon visible light irradiation makes the VTC unbalanced. In contrast to the effect of visible light, the UV light irradiation induced a shift in the inverter VTC towards a higher V_{IN} due to the V_{th} shift of the C8-BTBT layer. This shift, in turn, extended the width of the logic 1

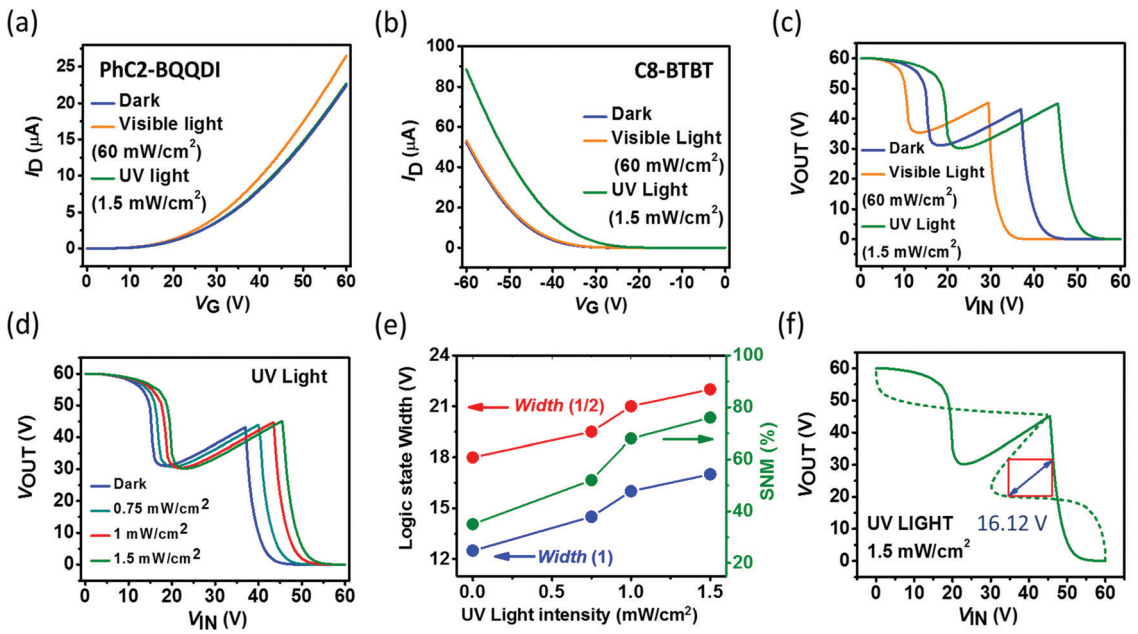

Fig. 3 Transfer characteristics (at $V_D = |60|$ V) of the (a) PhC_2-BQQDI and (b) C8-BTBT transistors, in the dark (blue lines), under visible light (orange lines) and under UV light irradiation (green lines). (c) Voltage transfer characteristics of the inverters in the dark (blue line), under visible light (orange line) and under UV light irradiation (green line). (d) Voltage transfer characteristics of the inverters under UV light inputs with various intensities. (e) Logic state widths and the values of SNM as a function of UV light intensity. (f) Voltage transfer characteristics of the inverter under UV light intensity of 1.5 mW cm^{-2} and the extracted value of SNM.

state. The width of the logic 1/2 state also increased due to the enhancement of the NDT range in the AATs. These UV-light-triggered variations in the inverter characteristics are expected to improve the SNMs in the ternary inverters. Therefore, we investigated the influence of UV light intensities on the inverter characteristics to explore the light tunability in a more quantitative way for the further optimization of the SNMs.

Fig. 3(d) shows the VTC with different UV light intensities. The widths of logic 1 and logic 1/2 are denoted as width (1) and width (1/2), respectively, and are plotted as a function of the UV light intensity in Fig. 3(e). Width (1) (blue line in Fig. 3(e)) increased monotonically with the increase in the UV light intensity from 12.5 V in the dark condition to 17 V under a UV light intensity of 1.5 mW cm^{-2}. Width (1/2) (red line in Fig. 3(e)) also exhibited a gradual enhancement from 17 V to 22 V. These UV light induced improvements in the logic state widths were reflected in the SNM of the ternary inverters. The SNM values increased from 7.5 V under dark condition to 16.1 V under the UV light intensity of 1.5 mW cm^{-2}, which was 76% of the ideal value. The butterfly curve of the ternary inverter under the UV light intensity of 1.5 mW cm^{-2} is shown in Fig. 3(f). The butterfly curves under the UV light intensities of 0.75 mW cm^{-2} and 1 mW cm^{-2} are shown in Fig. S7 (ESI†). In this manner, the use of UV light was found to be an effective technique not only to fine-tune the logic state widths and but also to induce a high endurance against the electrical noises in the ternary inverters.

Meanwhile, it is worth mentioning that although the VTC of the inverters degraded under visible light in terms of SNM (Fig. S8, ESI†), the contrasting photo response of the inverters under visible and UV light makes them suitable candidates for their potential application as inverter-based UV and visible light detectors. The primary advantage of the inverter-based photodetectors is their superior ability to convert the optical signals into the voltage output signals. This feature has the potential to overcome the difficulty in the measurement of nano-ampere (nA) level current signals, which is a major problem in the conventional photocurrent-based photodetectors.[47]

Thus, the contrasting optical responses of C8-BTBT and PhC_2-BQQDI semiconductors enable us to control the logic state properties improving the SNM of the inverters. Furthermore, this feature also opens up the possibility for the inverters to be used as photodetectors. In a similar manner, optically tunable MVL has been reported in α-6T/PTCDI-C8 and $MoSe_2$/WSe_2 systems.[29,35] In α-6T/PTCDI-C8 system, the photoresponse of α-6T was superior to that of PTCDI-C8 under both UV and visible light irradiation, and this impeded effective light tunability. In addition, visible and UV light was found to degrade the V_{OUT} level of logic 1 and logic 1/2 state, respectively.[29] On the other hand, in $MoSe_2$/WSe_2 system, both $MoSe_2$ and WSe_2 responded under 638 nm light irradiation. As a result, the light irradiation was found to be useful to enhance the V_{OUT} level of logic 1/2 state. However, no effective controllability in the logic state positions and widths were observed.[35] The combination of C8-BTBT and PhC_2-BQQDI provides an advantage in this regard. We can separately activate C8-BTBT or PhC_2-BQQDI using a UV or visible light signal and precisely control the width, position and V_{OUT} level of the inverter logic states. Furthermore, improvement in the noise immunity of the inverters were achievable through UV light signals, which reveals the merits of the proposed devices in opto-electronic logic applications.

3. Conclusion

In conclusion, we demonstrated an organic NDT transistor based on a heterojunction consisting of a new material combination, namely C8-BTBT for the p-type and PhC_2-BQQDI for the n-type semiconductors, respectively. Due to the high carrier mobility of these materials, the proposed AATs were able to exhibit a high on/off ratio of 10^6. These AATs also enabled us to achieve a complete V_{OUT} swing from V_{DD} to ground and an ideal logic 1/2 to logic 1 V_{OUT} ratio of 0.5 in the ternary inverters. Then, the AAT geometry was properly optimized to enhance the inverter logic 1/2 width. However, the obtained VTC were still not suitable for the practical applications of the inverters due to the poor SNM. Therefore, in order to improve the SNM, we demonstrated an efficient technique of UV light irradiation on the ternary inverters, which enabled an optical control on the inverter VTC and yielded a high SNM of 76%. The contrasting photoresponsivity of C8-BTBT/PhC_2-BQQDI material combination played the most critical role in this regard. This work, thus, represents progress towards the development of light tunable, high performance organic MVLs for future opto-electronic logic applications.

4. Experimental section

The transistors and inverters were fabricated on highly doped Si wafers with a 200 nm-thick SiO_2 layer, which worked as a bottom gate electrode and a dielectric layer, respectively. Prior to the device fabrication, the substrates were properly cleaned by ultra-sonication with acetone and isopropanol. They were then rinsed in deionized water and dried in a nitrogen gas flow. Then, a thin layer (~10 nm) of poly(methyl methacrylate) (PMMA) was spin-coated on top of the SiO_2 surface to passivate the surface defects and to facilitate the transport of the charge carriers at the dielectric–semiconductor interface.[26,48] Thereafter, organic semiconductors, PhC_2-BQQDI (~16 nm) and C8-BTBT (~19 nm), were thermally evaporated on the PMMA surface as n-type and p-type channels, respectively, at a background pressure of 10^{-7} Pa using corresponding shadow masks. These two semiconductors were partially overlapped to form the heterojunction, which played a major role to give rise to the NDT characteristics. Fixed deposition rates of 0.8 Å min^{-1} and 1.0 Å min^{-1} were maintained for the PhC_2-BQQDI and C8-BTBT layers, respectively. Finally, gold (Au) source and drain electrodes were deposited on the organic semiconductors by thermal evaporation using another shadow mask to complete the AAT structure. The channel length and width of the AATs were 100 μm and 350 μm, respectively. The ternary

inverters were produced by connecting the AAT with an n-channel PhC_2-BQQDI transistor in series.

All electrical measurements were performed in a vacuum ($\sim 10^{-1}$ Pa) using an Agilent B1500A semiconductor parameter analyser. The photoresponse of the devices was monitored using a xenon lamp as the light source. Reflecting mirrors were used to extract the UV and visible light, which had wavelength ranges of 300–385 nm and 385–800 nm, respectively.

Conflicts of interest

There are no conflicts to declare.

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