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A flexible dual-gate hetero-synaptic transistor for spatiotemporal information processing†

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Artificial synapses based on electrolyte gated transistors with conductance modulation characteristics have demonstrated their great potential in emulating the memory functions in the human brain for neuromorphic computing. While previous studies are mostly focused on the emulation of the basic memory functions of homo-synapses using single-gate transistors, multi-gate transistors offer opportunities for the mimicry of more complex and advanced memory formation behaviors in biological hetero-synapses. In this work, we demonstrate an artificial hetero-synapse based on a dual-gate electrolyte transistor that can implement *in situ* spatiotemporal information integration and storage. We show that electric pulses applied on a single gate or unsynchronized electric pulses applied on dual gates only induce volatile conductance modulation for short-term memory emulation. In contrast, the device integrates the electric pulses coincidently applied on the dual gates in a supralinear manner and exhibits nonvolatile conductance modulation, enabling long-term memory emulation. Further studies prove that artificial neural networks based on such hetero-synaptic transistors can autonomously filter the random noise signals in the dual-gate inputs during spatiotemporal integration, facilitating the formation of accurate and stable memory. Compared to the single-gate synaptic transistor, the classification accuracy of MNIST handwritten digits using the hetero-synaptic transistor is improved from 89.3% to 99.0%. These findings demonstrate the great potential of multi-gate hetero-synaptic transistors in simulating complex spatiotemporal information processing functions and provide new platforms for the design of advanced neuromorphic computing systems.

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Introduction

The human brain is highly efficient in executing various complex cognitive tasks such as learning, memory and decision making, outperforming state-of-the-art digital computers.[1,2] Synapses are the fundamental building blocks of the human brain for learning and memory, and their strength (synaptic weight) can adaptively adjust in response to neural spikes for information processing.[3–6] For decades, great efforts have been devoted to building electronic devices for the emulation of various memory formation behaviors in synapses, dreaming of physically realizing artificial intelligence systems with learning abilities close to the human brain.[1,7,8]

An electrolyte gated transistor is a typical device that consists of an ionic gating dielectric and channel layer made of semiconductors.[5,9,10] The voltage pulses applied on the gate terminal can tune the concentration of mobile ions around the channel layer, which modulates the channel conductance through ionic electrostatic or/and chemical doping effects.[8,11,12] Extensive studies have demonstrated the feasibility of the electrolyte gated transistor to emulate the memory formation of biological synapses, such as short-term and long-term memory effects, with excellent performances including good operation stability, low cycle to cycle variations, and high energy efficiency.[3,13–16] However, previous studies are mainly limited to the emulation of simple memory functions in homo-synapses using single-gate transistors, where the memory effects are solely dependent on the electric pulses applied on the single gate.[4,17–20] In contrast, biological hetero-synapses having sophisticated morphologies can effectively integrate the inputs delivered by multiple presynaptic terminals during memory formation, and

the memory behaviors are determined by the spatiotemporal correlations among the stimuli. Although experimental demonstration of hetero-synaptic functions has been realized in multi-terminal memristors, the inputs applied on the additional terminals mainly play a role of modulation for homo-synaptic devices, rather than being used for information processing.[21,22] In this case, an artificial hetero-synapse to reproduce spatiotemporal information processing functions remains largely unexplored. Recent studies showed that a multi-gate electrolyte gated transistor can be obtained by incorporating additional gate terminals,[5,17,23–28] offering opportunities for the implementations of complex memory functionalities of hetero-synapses, such as *in situ* noise filters and storage that are critical for accurate and stable memory storage.

In this work, we experimentally demonstrate an artificial hetero-synapse based on a dual-gate electrolyte gated transistor that is capable of computing and memorizing spatiotemporal information of multiple inputs. We show that electric pulses applied on a single gate or unsynchronized electric pulses applied on dual gates induce volatile conductance modulation and exhibit a short-term memory effect. In contrast, the application of electric pulses onto the two gate terminals in synchronization can lead to a super-linear summation of the device current and result in long-term memory formation, performing coincident detection computing and memory operations. Additional simulation results suggest that an artificial neural network built with such synaptic devices can effectively filter the random noise signals during information integration, helping to form accurate and stable memory. Compared to the single-gate synaptic transistor, the classification accuracy of MNIST handwritten digits is increased from 89.3% to 99.0%. These studies highlight the potential of the multi-terminal electrolyte gated transistor in emulating complex spatiotemporal information processing functions for efficient neuromorphic computing.

Results and discussion

Fig. 1a illustrates the schematic of a hetero-synapse with two presynaptic terminals and a postsynaptic terminal. The presynaptic terminals stimulated by neural spikes release neurotransmitters that bind to receptors on the postsynaptic terminal, generating an excitatory postsynaptic current (EPSC) and inducing memory formation.[29,30] Fig. 1b illustrates a dual-gate electrolyte gated transistor inspired by the biological counterpart, where the two gates and the drain/source channel correspond to the presynaptic terminals and postsynaptic terminal respectively. The voltage pulses applied on the gate and the drain/source current correspond to presynaptic spikes and postsynaptic current. The ionic transistor reported here employs [EMI][TFSA] as the ion-gel, where the mobile ions $[TFSA]^-$ play the role of neurotransmitters whose spatial distribution in the device is controlled by the electric stimulation conditions. The organic semiconductor P3HT is chosen as the channel material due to its good chemical stability, easy fabrication and compatibility with the ion gel. An optical image of the fabricated transistor device is illustrated in Fig. 1c. The fabrication process of the device is depicted in Fig. S1† in the ESI.† Fig. 1d shows the transfer characteristic curve of the synaptic transistor, obtained by monitoring the drain current during the sweep of the gate voltage (1.0 V → −1.0 V → 1.0 V). A hysteretic window in the I_D–V_G curve at negative gate voltages was observed, and the conductance ratio reaches ∼1000, suggesting the effective modulation of the channel conductance. The output characteristic curve of the ionic transistor is systematically investigated, as shown in Fig. 1e. With the negative gate voltage applied, the drain current increases with the drain voltage, and the increasing rate is proportional to the gate voltage amplitude. These results proved the reliable modulation of conductance in the electrolyte gated transistor transistors. Fig. 1f shows that the characteristic peak positions in the Raman spectrum of the P3HT channel shift to lower values after device gating, indicating that the conductance modulation stems from the formation of positive polarons during the voltage gating induced electrostatic/electrochemical doping of the P3HT films.[31–34]

Notably, owing to the intrinsic flexibility of the P3HT and [EMI][TFSA] ion gel as flexible organic materials, the ionic transistor device can be deposited on flexible substrates such as PET (polyethylene terephthalate). Fig. 1g shows the channel current of the device in response to gate pulses when the PET flexible substrate is flattened ($R = \infty$), with a bending radius of 1 cm (R = 1 cm) and a bending radius of 0.5 cm (R = 0.5 cm) respectively. It shows that under different pulse stimulation conditions (amplitude and pulse width), the device shows negligible conductance variations under different bending conditions, indicating its potential for flexible electronic application (Fig. 1h and i).

To evaluate the performance of the electrolyte gated transistor for memory function emulation, we studied the evolution of channel current with the gate pulses applied onto the gates. Fig. 2a shows the schematic of applying electric pulses on a single gate of the device, and a typical current response (EPSC) triggered by the gate pulse (−1.2 V and 100 ms) is shown in Fig. 2b. During pulse stimulation, the postsynaptic current increases from 8.9 nA to 190 nA quickly and then decays rapidly to the resting state within 500 ms. This result indicates that the voltage pulse drives $[TFSA]^-$ ions towards the P3HT interface during its application and these ions spontaneously diffuse back after the pulse is removed. This process emulates the short-term memory formation and can be explained by the formation of a volatile electric double layer at the P3HT surface that causes electrostatic doping effects.[35] The short-term dynamics enable the device to emulate the paired pulse facilitation (PPF) of synapses, where the second pulse (−1.2 V and 100 ms) closely following the first identical pulse can excite a higher device current (Fig. 2c). The inset in Fig. 2c plots the relationship between the PPF index and the time interval, where the PPF index refers to the ratio between A_2 and A_1, and A_1 and A_2 represent the device current during the first and second pulse stimulations respectively. The PPF index decreases quickly with the increase of the time interval in the paired pulses, owing to the increased time interval that allows the back diffusion of more ions and prevents ion accumulation at the P3HT interface.

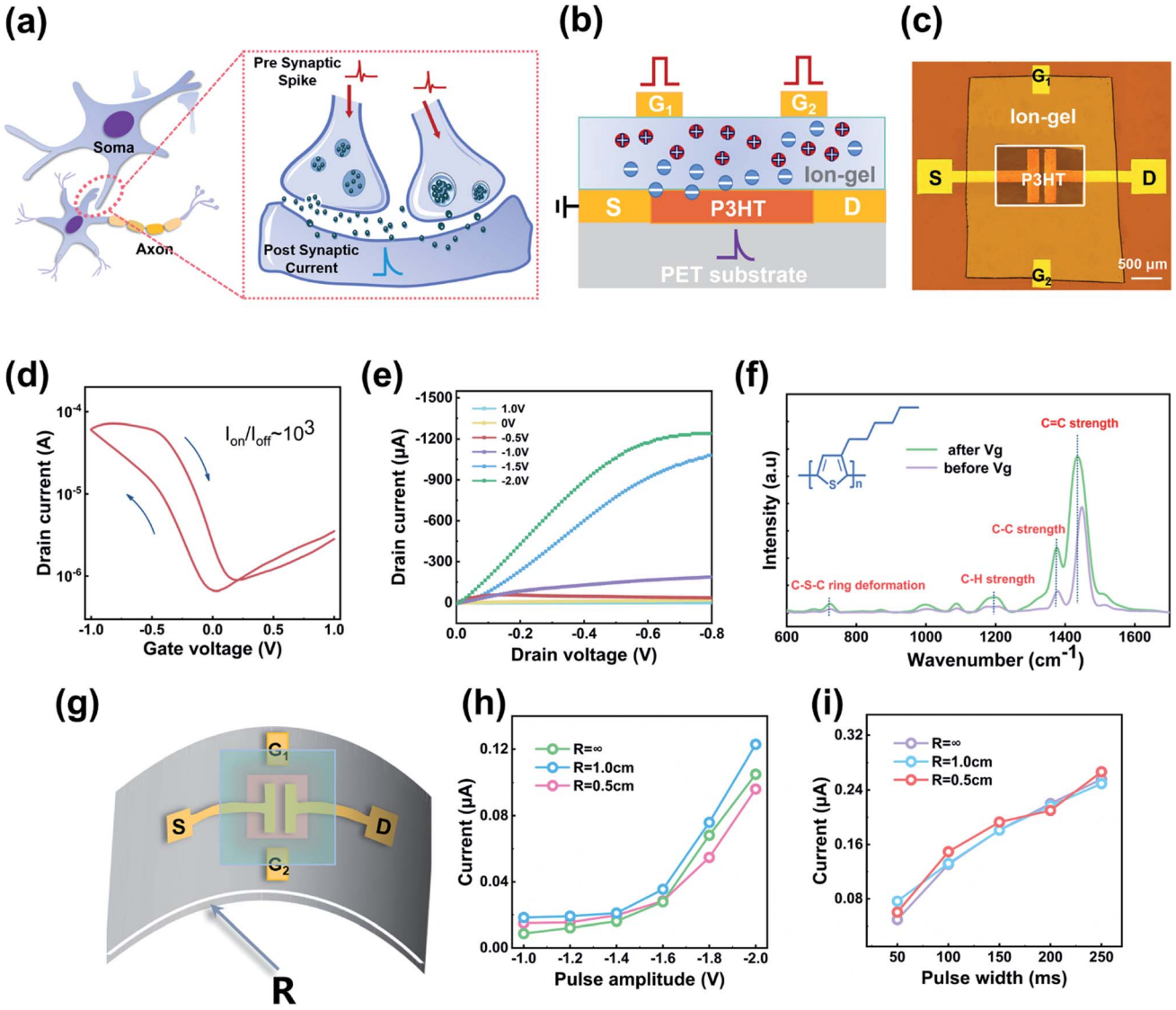

Fig. 1 (a) Schematic of a biological hetero-synapse with two presynaptic terminals and a postsynaptic terminal. (b) Schematic of a dual-gate electrolyte gated transistor. (c) Optical image of the P3HT based dual-gate electrolyte gated transistor. The channel length is 100 μm. Scale bar: 500 μm. (d) Transfer characteristic curve of the transistor measured during gate voltage sweeping. (e) Output characteristic curves of the transistor at different gate voltages. (f) Raman spectra of the P3HT channel film before and after gate voltage application. (g) Scheme showing a bent electrolyte gated transistor. (h) The channel current of the device in response to an electric pulse with varying amplitude at different bending states. (i) The channel current as a function of the pulse width for the device at different bending states.

The decay trend can be well fitted by an exponential decay equation illustrated in the inset in Fig. 2c. The characteristic decay time constant τ_1 is 203.83 ms, on the same order of magnitude as that in biological synapses.[30,36,37] Fig. 2d shows the EPSC current obtained in a device stimulated by pulses with different pulse frequencies (2.8 Hz, 3.3 Hz, 4.0 Hz, and 5.0 Hz). The peak EPSC current increases from 555.81 nA to 802.3 nA when the frequency increases from 2.8 Hz to 5.0 Hz (Fig. 2e). Likewise, with the pulse frequency fixed, the device current increases with the number of applied pulses (Fig. 2f). Fig. 2g shows that the peak EPSC current increases from 712.1 nA to 1690.1 nA when the pulse number increases from 15 to 50. To this end, the device possesses an intrinsic short-memory effect when programmed by the given electric pulses applied on a single gate. Notably, increasing the pulse amplitude can lead to a long-term memory effect, which was avoided in the implementations (Fig. S2, ESI†).

In biological neural networks, a postsynaptic terminal can receive excitatory synaptic inputs from multiple presynaptic terminals clustered by a dendritic tree. The strength of the inputs contributed by a single presynaptic terminal is usually insufficient to drive the membrane potential of the postsynaptic terminal to the threshold for stable memory formation.[23,24,30] However, the postsynaptic terminal can effectively accumulate and amplify the inputs from multiple presynaptic terminals, performing supralinear spatiotemporal signal integration. A schematic depicting this process is illustrated in Fig. 3a, showing the EPSC triggered by the two synchronized spikes

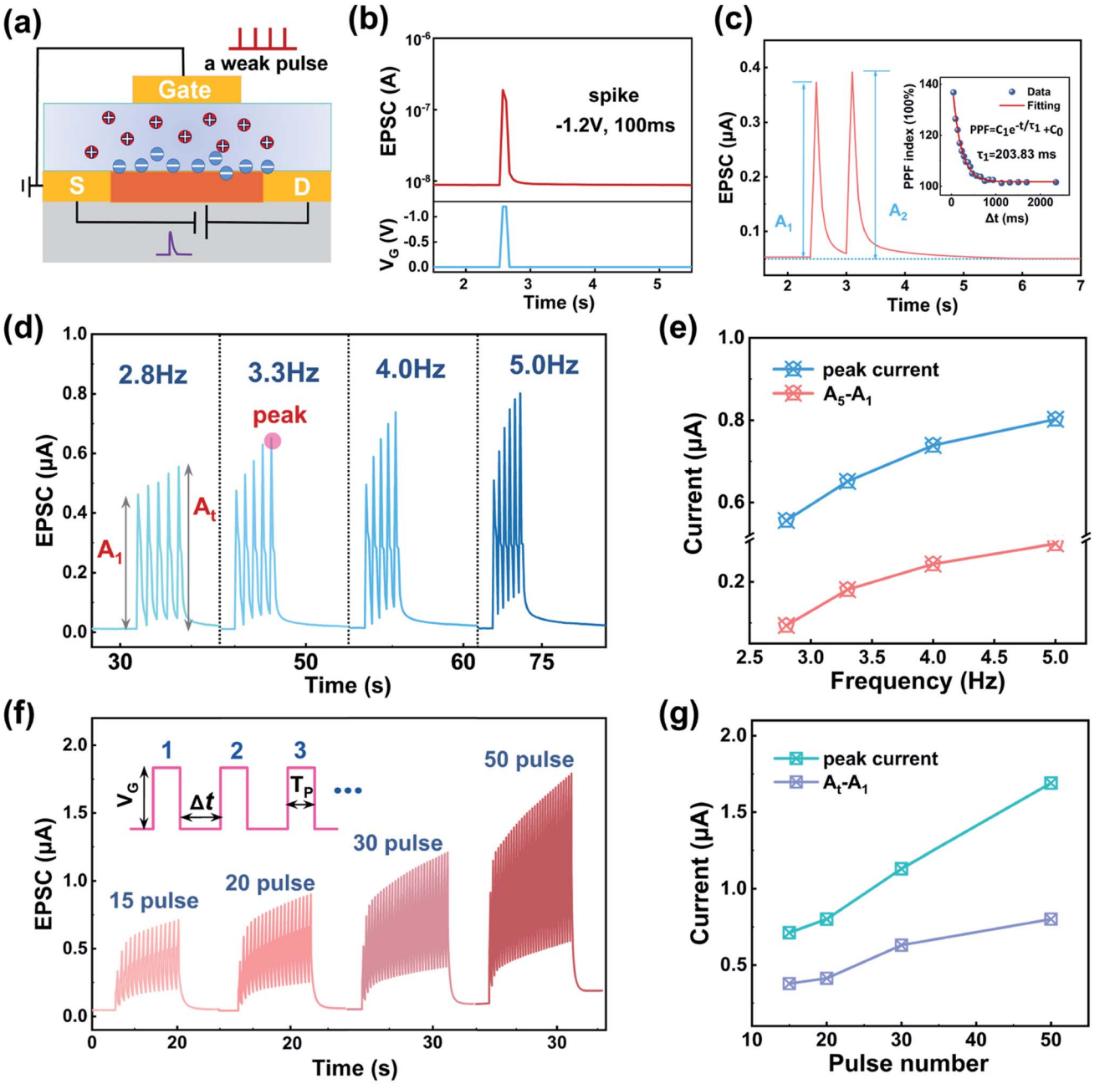

Fig. 2 (a) Schematic showing the electrostatic ion modulation of the channel layer in the electrolyte gated transistor under single-terminal voltage gating. (b) A typical EPSC obtained in the electrolyte gated transistor triggered by an electric pulse (−1.2 V and 100 ms). (c) EPSCs triggered by a pair of electric pulses with a time interval of 500 ms. A_1 and A_2 represent the current intensity after the first and second pulse stimulations, respectively. Inset: PPF index as a function of pulse interval (Δt); the curve is fitted with an exponential decay function. (d) EPSCs excited by five electric pulses (−1.2 V and 100 ms) with different frequencies. (e) Peak postsynaptic current and peak variation (A_t–A_1) as a function of the pulse frequency in (d). (f) EPSCs excited by electric pulses (−1.4 V, 0.5 s) with different pulse numbers. (g) Peak current and peak current difference (A_t–A_1) as a function of pulse number in (f).

separately delivered by two presynaptic terminals (red solid line), much higher than that produced by either one (pink dotted line). To explore the feasibility of implementing these effects in a dual-gate synaptic transistor, we studied the response of the synaptic transistor to pulse stimuli applied onto two gates. Fig. 3c illustrates the EPSCs excited by electric pulses (−1.2 V and 100 ms) applied to the presynaptic terminals, *i.e.* gate 1 (G_1) and gate 2 (G_2), respectively. Specifically, when the electric pulse was applied to G_1 or G_2 at different moments, each stimulation event excited an EPSC of ~0.3 μA. In contrast, for the electric pulses applied to G_1 and G_2 simultaneously, we can detect a much higher EPSC (~1.1 μA). Moreover, the difference in the current intensity increases with the pulse number (Fig. 3d). Fig. 3e plots the measured EPSC as a function of the

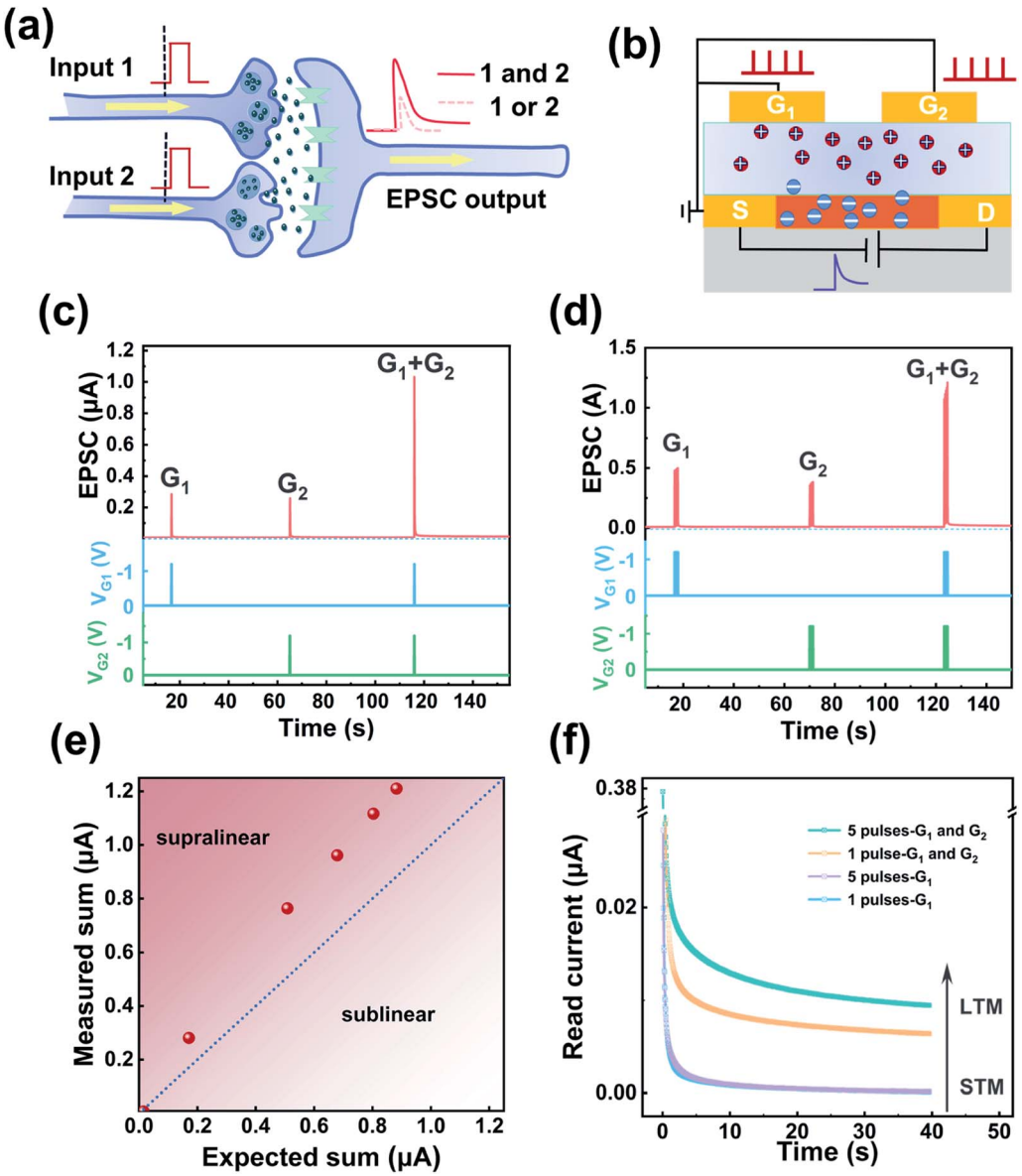

Fig. 3 (a) Illustration of a hetero-synapse excited by electric inputs transmitted by two presynaptic terminals and the resulting EPSC as an output. (b) Schematic showing the electrochemical ion modulation of the channel layer in the transistor under dual-terminal voltage gating. (c) EPSCs excited by the presynaptic spike (−1.2 V and 100 ms) separately/simultaneously applied on G_1 and G_2. (d) EPSCs excited by five presynaptic spikes (−1.2 V, 100 ms, and 3.3 Hz) separately/simultaneously applied on G_1 and G_2. (e) The measured sum (MS) current plotted as a function of the expected sum (ES) current. (f) Time-dependent device current under different stimuli conditions.

expected sum for different pulse amplitudes (0.6 V, 0.8 V, 1.0 V, 1.2 V and 1.4 V). The expected sum (ES) is defined as the arithmetic sum of the EPSC when G_1 and G_2 were triggered separately (ES = A_1 + A_2), and the measured sum (MS) is the EPSC when the G_1 and G_2 were triggered simultaneously. It is apparent that the ES is much higher than the MS, indicating the supralinear integration of the synchronized inputs delivered by multiple gates. Importantly, we note that after experiencing dual-gate stimulation, the device shows a nonvolatile conductance modulation effect, exhibiting a long-term memory effect, as demonstrated in Fig. 3f. The observation is likely caused by the accumulation of abundant ions near the channel that penetrate into the P3HT layer to induce the electrochemical doping effect (Fig. 3b). The strong chemical bonding between the ion and channel layer prevents the back diffusion of ions to the gate dielectric after the removal of the applied pulses, which account for the improved retention performance, thus enabling long-term memory formation.[2,36] This process emulates the spatiotemporal integration of spike inputs of hetero-synapses during memory formation which promotes accurate and stable memory formation.

In Fig. 4, we simulated an artificial neural network using such a multi-gate electrolyte gated transistor for MNIST (Modified National Institute of Standards and Technology)

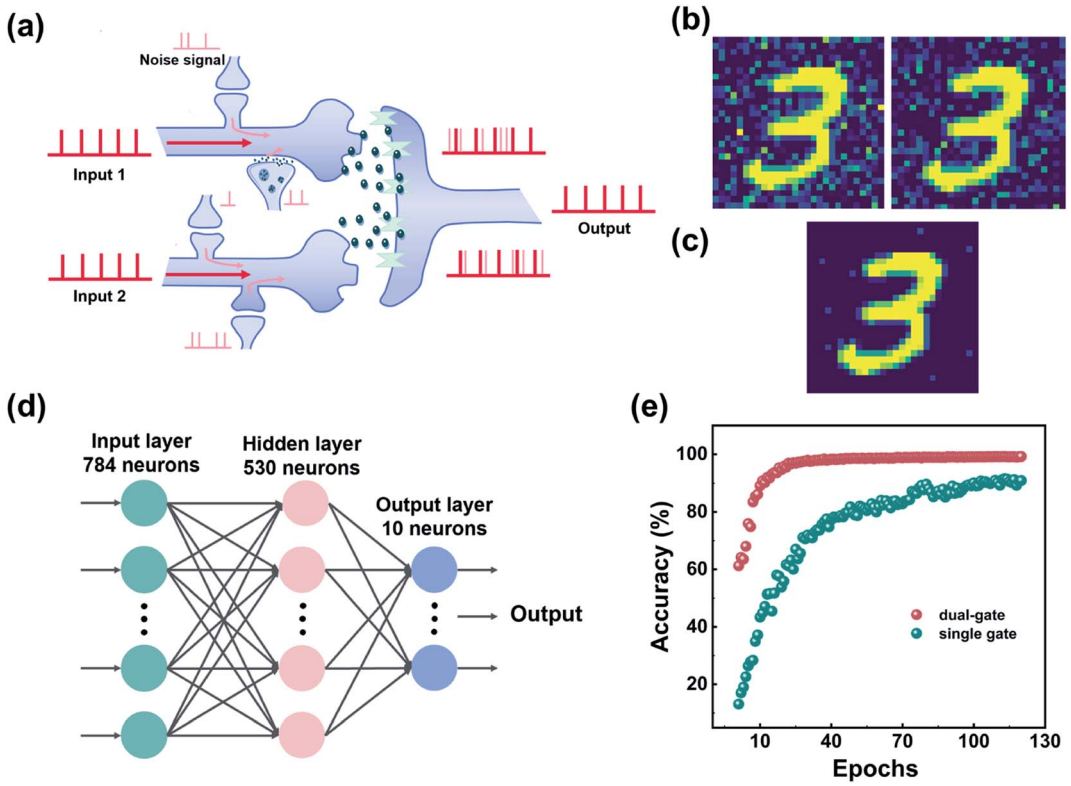

Fig. 4 (a) Illustration of a hetero-synapse performing spatiotemporal signal integration and memorization. Noise signals are introduced during the transmission of the original signals. (b) Examples of two noisy images separately delivered to the dual-gate hetero-synaptic transistor for processing. (c) The image stored in the dual-gate hetero-synaptic transistor after processing. (d) Illustration of a neural network based on the hetero-synaptic transistor for MNIST image recognition. (e) Comparison of the classification accuracy for the networks based on the dual-gate hetero-synaptic transistor and the single-gate homo-synaptic transistor.

handwritten digits training and recognition. A fully connected artificial neural network (784 × 10) is established for the training and inference (Fig. 4d). The 784 input neurons correspond to a digit (0–9) image with 28 × 28 pixels, and the 10 output neurons correspond to the 10 digits. During the implementations, both gates act as the presynaptic terminals to transmit the signals delivered by the same neuron. Random noises are created and superimposed with the images transmitted by each presynaptic terminal. Two typical digit patterns with noises applied to the presynaptic terminals are illustrated in Fig. 4b. As the noise signals transmitted by each path are random and uncorrelated, they are mostly unsynchronized in spatial and temporal domains. The simulation result shows that when these digit patterns are delivered to the device, the noise components can be autonomously filtered with the overlapped patterns retained, producing a high-quality digit image with enhanced feature contrast (Fig. 4c). Fig. 4e shows the recognition rate as a function of the training epochs, for the dual-gate transistor base artificial neural network. A recognition rate of ~99.0% is reached after ~90 training epochs. A control experiment using the single-gate synaptic device for the training and inference was also executed. Owing to the increased probability of learning the noises, the accuracy of the trained network in classifying the digit patterns drops to only 89.3%, and needs more training epochs (~120). These results prove that the dual-gate electrolyte gated transistor is more tolerant to noise disturbances than the conventional single-gate electrolyte gated transistor, highlighting the superiority of employing the multi-gate electrolyte gated transistor for complex hetero-synaptic function emulation and neuromorphic computing. For practical implementations using such proof-of-concept devices, continued efforts will be needed for further device minimization and high-density integration.

Conclusion

In conclusion, we report a flexible artificial hetero-synapse based on dual-gate electrolyte gated transistors with spatio-temporal information integration and storage capability. The device can effectively capture and store the signals applied to the dual gates that occurred in synchronization, performing *in situ* coincident detection and memory function of biological hetero-synapses. Such a device can autonomously filter the random noise signals in the multiple inputs and promote the formation of accurate and stable memory, leading to enhanced classification accuracy of the objects. These results open up new avenues for the efficient implementation of complex biological hetero-synaptic functions in physical devices and can possibly be used in flexible intelligent wearable systems.

Experimental

Device fabrication

The polyethylene terephthalate (PET) substrate was cleaned with acetone, alcohol, and deionized water using ultrasonic cleaning before device fabrication. Gold films (80 nm thick), serving as the gate, source and drain electrodes, were deposited through electron beam evaporation with a patterned metal shadow mask covered on the PET substrate. The channel length is 100 μm, and the dual gates are 1 mm away from the channel. The P3HT (purchased from Aladdin) solution was synthesized by dissolving weighed P3HT powders in chlorobenzene solution, with a concentration of 10 mg ml^{-1}. The P3HT channel film (100 nm thick) was fabricated by spin-coating the P3HT solution in chlorobenzene (10 mg ml^{-1}) between the source and drain electrodes on a substrate, followed by curing at 70 °C for two hours.

Poly(vinylidene fluoride-*co*-hexafluoropropylene) (P(VDF-HFP)) (purchased from Macklin) and 1-ethyl-3-methylimidazoliumbis (trifluoromethylsulfonyl) amide ([EMI][TFSA]) were dissolved in acetone with a weight ratio of 1 : 4 : 7 under vigorous stirring at 50 °C for 4 hours, and then spin-coated on a glass substrate. After being baked in a vacuum at 70 °C for 24 hours, the ionic gel was transferred to the PET substrate spin-coated with P3HT thin films to complete the transistor fabrication.

Sample characterization

All of the electrical measurements were conducted on a Lakeshore probe station with a Keithley 4200 semiconductor parameter analyzer at room temperature. Throughout the studies, we fabricated ~150 devices in total, and the yield is over 90%. The variation of the current response to pulse stimulation is ~4% for the devices fabricated in the same batch (Fig. S3, ESI†). To evaluate the device performance at different bending states, we attached the flexible device on a customized semi-cylindrical bending mold, followed by performing electrical characterization. The morphologies were characterized using a Scanning Electron Microscope (SEM, FEI Quanta FEG 250, American FEI, USA). Raman spectroscopy with a laser micro-Raman microscope (NRS-3100, JASCO Corporation, Japan) was used to obtain the Raman spectrum of the P3HT film in the transistor before and after programming.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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