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Flexible electric-double-layer thin film transistors based on a vertical $InGaZnO_4$ channel

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Flexible electric-double-layer (EDL) thin film transistors (TFTs) based on a vertical $InGaZnO_4$ (IGZO) channel are fabricated at room temperature. Such TFTs show a low operation voltage of 1.0 V due to the large specific gate capacitance of 3.8 μF cm^{-2} related to electric-double-layer formation. The threshold voltage, drain current on/off ratio and subthreshold swing are estimated to be −0.1 V, 1.2×10^6 and 80 mV per decade, respectively. The combination of low voltage, high current on-to-off ratio and room temperature processing make the flexible vertical-IGZO-channel TFTs very promising for low-power portable flexible electronics applications.

Introduction

Recently, there has been a strong interest in the use of $InGaZnO_4$ film as a channel layer in thin film transistors (TFTs).[1–5] However, these TFTs usually require high operation voltages (>10 V). High operation voltage results in high power consumption, a critical barrier for portable, battery-powered applications. To solve the problem, extensive consideration has been given to gate dielectric transistors with higher specific capacitance, due to two benefits of higher specific capacitance: much higher output current at a given applied gate voltage and much lower operating voltages, which are a direct consequence of the large two-dimensional electron density that can be induced in the channel by means of the high specific capacitance. In order to get higher specific capacitance for low-voltage operation, high-*k* dielectrics are used as the gate dielectrics for organic TFTs, these devices exhibit operating voltages of 5–10 V and <4 V.[6,7] Here, we found that microporous SiO_2-based solid-electrolytes can provide huge electric-double-layer (EDL) capacitance and negligible leakage current owing to the lack of electron carriers and limited mobility of mobile ions. In this work, vertical IGZO TFTs gated by microporous SiO_2-based solid-electrolyte were fabricated, compared with traditional transistors, vertical-structured TFTs could easily control channel length, because it exactly corresponds to the thickness of the channel layer. The operating voltage of such TFTs was reduced to 1.0 V, the drain current on/off ratio and subthreshold swing are estimated to be 1.2×10^6 and 80 mV per decade, respectively.

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Experimental

Flexible EDL vertical IGZO channel TFTs with a top gate were fabricated on paper substrates at room temperature, as shown schematically in Fig. 1. The paper substrate is common chrome paper, which is one of the most abundant materials and is a renewable resource. First, a 2 μm-thick SiO_2 buffer layer was deposited on bare paper substrates by the PECVD method using a mixture of SiH_4 and O_2 as the reactive gases; the processing pressure was 20 Pa. Secondly, ITO drain electrode with a thickness of 150 nm was deposited on the SiO_2 buffer layer by dc sputtering. Thirdly, semiconducting IGZO (Ga_2O_3 : In_2O_3 : ZnO = 1 : 1 : 2 mol%) with ~40 nm thickness is deposited by RF magnetron sputtering onto the source electrode, using a power of 110 W, a working pressure of 0.5 Pa, and an O_2/Ar [0.39/15 SCCM] mixed-gas atmosphere. Next, 20 nm ITO film is deposited on IGZO layer by radio-frequency magnetron sputtering of ITO target, where the ITO layer works as the bottom source electrode. Then, microporous SiO_2 gate dielectric with the thickness of about 5.0 μm was deposited on bottom ITO source electrode by PECVD at room temperature. Finally, 150 nm ITO film is deposited on top of the dielectric layer as the top gate electrode. The capacitance–frequency (*C*–*f*) measurement of microporous SiO_2-based solid electrolyte are performed using an Agilent 4294A precision impedance analyzer. The transfer/output characteristics of the transistors are measured using a semiconductor parameter characterization system (Keithley 4200 SCS) and a micromanipulator probe station in a clean and shielded box at room temperature in the darkness.

Results and discussion

To understand the operating mechanism of such vertical IGZO channel TFTs, an energy band model is proposed. Before

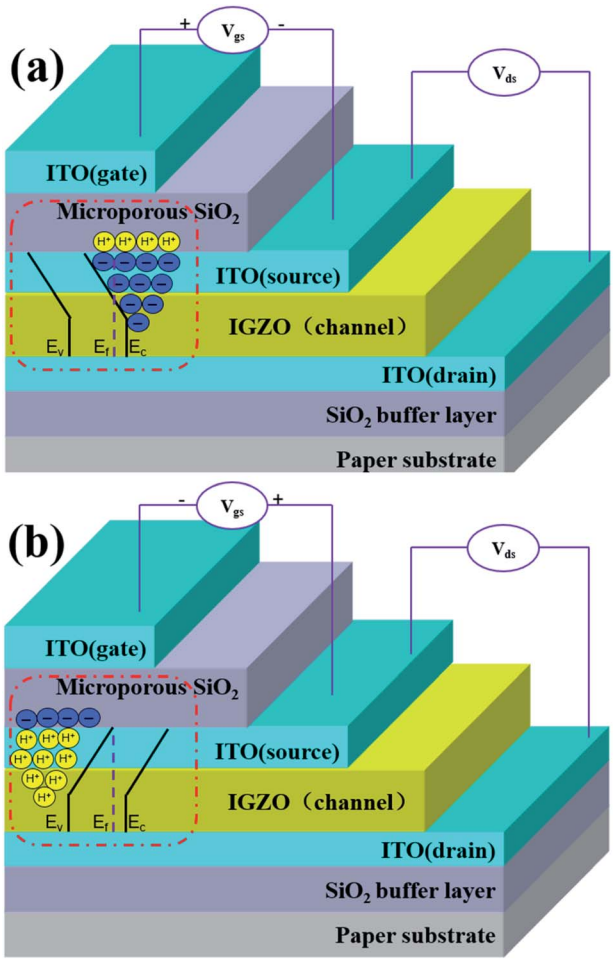

Fig. 1 Schematic diagram of flexible EDL vertical IGZO channel TFT with a top gate. (a) Red box: band diagram for the device biased with a positive gate voltage (V_{gs} > 0 V). (b) Red box: band diagram for the device biased with a positive gate voltage (V_{gs} < 0 V).

contacting, the conduction band and the valence band of ITO source and IGZO channel are horizontally distributed, the Fermi levels (E_f) are within the conduction band and band gap respectively. After contacting, the system will achieve a uniform E_f. Finally, the energy bands in the surface of vertical IGZO channel bending downwards because of the build-in electric field induced by the free electrons inject from the source to the channel.[8] When a positive V_{gs} is applied, high-density electrons will be induced and the surface energy bands bend downwards, as shown in the red box of Fig. 1(a), in this case, our vertical IGZO channel TFTs are turned on with a large on-state current. If a negative V_{gs} is applied to the gate electrode, the electrons in the ITO source and IGZO channel will be depleted, and the surface energy bands bend upwards, in this case, the device would be turned off, as shown in the red box of Fig. 1(b). The surface roughness of paper substrate can be improved by the SiO_2 buffer layer, the smooth surface and interface can improve the electrical performance of paper TFTs, which has been proved in our previous work.[9]

Fig. 2(a) shows the schematic diagram of EDL formation and low-voltage operation mechanism of the flexible EDL vertical IGZO channel TFTs with a top gate. In general, during the PECVD process, the hydrogen dissociated from SiH_4 in the plasma can enter the microporous SiO_2 dielectric, which can induce some mobile protons in SiO_2 layer as reported in the literature.[10] However, bare proton should not exist in SiO_2. What is most often referred to as the "proton" is almost certainly associated with a bridging oxygen atom to form a three coordinate oxygen centre (Si–OH^+–Si).[11] The schematic diagram of the working mechanism for the EDL TFTs is shown in Fig. 2(a), which can be described as follows. When a negative gate voltage is applied to the gate electrode, protons will move to the gate electrode/SiO_2-dielectric interface and the device is turned off. When a positive gate voltage is applied, protons move to a thin boundary layer at the SiO_2-dielectric/ITO source interface, and the positive charge induces an image charge and opposite sign in the ITO source layer, which is similar to the case of the EDL formation in organic transistors gated by ionic liquids or solid state electrolytes. This large EDL gate capacitance of 3.8 μF cm^{-2} results in a very low operating voltage of 1.0 V. The capacitance of the microporous SiO_2 was characterized by the capacitance–frequency (*C–f*) measurement using an Agilent 4294A precision impedance analyzer, as shown in Fig. 2(b). Remarkably, the *C–f* characteristics shows that the capacitance of the microporous SiO_2 dielectric deposited by PECVD at room temperature reaches a maximum of 3.8 μF cm^{-2} at 40 Hz and

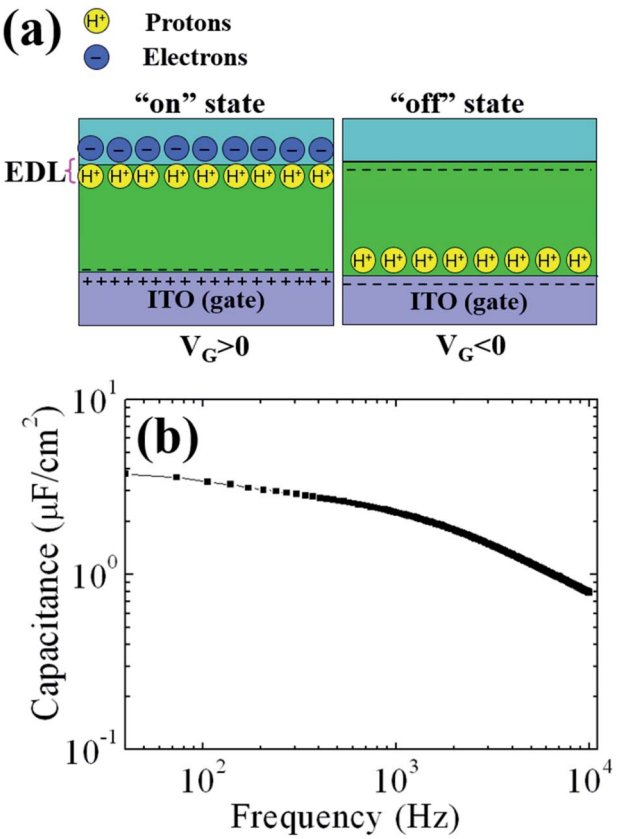

Fig. 2 (a) Schematic diagram of EDL formed in the vertical IGZO channel TFTs gated by microporous SiO_2. (b) The *C–f* characteristics for microporous-SiO_2 dielectric.

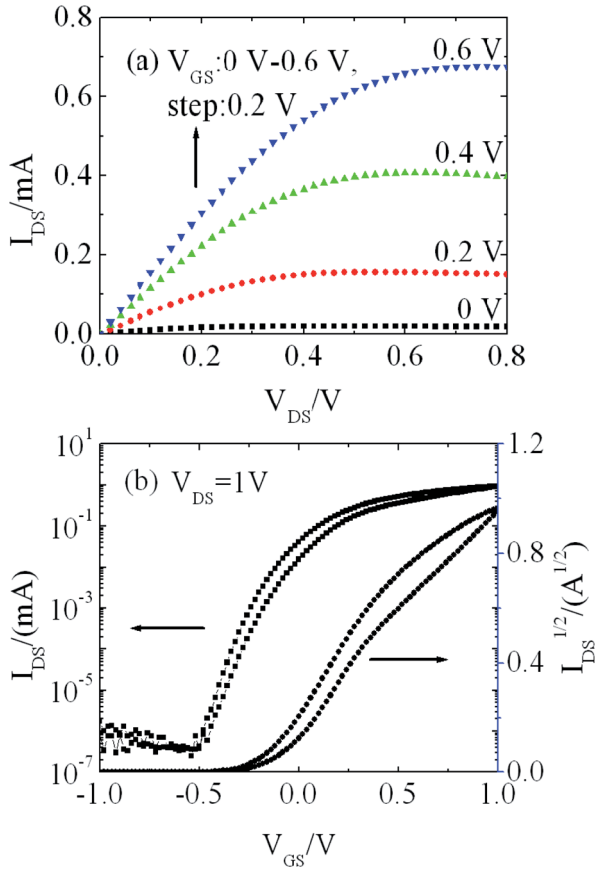

Fig. 3 (a) Typical output characteristics and (b) transfer characteristics of flexible EDL vertical IGZO channel TFTs with a top gate.

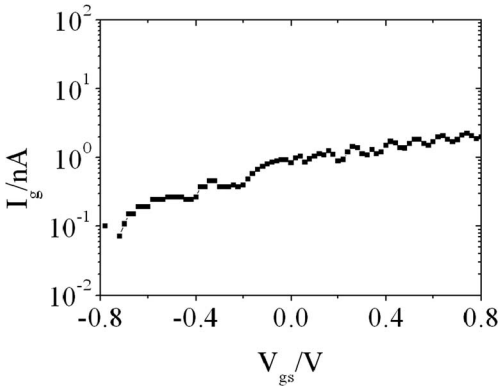

Fig. 4 Gate leakage current (I_g–V_{gs}) curve of the measured TFT.

down to 0.79 μF cm^{-2} at 10^4 Hz although the thickness of this microporous-SiO_2 is 4.0 μm. The relationship between the microporous SiO_2 capacitance and frequency is consistent with ion gel dielectrics.[12] The proton mobility in this 4.0 μm microporous SiO_2 limits the switching speed of TFTs, so the frequency dependence of this microporous SiO_2 capacitance is strong, which requires the migration of protons to form the EDL. The huge capacitance at low frequencies was mainly profited from the response of the EDL at the microporous SiO_2/ITO interface.

Table 1 Comparison of the electrical performance of such vertical channel TFTs with other works

	Operating voltage (V)	I_{on}/I_{off}	SS (mV per decade)	V_{th} (V)	Substrate
This work	1	1.2×10^6	80	−0.1	Paper
Ref. 14	15	3.39×10^7	210	—	Silicon wafer
Ref. 15	20	5.16×10^5	340	1.52	CPI on glass
Ref. 16	16	10^5	320	0.85	Glass

Fig. 3(a) shows the typical output characteristics (V_{ds}–I_{ds}) for flexible EDL vertical IGZO channel TFTs with a top gate. The V_{gs} was varied from 0 to 0.6 V in 0.2 V steps. The device operated in n-type field-effect transistor behaviors with a depletion mode because an obvious drain current was measured when $V_{gs} = 0$ V. A high saturation current of 0.67 mA was obtained under the bias conditions of $V_{ds} = 0.8$ V and $V_{gs} = 0.6$ V. The hard saturation reveals that the Fermi level in the channel is effectively controlled by the gate and drain voltages. The V_{ds}–I_{ds} curves did not show any evidence of current crowding at low V_{ds}, which indicates good ohmic contact between ITO source/drain electrodes and vertical IGZO channel. The corresponding transfer characteristics at fixed $V_{ds} = 1.0$ V are shown in Fig. 3(b). The subthreshold gate voltage swing $S = dV_{gs}/d(\log I_{ds})$, defined as the voltage required to increase the drain current by a factor of 10. The smaller the S, the easier it is to switch the transistor to an off state. For the as-fabricated TFT, the subthreshold slope S is estimated to be 80 mV per decade. The current on/off ratio is calculated to be about 1.2×10^6 with a low off current of 0.76 nA. The high output current (~1 mA) at less than 1.0 V for this device is remarkably attractive for devices needing high drive current at low voltage, such as organic light-emitting diodes.[13] Note that negligibly small hysteresis (~50 mV) in the transfer characteristic when the gate voltage sweeping from −1.0 V to +1.0 V and back. Such small hysteresis is mainly due to the mobile protons in the microporous SiO_2 dielectric. According to the equation of $N = \Delta V_{th} C_{OX}/e$, where ΔV_{th} is the threshold voltage shift between the dual sweeping of transfer curve, the C_{OX} is the capacitance per unit area, the proton density is calculated to be 1.2×10^{12} cm^{-2}.

The gate leakage current (I_g) of the microporous SiO_2 gate dielectric deposited by PECVD at room temperature is shown in Fig. 4. Leakage current is about 1.0 nA under the bias of 0.8 V, which is acceptable for our vertical IGZO channel TFTs operation. This small leakage current is likely due to the electrochemical silence and the small ionic current in microporous SiO_2. Despite the porosity in gate dielectric, the leakage current is six orders of magnitude smaller than the channel current, which assures the field-effect performance will not be affected by the leakage.

The comparison of electrical performance of such vertical channel TFTs with other works is shown in Table 1. The electrical performance of such vertical channel paper TFTs is much better than that of other works. The operating voltage of such vertical channel paper TFT is much lower than other works with smaller SS.

Conclusions

In conclusion, huge EDL capacitance was measured in microporous SiO_2-based solid-electrolyte deposited by PECVD method at room temperature. Flexible vertical IGZO channel TFTs with a top gate gated by such EDL dielectric operate in an n-type depletion mode with a low operation voltage of 1.0 V. The threshold voltage, drain current on/off ratio and subthreshold swing are estimated to be -0.1 V, 1.2×10^6 and 80 mV per decade, respectively. The combination of low voltage and room-temperature processing demonstrate that flexible EDL vertical IGZO channel TFTs with a top gate are very promising for low power portable flexible electronics.

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Author contributions

LHL and WD performed the experiments and drafted the manuscript with the help of YYT, XY, JLZ, YKW, SZZ, SYD, HTG, WCZ and DST. All authors read and approved the final manuscript.

Conflicts of interest

There are no conflicts to declare.

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