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# Fabrication of ring oscillators using organic molecules of phenacene and perylenedicarboximide

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Organic field-effect transistors (FETs) can be applied to radio-frequency identification tags (RFIDs) and active-matrix flat-panel displays. For RFID application, a cardinal functional block is a ring oscillator using an odd number of inverters to convert DC voltage to AC. Herein, we report the properties of two ring oscillators, one formed with [6]phenacene for a p-channel FET and *N,N'*-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) for an n-channel FET, and one formed with 3,10-ditetradecylpicene ((C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene) for a p-channel FET and PTCDI-C8 for an n-channel FET. The former ring oscillator provided a maximum oscillation frequency,  $f_{osc}$  of 26 Hz, and the latter a maximum  $f_{osc}$  of 21 Hz. The drain–drain voltage,  $V_{DD}$ , applied to these ring oscillators was 100 V. This may be the first step towards a future practical ring oscillator using phenacene molecules. The values of field-effect mobility,  $\mu$  in the p-channel [6]phenacene FET and n-channel PTCDI-C8 FET, which form the building blocks in the ring oscillator with an  $f_{osc}$  value of 26 Hz, are 1.19 and  $1.50 \times 10^{-1} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , respectively, while the values in the p-channel (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene FET and n-channel PTCDI-C8 FET, which form the ring oscillator with an  $f_{osc}$  of 21 Hz, are 1.85 and  $1.54 \times 10^{-1} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , respectively. The  $\mu$  values in the p-channel FETs are higher by one order of magnitude than those of the n-channel FET, which must be addressed to increase the value of  $f_{osc}$ . Finally, we fabricated a ring oscillator with ZrO<sub>2</sub> instead of parylene for the gate dielectric, which provided the low-voltage operation of the ring oscillator, in which [6]phenacene and PTCDI-C8 thin-film FETs were employed. The value of  $f_{osc}$  obtained in the ring oscillator was 24 Hz. In this ring oscillator, the  $V_{DD}$  value applied was limited to 20 V. The durability of the ring oscillators was also investigated, and the bias stress effect on the  $f_{osc}$  and the amplitude of the output voltage,  $V_{out}$  are discussed. This successful operation of ring oscillators represents an important step towards the realization of future practical integrated logic gate circuits using phenacene molecules.

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## 1. Introduction

Organic field-effect transistors (FETs) have been studied extensively during the past two decades to incorporate the advantages of organic materials, such as light weight, shock resistance, flexibility, large area coverage, relatively low toxicity, and ease of material design through knowledge of organic chemistry. Many chemists, physicists, and materials scientists have devoted significant effort to improving the transistor performance of

organic FETs. Most of the advantages described above for organic FETs originate from the weak interactions between organic molecules, *i.e.*, van der Waals force. However, the values of field-effect mobility,  $\mu$ , in organic FETs have been relatively low in comparison with those of inorganic FETs, the interaction of which is attributed to covalent bonds between atoms. Organic FETs exhibiting high  $\mu$  values have been pursued by seeking new organic molecules suitable for FET devices. The first promising molecule for FET devices was pentacene, whose  $\mu$  value in thin-film FETs was  $1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .<sup>1</sup> Pentacene FETs made p-channel operation possible. Meanwhile, the C<sub>60</sub> molecule had been found to be a good material for n-channel FETs. However, its  $\mu$  value was  $0.08 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ,<sup>2</sup> which was much smaller than those of p-channel FETs. The  $\mu$  value of C<sub>60</sub> thin film FETs reaches  $\sim 1.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ,<sup>3,4</sup> but in general an n-channel organic FET's  $\mu$  value is still lower than that of a p-channel organic FET. This is because electrons are easily captured by OH groups formed on gate dielectrics.

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The  $\mu$  value has rapidly increased through the application of various organic materials in FETs, especially during the past two decades. Various materials have garnered significant attention owing to the high  $\mu$  value observed. For instance, an FET device with a single crystal of rubrene has attracted interest from researchers in this community owing to its excellent p-channel FET properties, with a  $\mu$  value as high as  $40 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which was recorded in four-terminal measurements.<sup>5</sup> Promising materials recently found for FET devices are dioctylbenzothienobenzothiophene (C8-BTBT) ( $\mu \sim 6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ )<sup>6</sup> and bis(benzothieno)naphthalene (BBTN) ( $\mu = 15.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ).<sup>7</sup> Currently, the  $\mu$  value of a C8-BTBT thin-film FET has reached  $43 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .<sup>8</sup> Furthermore, we have been reporting the good FET performance of picene and its derivatives since 2008.<sup>9–18</sup> The picene molecule possesses a W-shaped benzene network, which is generally called “phenacene”. A phenacene molecule with five benzene rings is known as a picene. A picene FET device demonstrated typical p-channel normally-off FET characteristics with a  $\mu$  value of  $10^{-1}$  to  $3.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .<sup>9–18</sup> Various characteristics have been clarified in picene thin-film and single-crystal FETs, and their high performance and functionality have been demonstrated.<sup>9–18</sup>

Moreover, thin-film and single-crystal FETs have been fabricated using more extended phenacene molecules than picene.<sup>19–31</sup> Among them, the  $\mu$  value of a [6]phenacene thin-film FET reached  $7.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ,<sup>21</sup> which is one of the highest  $\mu$  values reported for organic thin-film FETs. A  $\mu$  value as high as  $18 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  has been recorded for [9]phenacene single-crystal FETs with a  $\text{ZrO}_2$  gate dielectric.<sup>28</sup> A thin-film FET using alkyl-substituted picene (3,10-ditetradecylpicene:  $(\text{C}_{14}\text{H}_{29})_2$ -picene) provided a  $\mu$  value as high as  $20.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ,<sup>25</sup> which was one of the best  $\mu$  values recorded in a two-terminal mode. These values are comparable to that of rubrene single-crystal FETs measured in a two-terminal mode.<sup>32</sup> Therefore, phenacene molecules are promising materials for high-performance FET devices. In addition, the stability of

phenacene molecules in atmospheric conditions is very promising for their future utility in FETs. Their stability originates from their armchair-shaped molecular structure.

Next, as current research results are insufficient, we must prove the potential utility of phenacene FETs in complementary metal-oxide-semiconductor (CMOS) logic integrated circuits. The simplest way to demonstrate the effectiveness of phenacene FETs in CMOS logic circuits is to fabricate a ring oscillator composed solely of an odd number of inverters. Ring oscillators using phenacene FETs have seldom been fabricated, and only one trial has been reported, which showed poor operation (oscillation frequency,  $f_{\text{osc}}$  of 1 Hz).<sup>33</sup> Therefore, research on phenacene molecules in integrated logic gate circuits (or electronic devices) such as ring oscillators must involve using deep insights into the physical chemistry of networks of fused benzene molecules, including the abundant FET data that has accumulated thus far.<sup>9–31</sup> In addition, the use of phenacene molecules in a ring oscillator may open an avenue for the stable operation of organic electronic devices because of their stability in air, as mentioned above.

In this study, we fabricated a ring oscillator comprising five CMOS inverters using two phenacene molecules, [6]phenacene and  $(\text{C}_{14}\text{H}_{29})_2$ -picene, which demonstrated excellent p-channel FET properties.<sup>19,21,25</sup> An  $N,N'$ -dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) molecule was used as an n-channel FET in a CMOS inverter. Three types of ring oscillators were fabricated using the above molecules, and low-voltage operation was realized using  $\text{ZrO}_2$  instead of a parylene gate dielectric. An  $f_{\text{osc}}$  value of 26 Hz was recorded in the ring oscillator using [6]phenacene and PTCDI-C8 FETs with parylene. This study represents an important step toward practical integrated logic gate circuits using phenacene molecules.

## 2. Experimental

An  $\text{SiO}_2/\text{Si}$  substrate was employed to prepare the ring oscillator. Before the fabrication of the FET device, the  $\text{SiO}_2/\text{Si}$

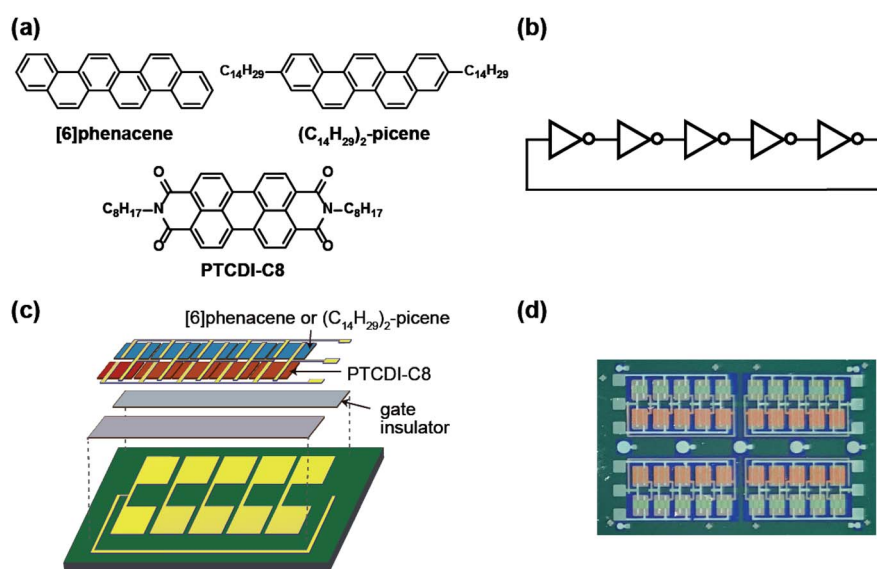


Fig. 1 (a) Molecular structures of [6]phenacene,  $(\text{C}_{14}\text{H}_{29})_2$ -picene, and PTCDI-C8. (b) Equivalent circuit of ring oscillator. (c) Protocol for fabrication of the ring oscillator employed in this study. (d) Photograph of the ring oscillator fabricated in this study. Four sets of ring oscillators were formed.



substrate was cleaned using the procedure described elsewhere.<sup>30</sup> The structures of the organic molecules employed for the ring oscillators, [6]phenacene, (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene, and PTCDI-C8, are shown in Fig. 1(a). The equivalent circuit of the five-step ring oscillators is shown in Fig. 1(b). The ring oscillators were fabricated according to the procedure shown in Fig. 1(c).

First, the electrodes were prepared on the SiO<sub>2</sub>/Si substrate, which become the gate electrodes for operating the FETs constituting each inverter. Next, a 600 nm-thick parylene or 320 nm-thick ZrO<sub>2</sub> gate dielectric was formed on the electrodes. The parylene thin film was prepared according to the procedure described elsewhere,<sup>30</sup> and the ZrO<sub>2</sub> thin film was prepared by electron beam evaporation, as described previously.<sup>30</sup> The gate dielectric was not formed in the central area to establish contacts between the output and input electrodes in each inverter. Subsequently, active layers were prepared by the thermal deposition of organic materials under a vacuum of 10<sup>-7</sup> Torr for p-channel and n-channel FET operations; either [6]phenacene or (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene was used for the p-channel active layer, while PTCDI-C8 was used for the n-channel active layer. The thickness of the active layer was 60 nm. Finally, the top electrodes were fabricated for voltage application (V<sub>DD</sub>), ground (GND), and detection of output voltage (V<sub>out</sub>). All electrodes were formed by the thermal deposition of gold (Au) under a vacuum of 10<sup>-7</sup> Torr, and the Au layer was 100 nm thick for the gate electrodes, and 150 nm for the top electrodes. Also, 5 nm-thick chromium (Cr) was inserted between the gate electrode and SiO<sub>2</sub>/Si substrate to increase the adhesion, while a 3 nm-thick 7,7,8,8-teracyanoquinodimethane was inserted between the active layer and top electrodes to reduce the contact resistance. A photograph of the ring oscillator prepared is shown in Fig. 1(d). In this study, the ring oscillators were prepared with active layers using (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene and PTCDI-C8 FETs, as well as [6]phenacene and PTCDI-C8 FETs, where a parylene gate dielectric was used. Also, a ring oscillator was fabricated using [6]phenacene and PTCDI-C8 FETs, as well as a ZrO<sub>2</sub> gate dielectric to reduce the operation voltage.

The channel length (*L*) of the [6]phenacene and PTCDI-C8 FETs contained in the ring oscillator was 200 μm, while the values of channel width (*W*) were 200 μm for the [6]phenacene FET and 500 μm for the PTCDI-C8 FETs in this ring oscillator, where parylene was used for the gate dielectric. The *L* value of the (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene and PTCDI-C8 FETs in the ring oscillator was 300 μm, while the *W* values were 500 μm for the (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene FET and 1000 μm for the PTCDI-C8 FETs in the ring oscillator, where parylene was used for the gate dielectric. The *L* of the [6]phenacene and PTCDI-C8 FETs in the ring oscillator was 300 μm, while the values of *W* were 500 μm for the [6]phenacene FET and 1000 μm for the PTCDI-C8 FETs in this ring oscillator, where ZrO<sub>2</sub> was used for the gate dielectric.

The capacitance per area of the parylene gate dielectric, *C*<sub>0</sub>, was determined experimentally to be 4.57 nF cm<sup>-2</sup> in the ring oscillator composed of [6]phenacene/PTCDI-C8 FETs, and 6.15 nF cm<sup>-2</sup> in that composed of (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene/PTCDI-C8 FETs. The *C*<sub>0</sub> value for ZrO<sub>2</sub> was experimentally determined to be 30.9 nF cm<sup>-2</sup> in the ring oscillator composed of [6]phenacene/PTCDI-C8 FETs. These values were directly measured using the corresponding devices. The difference in *C*<sub>0</sub> of the parylene film described above may be due to some microscopic quality of the film because its thickness was fixed

at 600 nm. In fact, the FET parameters were precisely evaluated because the values of the real *C*<sub>0</sub> were employed.

The operating properties of each FET device and inverter constituting the ring oscillator were measured in two-terminal measurement mode at room temperature. The operating properties were recorded using an Agilent B1500A semiconductor parametric analyzer in an Ar-filled glove box (O<sub>2</sub> < 0.3 ppm, H<sub>2</sub>O < 3 ppm). The FET properties were analyzed with the following equation in the saturation regime:<sup>34</sup>

$$I_D = \frac{\mu WC_0}{2L}(V_G - V_{th})^2, \quad (1)$$

where *I*<sub>D</sub>, *V*<sub>G</sub>, and *V*<sub>th</sub> refer to the drain current, gate voltage, and threshold voltage, respectively. For the analysis of the p-channel operation, the absolute values of *I*<sub>D</sub>, *V*<sub>D</sub>, and *V*<sub>G</sub> were employed. The operating properties of the ring oscillator were measured using the equipment above. All measurements in this study were performed at room temperature in an Ar-filled glove box. The measurement modes of the FET properties, CMOS inverter, and ring oscillator are shown in Fig. 2, to facilitate understanding of the measurement methods employed in Sections 3.1–3.4. The measurement methods for transport and output characteristics of independent FETs (Fig. 3) are substantially the same as those shown in ref. <sup>30</sup> and <sup>33</sup>. The polarities of *V*<sub>D</sub> and *V*<sub>G</sub> are opposite to each other between p-channel and n-channel FETs.

## 3. Results and discussion

### 3.1. Characteristics of FET devices constituting a ring oscillator

The transfer and output curves of independent [6]phenacene, (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene and PTCDI-C8 thin-film FETs are shown in Fig. 3(a)–(c); 400 nm-thick SiO<sub>2</sub> was used for the gate dielectric. The transfer and output curves of both the [6]phenacene and (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene thin-film FETs showed p-channel properties, which are the same as in previous reports.<sup>19,21,25,30</sup> The values of *μ* and *V*<sub>th</sub> were 1.1 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and 26 V, for a [6]phenacene FET, and 4.0 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and 51 V for a (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene thin-film FET. On the other hand, the transfer and output curves of the PTCDI-C8 thin-film FETs showed n-channel properties, demonstrating the same behaviour as previous reports;<sup>30</sup> the values of *μ* and *V*<sub>th</sub> were 2.5 × 10<sup>-1</sup> cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and 44 V. Thus, these FETs displayed either p-channel or n-channel unipolar behaviour.

Fig. 4(a) and (b) show the transfer and output characteristics of the [6]phenacene thin-film FET, which constitutes the p-channel part of one CMOS inverter in the ring oscillator; the n-channel part of the inverter is a PTCDI-C8 FET. The ring oscillator comprises five inverters, in which a 600 nm-thick parylene layer was used for the gate dielectric. The ring oscillator provides an *f*<sub>osc</sub> value of 26 Hz, which will be described later. The measurement mode of the FET characteristics is illustrated in Fig. 2(a). As shown in Fig. 4(a) and (b), p-channel FET characteristics were observed for the [6]phenacene FET, and weak n-channel FET properties were observed as well, indicating ambipolar properties. The characteristics of the [6]phenacene thin-film FET were affected by the PTCDI-C8 thin-film FET, which typically exhibits n-channel FET



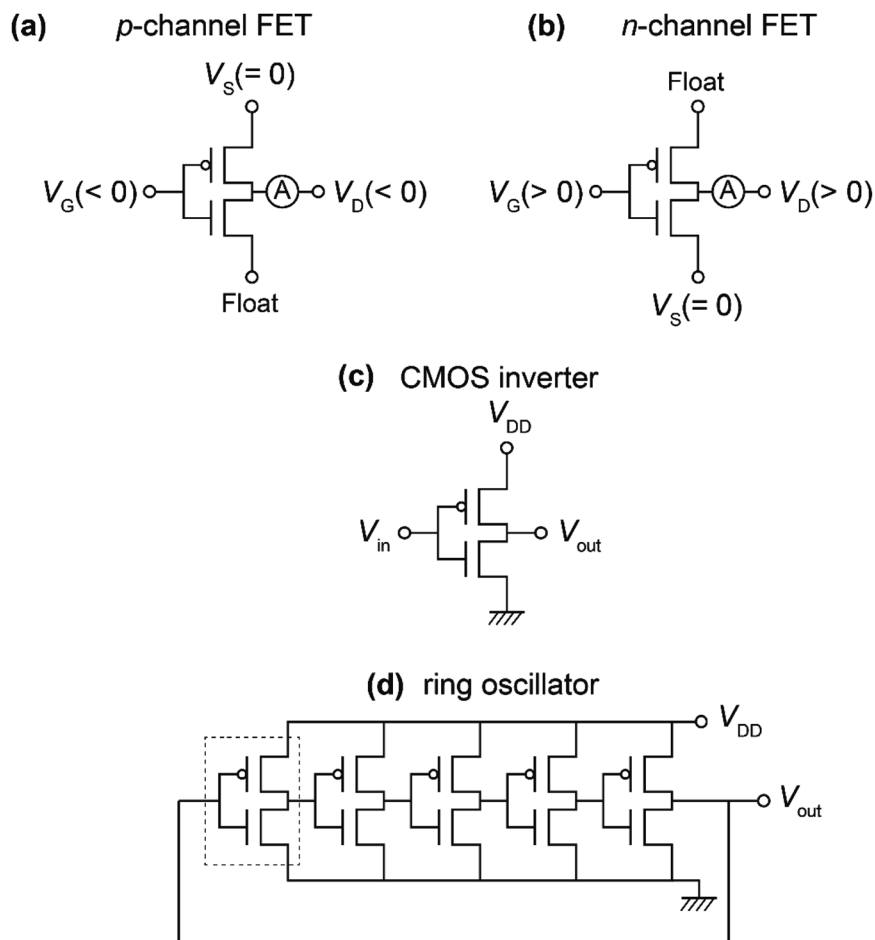


Fig. 2 Measurement modes of (a) p-channel FET properties, (b) n-channel FET properties, (c) CMOS inverter, and (d) ring oscillator. Devices discussed in Sections 3.1 to 3.4 are shown.

characteristics. Moreover, as shown in Fig. 4(c) and (d), the PTCDI-C8 thin-film FET showed not only n-channel FET characteristics, but also weak p-channel characteristics, *i.e.*, weak ambipolar characteristics were observed as well, as in the [6]phenacene FET; the measurement mode is shown in Fig. 2(b). Ambipolar characteristics were observed because another FET was operating below the absolute threshold voltage  $|V_{th}|$  for each FET.

Fig. 5(a) and (b) show the transfer and output characteristics of the  $(C_{14}H_{29})_2$ -picene thin-film FET, which constitutes the p-channel part of one CMOS inverter in the ring oscillator, providing an  $f_{osc}$  value of 21 Hz. PTCDI-C8 was employed as the active layer of the n-channel part. The measurement mode of the FET characteristics is illustrated in Fig. 2(a). As shown in Fig. 5(a) and (b), p-channel FET characteristics were observed for the  $(C_{14}H_{29})_2$ -picene FET, together with clear n-channel FET characteristics, indicating ambipolar properties. Therefore, the operation of the  $(C_{14}H_{29})_2$ -picene thin-film FET was affected by the PTCDI-C8 thin-film FET. As shown in Fig. 5(c) and (d), the PTCDI-C8 thin-film FET showed not only n-channel FET characteristics, but also p-channel characteristics; the measurement mode is shown in Fig. 2(b). Therefore, the ambipolar FET characteristics in the  $(C_{14}H_{29})_2$ -picene/PTCDI-C8 inverter are clearer than those discovered in the CMOS inverter with [6]phenacene and PTCDI-C8. In addition, a small hysteresis was observed in the forward and

reverse transfer curves (Fig. 4 and 5), which probably originates from the bias stress effect. Namely, the reverse curve degrades slightly owing to the formation of trap states induced by the bias voltage application. In particular, the characteristics due to the p-channel FET showed a larger hysteresis than those due to the n-channel FET, demonstrating a stronger bias stress effect. In addition, in the case of using an  $SiO_2$  gate dielectric treated with 1,1,1,3,3,3-hexamethyldisilazane (HMDS), the hysteresis of a picene thin-film FET may be larger than that of [6]phenacene and [7]phenacene thin-film FETs,<sup>9,19,20</sup> although this may be due to an extrinsic factor such as the difference in hydrophobicity of the surface of gate dielectric.

Previous studies indicated that [6]phenacene and  $(C_{14}H_{29})_2$ -picene thin-film FETs exhibited only p-channel FET characteristics when these devices were not electrically connected to PTCDI-C8 FETs.<sup>19,21,25,30</sup> Meanwhile, only n-channel FET characteristics should be observed in PTCDI-C8 thin-film FET devices separated electrically from a p-channel FET, as reported previously.<sup>30,35</sup>

The FET parameters of the [6]phenacene and PTCDI-C8 thin-film FETs in the inverters constituting the ring oscillator ( $f_{osc} = 26$  Hz) fabricated in this study are listed in Table 1. The average values of  $\mu$  and  $V_{th}$  ( $\langle\mu\rangle$  and  $\langle V_{th}\rangle$ ) were  $8(4) \times 10^{-1} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $-2(3) \times 10 \text{ V}$  for the [6]phenacene thin-film FET, respectively. Because of the ambipolar FET properties, the  $\langle\mu\rangle$  and  $\langle V_{th}\rangle$  were a little subpar, *i.e.*, low  $\mu$  and high  $\langle|V_{th}|\rangle$  were





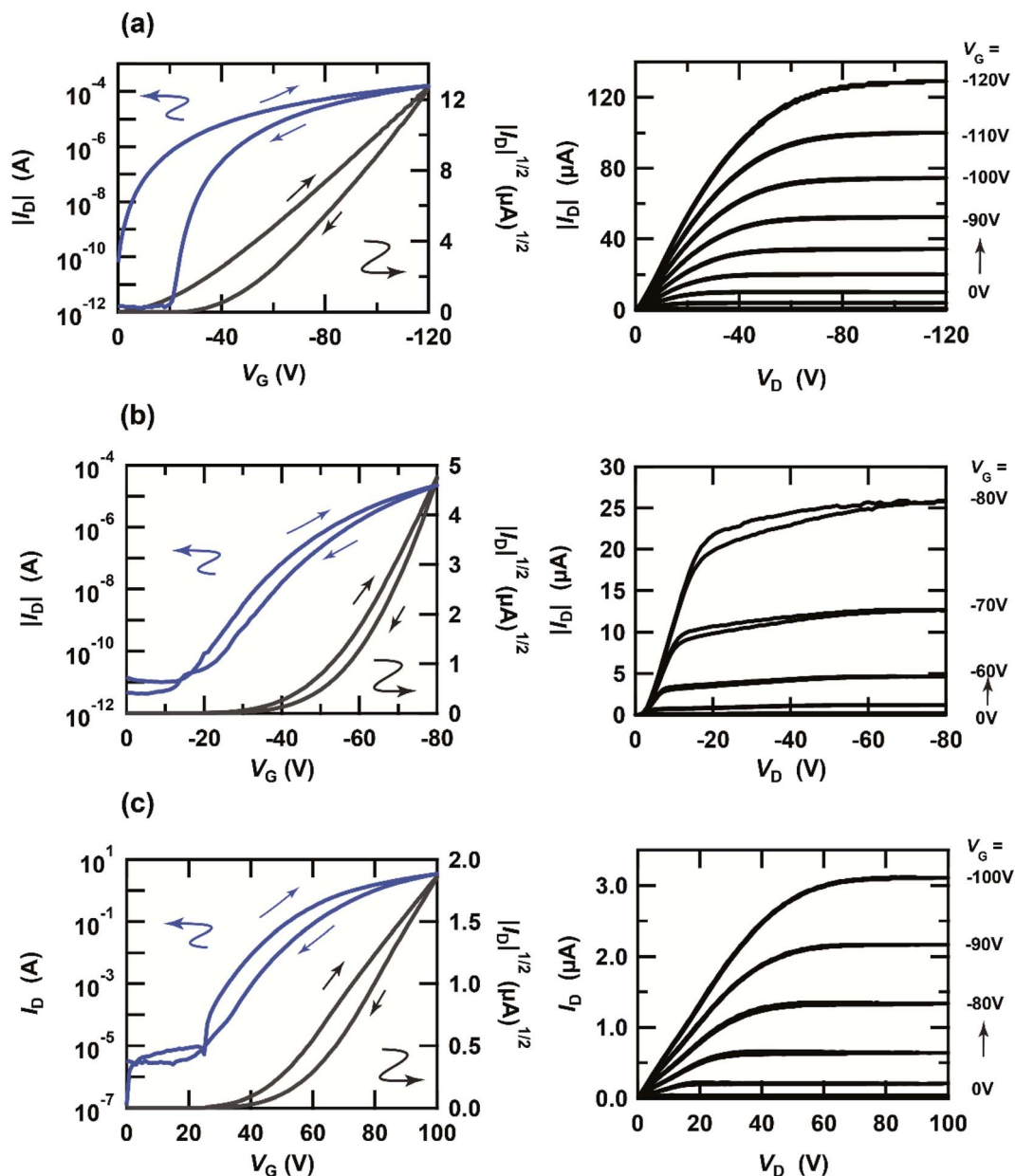


Fig. 3 Transfer (left) and output (right) characteristics of thin-film FETs with (a) [6]phenacene, (b)  $C_{14}H_{29}$ -picene and (c) PTCDI-C8. The device structure is bottom-gate top-contact type, and 300 nm-thick  $SiO_2$  was used for the gate dielectric. Two-terminal mode was used for the measurement of FET properties.

obtained, in comparison with those recorded for the normal [6] phenacene thin-film FET without electrical series connection with an n-channel FET device.<sup>19,21</sup> In particular, the average on-off ratio ( $\langle \text{on-off ratio} \rangle$ ) was exactly low, as shown in Table 1.

In addition, studies on overestimation of the  $\mu$  value have recently been reported.<sup>36,37</sup> One of the studies recommended showing the measurement reliability factor ( $r_{\text{sat}}$ ) for the evaluated mobility values.<sup>37</sup> The values of  $r_{\text{sat}}$  for [6]phenacene and  $(C_{14}H_{29})_2$ -picene thin-film FETs with  $SiO_2$  gate dielectrics showing high  $\mu$  values of 7.4 and 3.9  $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ , which were reported previously,<sup>21,25</sup> were found to be 9.3% and 24% in this study, respectively, indicating effective mobilities,  $\mu_{\text{eff}} (=r_{\text{sat}} \times \mu)$ , of 0.69 and 0.94  $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ . On the other hand, the value of  $r_{\text{sat}}$  was 27% for a  $(C_{14}H_{29})_2$ -picene thin-film FET with

$ZrO_2$  gate dielectric showing the  $\mu$  value of 5.1  $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ ,<sup>30</sup> demonstrating an effective mobility value of 1.3  $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ . Here, the  $r_{\text{sat}}$  value was determined using the formula reported in ref. <sup>37</sup>. In this study, no further investigation of the effective mobility was made for the FETs constituting the ring oscillator. Therefore, in this paper, the FET properties will be discussed based on the value of  $\mu$  (not effective mobility), but it may be necessary to consider the effective mobility if high FET performance is reported.

The high subthreshold slope ( $\langle S \rangle$ ) was due to the ambipolar properties. The values of  $\langle \mu \rangle$  and  $\langle V_{\text{th}} \rangle$  were  $2.0(4) \times 10^{-1} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$  and 3(7) V for the PTCDI-C8 thin-film FET; the  $\mu$  value was much lower than that in the FET using a PTCDI-C8 thin film formed on pentacene, as reported recently.<sup>35</sup> The values of  $\langle \text{on-off ratio} \rangle$  and  $\langle S \rangle$



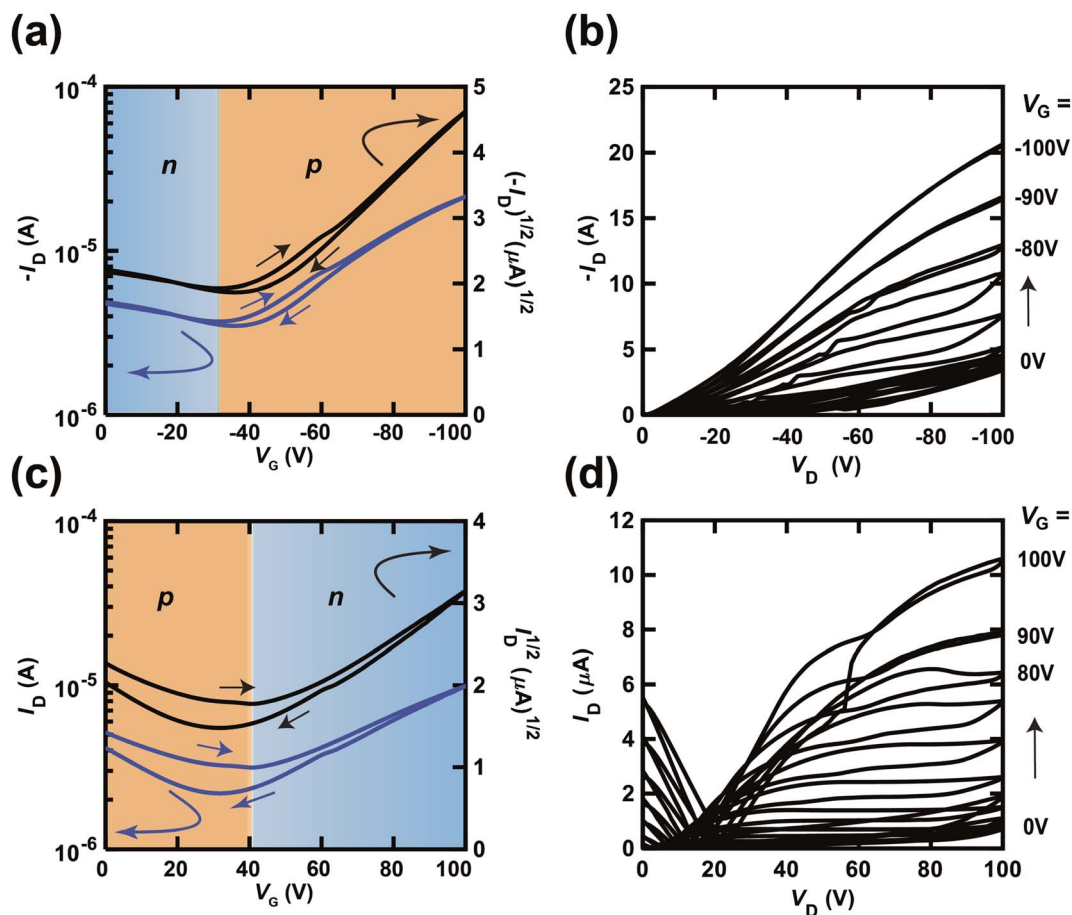


Fig. 4 (a) Transfer and (b) output characteristics of a [6]phenacene thin-film FET, which constitutes the p-channel part of the CMOS inverter in the ring oscillator ( $f_{\text{osc}} = 26$  Hz at  $V_{\text{DD}} = 100$  V). (c) Transfer and (d) output characteristics of a PTCDI-C8 thin-film FET, which constitutes the n-channel part of the CMOS inverter in the ring oscillator ( $f_{\text{osc}} = 26$  Hz at  $V_{\text{DD}} = 100$  V). In (a) and (c), the p-channel and n-channel parts are shown by orange and blue backgrounds, respectively. The gate dielectric was 600 nm-thick parylene. The FETs employed refer to device 3 (#3) in Table 1.

were subpar because of the ambipolar properties observed in a series connection of CMOS inverters composed of p-channel and n-channel FETs. To summarize, the relatively low FET properties recorded in this study were not due to the intrinsic nature of the materials employed, but the electrical series connections of the inverters.

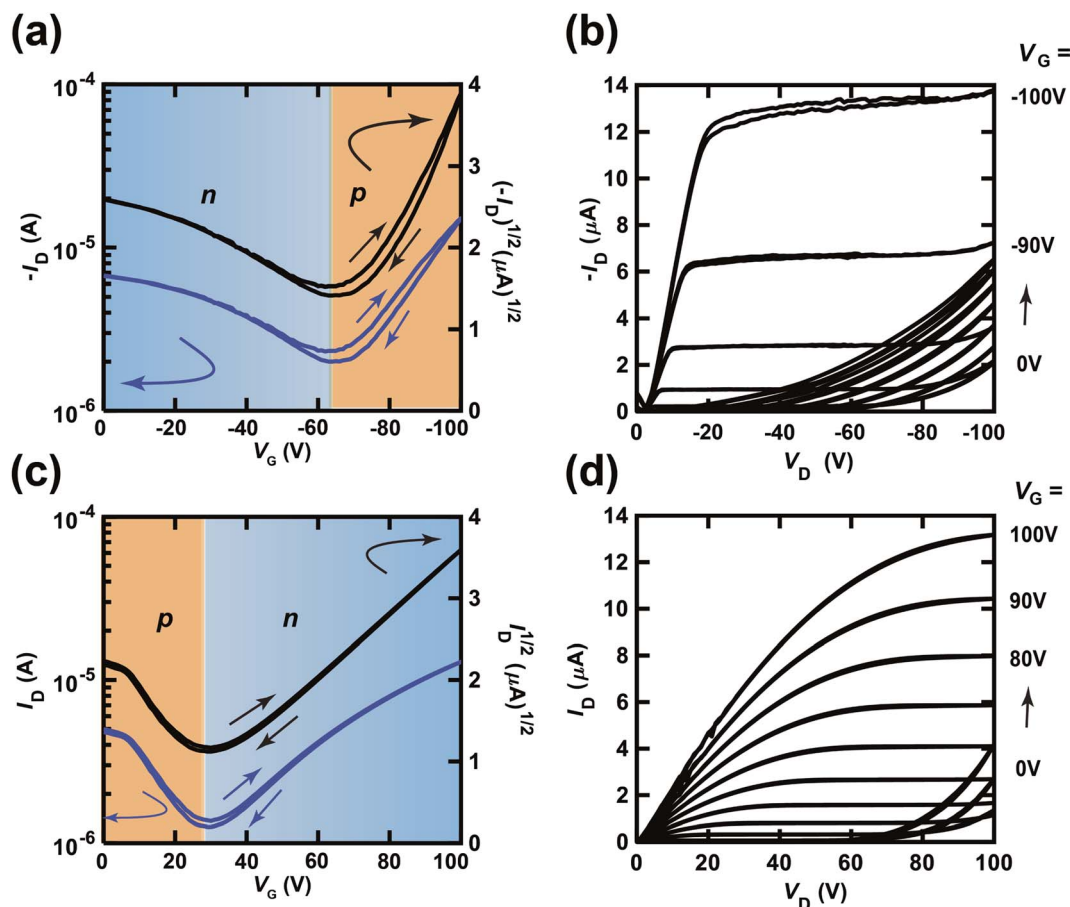
All FET parameters in the  $(\text{C}_{14}\text{H}_{29})_2$ -picene thin-film and PTCDI-C8 thin-film FETs in the CMOS inverters constituting the ring oscillator ( $f_{\text{osc}} = 21$  Hz) fabricated in this study are listed in Table 2. The average values of  $\mu$  and  $V_{\text{th}}$  ( $\langle\mu\rangle$  and  $\langle V_{\text{th}}\rangle$ ) were  $1.4(7) \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $-5.9(9) \times 10 \text{ V}$  for the  $(\text{C}_{14}\text{H}_{29})_2$ -picene thin-film FET. The  $\langle\mu\rangle$  value for the normal  $(\text{C}_{14}\text{H}_{29})_2$ -picene thin-film FET recorded previously by our group was beyond  $5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .<sup>25</sup> The low  $\langle\text{on-off ratio}\rangle$  and high  $\langle S\rangle$  were due to the ambipolar properties observed in the series connection of CMOS inverters. The values of  $\langle\mu\rangle$  and  $\langle V_{\text{th}}\rangle$  were respectively  $1.3(5) \times 10^{-1} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $9.2(6) \text{ V}$  for the PTCDI-C8 thin-film FET. Similarly, the low value of  $\langle\text{on-off ratio}\rangle$  and high  $\langle S\rangle$  were likely due to the effects of the ambipolar properties observed in the series connection of CMOS inverters.

### 3.2. Characteristics of CMOS inverters in the ring oscillators

Fig. 6(a) shows plots of  $V_{\text{out}}-V_{\text{in}}$  (inverter characteristics) and  $|dV_{\text{out}}/dV_{\text{in}}|-V_{\text{in}}$  (gain plot) for one CMOS inverter based on [6]

phenacene and PTCDI-C8 thin-film FETs, which form a ring oscillator with an  $f_{\text{osc}}$  of 26 Hz. The inverter contains the [6] phenacene and PTCDI-C8 thin-film FETs described in Section 3.1. Clear inverter properties were observed in the plot shown in Fig. 6(a); the method used to measure the inverter properties is shown in Fig. 2(c). The  $V_{\text{DD}}$  was 100 V. As shown in Fig. 6(a), the  $V_{\text{in}}$  (59.7 V for the forward measurement and 47.5 V for the reverse measurement) providing half the maximum value of  $V_{\text{out}}$  (called “logic threshold voltage ( $V_{\text{TC}}$ )”) deviates slightly from the ideal value of  $V_{\text{DD}}/2 = 50$  V. The gain plot of the CMOS inverter with [6]phenacene and PTCDI-C8 thin-film FETs is shown in Fig. 6(a), which was obtained from the first derivative of the  $V_{\text{out}}-V_{\text{in}}$  plot (Fig. 6(a)). The gain of the CMOS inverter above was evaluated to be 285.8 for the forward measurement and 145.3 for the reverse measurement, which is slightly lower than that ( $\sim 300$ ) of recent CMOS inverters formed on a plastic substrate using [6]phenacene and PTCDI-C8 thin-film FETs.<sup>30</sup> It is worth noting that the inverter properties were measured using a fabricated ring oscillator, *i.e.*, five inverters were connected in series (Fig. 2(d)). Therefore, these inverter properties cannot be compared directly with the previous inverter properties.





**Fig. 5** (a) Transfer and (b) output characteristics of a  $(C_{14}H_{29})_2$ -picene thin-film FET, which constitutes the p-channel part of the CMOS inverter in the ring oscillator ( $f_{osc} = 21$  Hz at  $V_{DD} = 100$  V). (c) Transfer and (d) output characteristics of a PTCDI-C8 thin-film FET, which constitutes the n-channel part of the CMOS inverter in the ring oscillator ( $f_{osc} = 21$  Hz at  $V_{DD} = 100$  V). In (a) and (c), the p-channel and n-channel parts are shown by orange and blue backgrounds, respectively. The gate dielectric was 600 nm-thick parylene. The FETs employed refer to device 1 (#1) in Table 2.

The  $V_{TC}$  value of the CMOS inverter circuit is given by the following equation:<sup>38</sup>

$$V_{TC} = \frac{V_{THn} + \sqrt{\frac{k_p}{k_n}} (V_{DD} + V_{THp})}{\left(1 + \sqrt{\frac{k_p}{k_n}}\right)}, \quad (2)$$

where  $k = \frac{\mu WC_0}{L}$ ;  $k_p$  and  $k_n$  refer to the  $k$  values for the p- and n-channel FETs;  $V_{THp}$  and  $V_{THn}$  refer to the  $V_{TH}$  values for the p- and n-channel FETs. By substituting the FET parameters obtained in Section 3.1 into eqn (2), we evaluated the  $V_{TC}$  for the

CMOS inverter above and obtained a value of 54.2 V. This  $V_{TC}$  value is consistent with the average ( $\langle V_{TC} \rangle = 53.6$  V) of the values observed in the forward and reverse measurements ( $V_{TC} = 59.7$  V and  $V_{TC} = 47.5$  V), which indicates the effectiveness of the above equation and the reliability of the FET parameters in Section 3.1. The values of gain and  $V_{TC}$  for all inverters constituting the ring oscillator are listed in Table 3; the plots shown in Fig. 6(a) were obtained using the inverter device (#3) in Table 3.

Fig. 6(b) shows plots of  $V_{out} - V_{in}$  and  $|dV_{out}/dV_{in}| - V_{in}$  for one CMOS inverter built with  $(C_{14}H_{29})_2$ -picene and PTCDI-C8 thin-film FETs, which created a ring oscillator with an  $f_{osc}$  of

**Table 1** FET parameters of [6]phenacene and PTCDI-C8 thin-film FETs built into ring oscillators

| [6]Phenacene |   |                     |                     |                    | PTCDI-C8 |   |              |                    |                    |
|--------------|---|---------------------|---------------------|--------------------|----------|---|--------------|--------------------|--------------------|
| Device       | M ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) | $V_{th}$ (V)        | On-off              | S (V per decade)   | Device   | M ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) | $V_{th}$ (V) | On-off             | S (V per decade)   |
| #1           | $8.1 \times 10^{-1}$                            | $-7.0 \times 10^1$  | $2.69 \times 10^3$  | $2.7 \times 10^1$  | #1       | $2.33 \times 10^{-1}$                           | 8.7          | $4.8 \times 10^1$  | $1.0 \times 10^1$  |
| #2           | $8.1 \times 10^{-1}$                            | $-3.1 \times 10^1$  | 2.71                | $8.2 \times 10^1$  | #2       | $1.69 \times 10^{-1}$                           | -1.5         | 3.2                | $9.7 \times 10^1$  |
| #3           | 1.19  | $-1.1 \times 10^1$  | 6.12                | $6.1 \times 10^1$  | #3       | $1.50 \times 10^{-1}$                           | -7.7         | 3.1                | $9.9 \times 10^1$  |
| #4           | $2.7 \times 10^{-1}$                            | $1.7 \times 10^1$   | 2.44                | $1.2 \times 10^2$  | #4       | $1.96 \times 10^{-1}$                           | 6.1          | 4.8                | $8.0 \times 10^1$  |
| #5           | 1.16  | $-1.4 \times 10^1$  | 5.71                | $5.9 \times 10^1$  | #5       | $2.27 \times 10^{-1}$                           | 9.9          | 4.7                | $8.0 \times 10^1$  |
| Average      | $8(4) \times 10^{-1}$                           | $-2(3) \times 10^1$ | $5(12) \times 10^2$ | $7(4) \times 10^1$ | Average  | $2.0(4) \times 10^{-1}$                         | 3(7)         | $1(2) \times 10^1$ | $8(3) \times 10^1$ |



Table 2 FET parameters of (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene and PTCDI-C8 thin-film FETs built into ring oscillators

| (C <sub>14</sub> H <sub>29</sub> ) <sub>2</sub> -Picene |  |                           |        |                          | PTCDI-C8 |  |                     |                          |                          |
|---|--|---------------------------|--------|--------------------------|----------|--|---------------------|--------------------------|--------------------------|
| Device  | M (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> ) | V <sub>th</sub> (V)       | On-off | S (V per decade)         | Device   | μ (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> ) | V <sub>th</sub> (V) | On-off                   | S (V per decade)         |
| #1  | 1.85   | -6.0 × 10 <sup>1</sup>    | 6.6    | 3.60 × 10 <sup>1</sup>   | #1       | 1.54 × 10 <sup>-1</sup>                              | 9.49                | 1.03 × 10 <sup>1</sup>   | 5.13 × 10 <sup>1</sup>   |
| #2  | 2.40 × 10 <sup>-1</sup>                              | -4.4 × 10 <sup>1</sup>    | 6.8    | 5.24 × 10 <sup>1</sup>   | #2       | 3.10 × 10 <sup>-2</sup>                              | 9.74                | 8.29                     | 4.92 × 10 <sup>1</sup>   |
| #3  | 1.73   | -6.3 × 10 <sup>1</sup>    | 9.8    | 2.99 × 10 <sup>1</sup>   | #3       | 1.53 × 10 <sup>-1</sup>                              | 8.51                | 1.82 × 10 <sup>1</sup>   | 5.08 × 10 <sup>1</sup>   |
| #4  | 1.90   | -6.4 × 10 <sup>1</sup>    | 7.0    | 3.37 × 10 <sup>1</sup>   | #4       | 1.53 × 10 <sup>-1</sup>                              | 9.39                | 1.21 × 10 <sup>1</sup>   | 5.00 × 10 <sup>1</sup>   |
| #5  | 1.19   | -6.6 × 10 <sup>1</sup>    | 5.4    | 3.13 × 10 <sup>1</sup>   | #5       | 1.52 × 10 <sup>-1</sup>                              | 8.60                | 1.30 × 10 <sup>1</sup>   | 4.66 × 10 <sup>1</sup>   |
| Average   | 1.4(7)   | -5.9(9) × 10 <sup>1</sup> | 7(2)   | 3.7(9) × 10 <sup>1</sup> | Average  | 1.3(5) × 10 <sup>-1</sup>                            | 9.2(6)              | 1.2(4) × 10 <sup>1</sup> | 5.0(2) × 10 <sup>1</sup> |

21 Hz. The inverter was composed of the (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene and PTCDI-C8 thin-film FETs evaluated in Section 3.1. Clear inverter properties were observed in the V<sub>out</sub>-V<sub>in</sub> plot shown in Fig. 6(b); the V<sub>DD</sub> was 100 V. As shown in Fig. 6(b), the observed value of V<sub>TC</sub> (38.9 V for the forward measurement and 33.9 V for the reverse measurement) deviated from the value of V<sub>DD</sub>/2 = 50 V. The gain plot obtained from the first derivative of the V<sub>out</sub>-V<sub>in</sub>

plot (Fig. 6(b)) for the CMOS inverter with (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene and PTCDI-C8 thin-film FETs is shown in Fig. 6(b). The gain of the above CMOS inverter was evaluated to be 61.8 for the forward measurement and 90.8 for the reverse measurement. As described above, the five inverters were connected in series in the measurement of the inverter properties, which may suppress the gain of each inverter. Using eqn (2), we evaluated

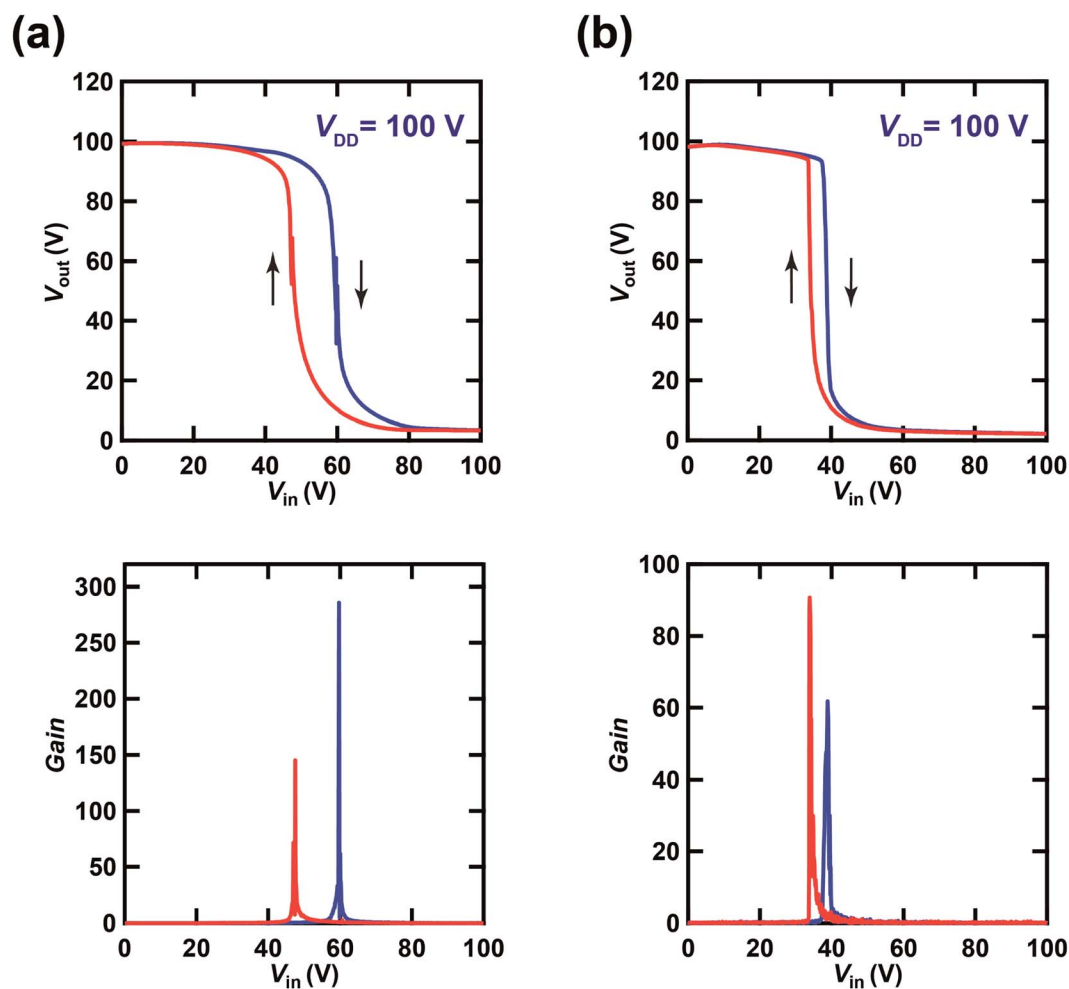


Fig. 6 Plots of V<sub>out</sub>-V<sub>in</sub> and dV<sub>out</sub>/dV<sub>in</sub>-V<sub>in</sub> in (a) a CMOS inverter composed of [6]phenacene and PTCDI-C8 FETs, which is a block of ring oscillators (f<sub>osc</sub> = 26 Hz at V<sub>DD</sub> = 100 V), and (b) a CMOS inverter composed of (C<sub>14</sub>H<sub>29</sub>)<sub>2</sub>-picene and PTCDI-C8 FETs FET, which is a block of ring oscillators (f<sub>osc</sub> = 21 Hz at V<sub>DD</sub> = 100 V). The gate dielectric was 600 nm-thick parylene. The blue and red curves refer to the plots recorded in forward and reverse measurement modes, respectively (see text). The inverter in (a) corresponds to Device 3 (#3) in Table 3, while the inverter in (b) corresponds to Device 1 (#1) in Table 4.





**Table 3** Values of  $V_{TC}$  and gain of inverters made of [6]phenacene/PTCDI-C8 FETs, and built into a ring oscillator

| Device  | Forward      |          | Reverse      |         |
|---------|--------------|----------|--------------|---------|
|         | $V_{TC}$ (V) | Gain     | $V_{TC}$ (V) | Gain    |
| #1      | 55.9         | 32.9     | 52.4         | 25.2    |
| #2      | 37.7         | 67.8     | 33.0         | 193.4   |
| #3      | 59.7         | 285.8    | 47.5         | 145.3   |
| #4      | 58.2         | 181.4    | 48.3         | 262.4   |
| #5      | 54.9         | 146.6    | 50.5         | 60.9    |
| Average | 53(9)        | 143(100) | 46(8)        | 140(97) |

the theoretical value of  $V_{TC}$  for the CMOS inverter and obtained a value of 31.2 V. This  $V_{TC}$  value is almost consistent with the  $\langle V_{TC} \rangle$  (=36.4 V) obtained from  $V_{TC} = 38.9$  V (forward measurement) and  $V_{TC} = 33.9$  V (reverse measurement), which also indicates the effectiveness of the above equation and the reliability of the FET parameters in Section 3.1. The values of gain and  $V_{TC}$  for all inverters constituting the ring oscillator are listed in Table 4; the plots shown in Fig. 6(b) are obtained using Inverter Device 1 (#1). We note that significant hysteresis in the  $V_{out}$ - $V_{in}$  plots (Fig. 6(a) and (b)) is observed owing to the bias stress effect found in p-channel FETs as described in Section 3.1. The bias stress effect is discussed later in detail.

### 3.3. Ring oscillators using CMOS inverters composed of phenacene and PTCDI-C8 FETs

Fig. 7(a) shows the  $V_{out}$ - $t$  plot for the ring oscillator comprising five CMOS inverters. Each inverter was fabricated using a [6]phenacene thin-film FET for p-channel operation and a PTCDI-C8 thin-film FET for n-channel operation. Furthermore, a 600 nm-thick parylene film was used for the gate dielectric in the ring oscillator. As shown in Fig. 7(a), the value of the operation frequency,  $f_{osc}$  was 26 Hz when  $V_{DD}$  was 100 V. This is the first time acceptable operation of a ring oscillator using phenacene molecules, although the  $f_{osc}$  value of 1 Hz has been recorded previously in a ring oscillator using [6]phenacene and PTCDI-C8.<sup>33</sup>

Fig. 7(b) shows the  $V_{out}$ - $t$  plot for a ring oscillator comprising five CMOS inverters; each inverter was fabricated using a  $(C_{14}H_{29})_2$ -picene thin-film FET for p-channel operation and a PTCDI-C8 thin-film FET for n-channel operation. Furthermore, a 600 nm-thick parylene film was used for the gate dielectric in this ring oscillator. As shown in Fig. 7(b), the value of  $f_{osc}$  was 21 Hz when a  $V_{DD}$  of 100 V was applied. Therefore, the clear operation of

**Table 4** Values of  $V_{TC}$  and gain of inverters made with  $(C_{14}H_{29})_2$ -picene/PTCDI-C8 FETs and built into a ring oscillator

| Device  | Forward      |       | Reverse      |         |
|---------|--------------|-------|--------------|---------|
|         | $V_{TC}$ (V) | Gain  | $V_{TC}$ (V) | Gain    |
| #1      | 38.9         | 61.8  | 33.9         | 90.8    |
| #2      | 38.8         | 54.1  | 33.5         | 108.7   |
| #3      | 41.1         | 50.9  | 33.8         | 159.6   |
| #4      | 38.6         | 56.5  | 33.5         | 281.3   |
| #5      | 36.6         | 47.1  | 30.9         | 125.5   |
| Average | 39(2)        | 54(6) | 33(1)        | 153(76) |

the ring oscillator was confirmed when using [6]phenacene/PTCDI-C8 FETs and  $(C_{14}H_{29})_2$ -picene/PTCDI-C8 FETs, indicating the possibility of using the above FETs in RFID devices.

We also attempted to fabricate a ring oscillator incorporating five inverters composed of [6]phenacene/PTCDI-C8 FETs with a  $ZrO_2$  gate dielectric to realize low-voltage operation. The  $V_{out}$ - $t$  plot of the ring oscillator is shown in Fig. 7(c). A  $V_{DD}$  of 20 V was applied to this ring oscillator, providing a 24 Hz oscillation. This device performance is comparable to those of the ring oscillators above using parylene gate dielectrics. Therefore, low-voltage operation was realized using a  $ZrO_2$  gate dielectric, as described below.

We changed the  $V_{DD}$  value applied to the ring oscillator to verify the operation properties. Fig. 8 shows the  $V_{out}$ - $t$  plots for the ring oscillator composed of five inverters using [6]phenacene and PTCDI-C8 FETs with the parylene gate dielectric measured at different  $V_{DD}$ . When  $V_{DD}$  was decreased from 120 to 40 V, the  $f_{osc}$  and the amplitude of  $V_{out}$  decreased gradually, so the  $f_{osc}$  was 28 Hz for  $V_{DD} = 120$  V, and 10 Hz for  $V_{DD} = 80$  V. Below  $V_{DD} = 40$  V, oscillations were not observed. Thus it was found that the threshold  $V_{DD}$  for oscillation was 40 V for this ring oscillator.

Fig. 9 shows the  $V_{out}$ - $t$  plots for the ring oscillator composed of five inverters using [6]phenacene and PTCDI-C8 FETs with  $ZrO_2$  gate dielectrics, as measured at different  $V_{DD}$ . When decreasing  $V_{DD}$  from 22 to 8 V, the  $f_{osc}$  decreased gradually. Specifically, the  $f_{osc}$  was 25 Hz for  $V_{DD} = 22$  V and 8.8 Hz for  $V_{DD} = 14$  V. Below  $V_{DD} = 8$  V, oscillations were not observed. Thus, the threshold  $V_{DD}$  for the oscillation of this ring oscillator was 8 V, showing the operation of a ring oscillator at a lower voltage than that (threshold  $V_{DD}$  of 40 V) of the previous ring oscillator (Fig. 8). Namely, the  $ZrO_2$  gate dielectric used in the ring oscillator resulted in low-voltage operation. In addition, as shown in Fig. 8, the amplitude of  $V_{out}$  increased when  $V_{DD}$  was decreased from 22 to 18 V and then decreased when  $V_{DD}$  was further decreased. The origin of the increase is still unclear.

The  $f_{osc}$  value of the ring oscillator obtained in this study is smaller than that (=200 kHz) of the ring oscillator composed of five CMOS inverters with pentacene/ $C_{60}$  FETs,<sup>39</sup> which is a small-sized device where  $L = 2$   $\mu$ m. The ring oscillator was fabricated by the mass-printed roll-to-roll method, where five unipolar inverters with a conjugated polymer, poly[[2,2'-bithiophene]-5,5'-diyl(9,9-dioctyl-9H-fluorene-2,7-diyl)] (F8T2), was utilized and provided an  $f_{osc}$  of 6 Hz; the  $L$  was 100  $\mu$ m, which was the same order as those ( $L = 200$  or 300  $\mu$ m) of the ring oscillators in this study.<sup>40</sup> The  $f_{osc}$  value was smaller than that of our ring oscillator ( $\sim 26$  Hz). It is shown in ref. <sup>41</sup> that  $f_{osc}$  is clearly correlated with  $L$ . A smaller  $L$  in the FET blocks in each inverter of the ring oscillator provides a higher  $f_{osc}$ . This result is explained by the theoretical model described below.<sup>33,38</sup>

The  $f_{osc}$  value is expressed as follows:

$$f_{osc} = \frac{1}{2n\langle\tau_p\rangle}, \quad (3)$$

where  $n$  refers to the number of inverters;  $\langle\tau_p\rangle$  is the average value of signal delay per stage,  $\tau_p$ , of the ring oscillator;

$\tau_p$  is expressed by

$$\tau_p = (\tau_{pLH} + \tau_{pHL})/2. \quad (4)$$



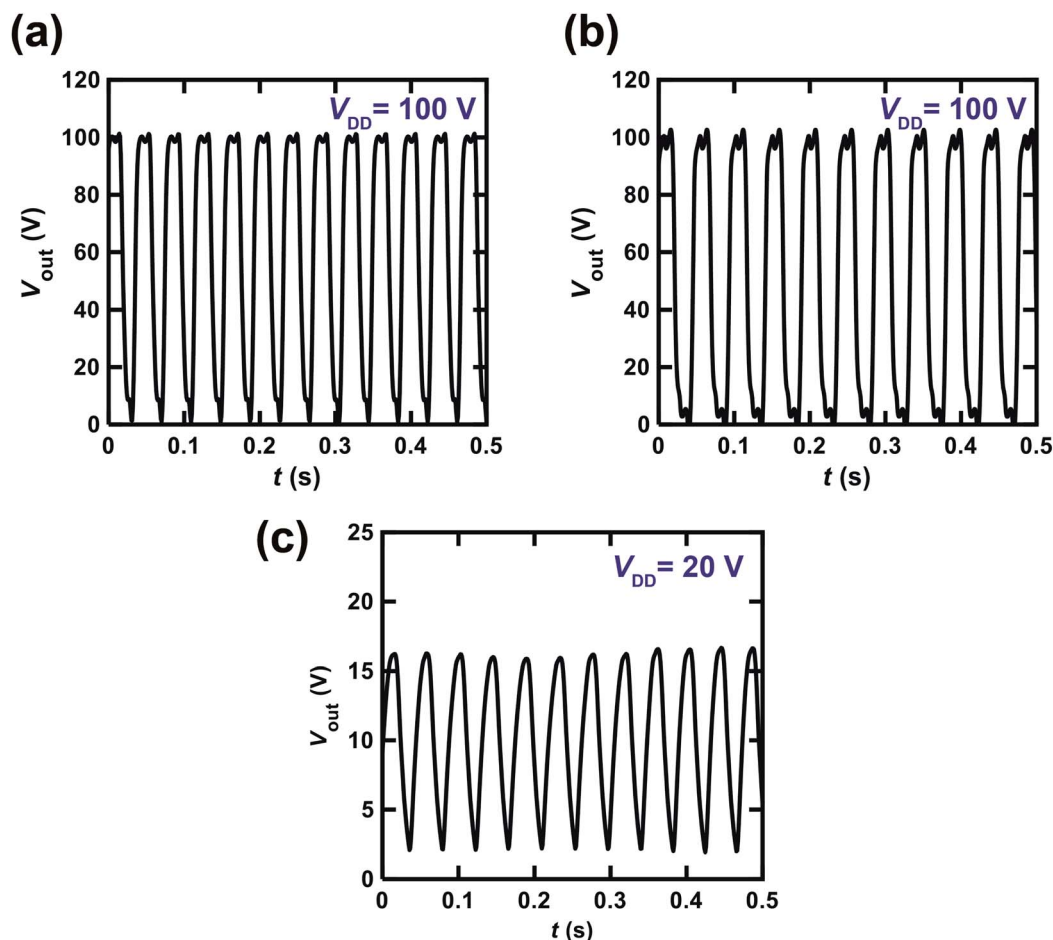


Fig. 7  $V_{\text{out}}-t$  plots of ring oscillators comprising five inverters, composed of (a) [6]phenacene and PTCDI-C8 thin-film FETs, and (b)  $(\text{C}_{14}\text{H}_{29})_2$ -picene and PTCDI-C8 thin-film FETs. In (a) and (b), the gate dielectric was 600 nm-thick parylene. (c)  $V_{\text{out}}-t$  plot of a ring oscillator comprising five inverters, composed of [6]phenacene and PTCDI-C8 thin-film FETs; the gate dielectric was 320 nm-thick  $\text{ZrO}_2$ .

The values of  $\tau_{\text{pLH}}$  and  $\tau_{\text{pHL}}$  are explained in Fig. 8.8 of ref. 33 and Fig. 6.10 of ref. 38, and they are expressed as follows:

$$\tau_{\text{pHL}} = \frac{C_{\text{load}}}{k_{\text{n}}(V_{\text{DD}} - V_{\text{THn}})} \left[ \frac{2V_{\text{THn}}}{V_{\text{DD}} - V_{\text{THn}}} + \ln \left( \frac{4(V_{\text{DD}} - V_{\text{THn}})}{V_{\text{DD}}} - 1 \right) \right], \quad (5)$$

and

$$\tau_{\text{pLH}} = \frac{C_{\text{load}}}{k_{\text{p}}(V_{\text{DD}} - |V_{\text{THp}}|)} \left[ \frac{2|V_{\text{THp}}|}{V_{\text{DD}} - |V_{\text{THp}}|} + \ln \left( \frac{4(V_{\text{DD}} - |V_{\text{THp}}|)}{V_{\text{DD}}} - 1 \right) \right]. \quad (6)$$

$C_{\text{load}}$  refers to the total capacitive load of the inverter, as shown in ref. 38. It is noteworthy that  $k = \frac{\mu WC_0}{L}$ , where  $k_{\text{p}}$  and  $k_{\text{n}}$  refer to the  $k$  values for the p- and n-channel FETs, as described in Section 3.2. As shown in eqn (3), a decrease in  $n$  results in an increase in  $f_{\text{osc}}$ . In addition, the values of experimental  $\langle \tau_{\text{p}} \rangle$  were determined to be 3.8 ms for  $f_{\text{osc}} = 26$  Hz

(Fig. 7(a)) and 4.8 ms for  $f_{\text{osc}} = 21$  Hz (Fig. 7(b)) from the equation,  $\langle \tau_{\text{p}} \rangle = \frac{1}{10f_{\text{osc}}}$ .

As shown in eqn (4)–(6), a smaller  $L$  should provide a smaller  $\langle \tau_{\text{p}} \rangle$  through a larger  $k_{\text{p}}$  and  $k_{\text{n}}$ . Consequently, a smaller  $\langle \tau_{\text{p}} \rangle$  results in a larger  $f_{\text{osc}}$ , as indicated from eqn (3). It is noteworthy that a larger  $W$  ( $=500$  or  $1000 \mu\text{m}$ ) in the PTCDI-C8 thin-film FET than that ( $W = 200$  or  $300 \mu\text{m}$ ) in the p-channel FET was used in the ring oscillator, so that the small  $\mu$  value obtained in the n-channel PTCDI-C8 FET was compensated in  $k_{\text{n}} = \frac{\mu WC_0}{L}$ . To summarize, the fabrication of a ring oscillator with a smaller  $L$  (*i.e.*, a microscale ring oscillator) will significantly increase the value of  $f_{\text{osc}}$ . Furthermore, a larger value of  $\mu$  must be realized in n-channel FETs, because the inferior  $\mu$  value of an n-channel FET should enhance  $\langle \tau_{\text{p}} \rangle$  to reduce the value of  $f_{\text{osc}}$ . In the future, the solution to these problems will be attempted in the fabrication of practical RFIDs using phenacene molecules.

The decent operation of a ring oscillator *via* a combination of phenacene molecules and PTCDI-C8 is an important step for the integration of practical organic logic gate circuits, regardless of the observed low oscillation frequency, because the phenacene molecules provide high FET performance. In



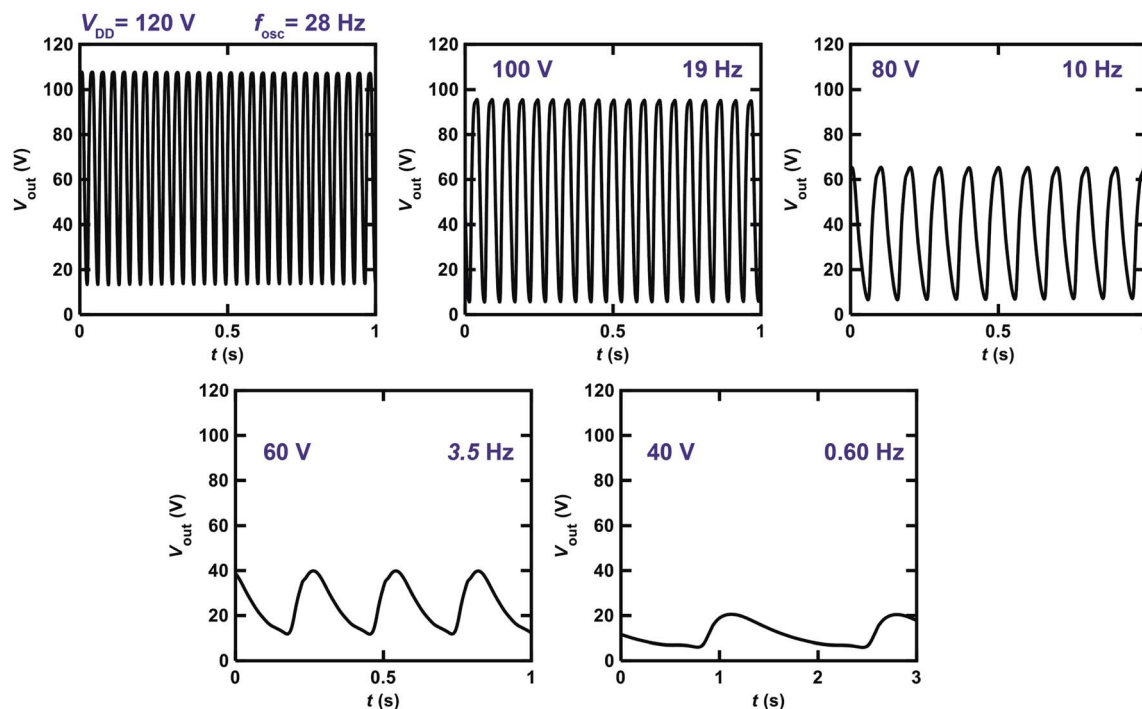


Fig. 8  $V_{out}$ - $t$  plots of ring oscillators comprising five inverters, which are composed of [6]phenacene and PTCDI-C8 thin-film FETs, measured at different  $V_{DD}$  values. The gate dielectric was 600 nm-thick parylene.

addition, the diverse possibilities and the ease with which phenacene molecules can be designed appears quite likely to lead to the development of promising materials for ring oscillators with high oscillation frequency in the near future. Finally, we comment briefly on a relevant recent ring oscillator based on a small organic molecule, 2,9-diphenyl-dinaphtho-[2,3-*b*:2',3'-*f*]thieno[3,2-*b*]thiophene (DPH-DNTT).<sup>42</sup> The best value of  $\tau_p$  was 138 ns for the ring oscillator. Our next research target is to

fabricate a ring oscillator with a  $\tau_p$  comparable to that value using phenacene molecules. For this purpose, we will optimize the device structure, as well as searching for more suitable phenacene molecules for the ring oscillator. Also, to fabricate ring oscillators using phenacene molecules on a plastic or glass substrate, which may have a smaller parasitic capacitance than an SiO<sub>2</sub>/Si substrate, would be a future task to realize a ring oscillator with a high value of  $f_{osc}$ .

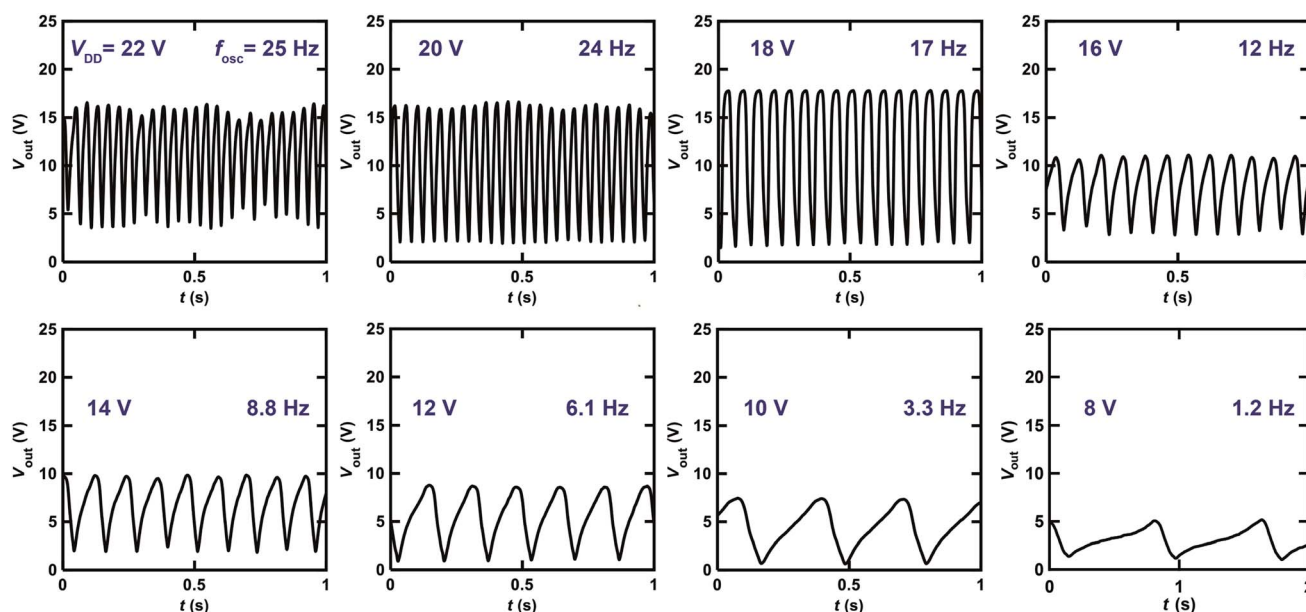


Fig. 9  $V_{out}$ - $t$  plots of ring oscillators comprising five inverters, which are composed of [6]phenacene and PTCDI-C8 thin-film FETs, measured at different  $V_{DD}$  values. The gate dielectric was 320 nm-thick ZrO<sub>2</sub>.



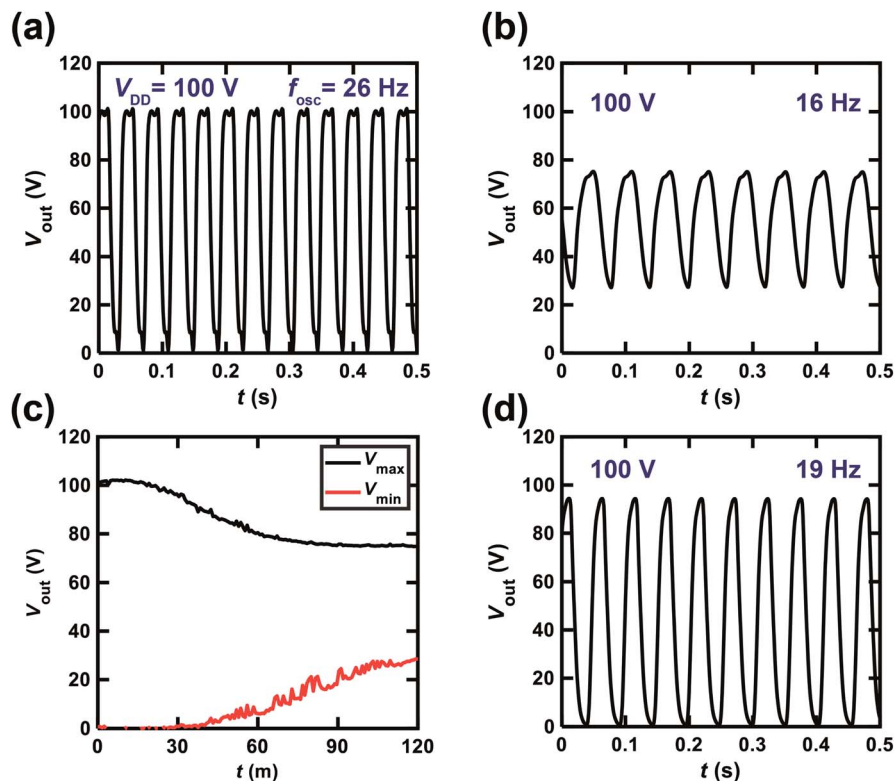


Fig. 10  $V_{\text{out}}-t$  plots of ring oscillators using five inverters that are composed of [6]phenacene and PTCDI-C8 thin-film FETs and a gate dielectric of 600 nm-thick parylene.  $V_{\text{out}}-t$  plots recorded at (a) the first measurement and (b) the measurement after a continuous application of  $V_{\text{DD}} = 100$  V for 2 h. (c) Plots of  $V_{\text{max}}$  and  $V_{\text{min}}$  as a function of  $t$  of the ring oscillator, which refer to the variation in  $V_{\text{out}}$  measured between the plots shown in (a) and (b). (d)  $V_{\text{out}}-t$  plot measured after storing the ring oscillator device above without applying  $V_{\text{DD}}$  for two months.

### 3.4. Durability of ring oscillators fabricated using phenacene and PTCDI-C8 FETs

Fig. 10(a) shows the  $V_{\text{out}}-t$  plot for the ring oscillator comprising five CMOS inverters; each inverter was fabricated using a [6] phenacene thin-film FET for p-channel operation and a PTCDI-C8 thin-film FET for n-channel operation; the parylene film was used for the gate dielectric in this ring oscillator. As shown in Fig. 10(a), the  $f_{\text{osc}}$  was 26 Hz when the applied  $V_{\text{DD}}$  was 100 V. The ring oscillator was operated continuously for 2 h, and then the  $V_{\text{out}}-t$  plot was recorded (Fig. 10(b)), indicating a 16 Hz operation in the ring oscillator. Namely, the value of  $f_{\text{osc}}$  decreased from 26 to 16 Hz during continuous application of  $V_{\text{DD}} = 100$  V. Furthermore, the amplitude of  $V_{\text{out}}$  decreased from 100 (Fig. 10(a)) to 50 V (Fig. 10(b)). Thus both the  $f_{\text{osc}}$  and amplitude of  $V_{\text{out}}$  were decreased by continuous operation of the ring oscillator, which was likely due to the bias stress effect. The bias stress effect degraded the FET properties in the phenacene thin-film FET,<sup>16,19,26,30</sup> which may have been caused by the presence of trap states in the interface between the phenacene/PTCDI-C8 and the parylene gate dielectric. The trap states were produced by a trace of water at the interface and gate voltage application.<sup>43-48</sup> The small amount of water at the interface, which yields trap states, might not be removed for a long time, even in an Ar-filled glove box, which is a common phenomenon.

Fig. 10(c) shows the  $V_{\text{max}}-t$  and  $V_{\text{min}}-t$  plots for the ring oscillator, indicating that the value of  $V_{\text{max}}$  minus  $V_{\text{min}}$

(amplitude of  $V_{\text{out}}$ ) decreases continuously above  $t = 30$  min. In other words, the amplitude of  $V_{\text{out}}$  remains constant up to  $\sim 30$  min. We stopped the operation of the ring oscillator and stored the ring oscillator without any  $V_{\text{DD}}$  for two months. After two months, we recorded the  $V_{\text{out}}-t$  plot (Fig. 10(d)), which showed an  $f_{\text{osc}}$  value of 19 Hz, and an  $V_{\text{out}}$  amplitude of 90 V. Therefore, the oscillation performance was recovered by not applying  $V_{\text{DD}}$  for two months. The features are intrinsically the same as the bias-stress degradation of FET properties discovered in some phenacene thin-film FETs.<sup>16,19,26,30</sup>

## 4. Conclusion

In this study, the successful operation of a ring oscillator composed of five CMOS inverters using phenacene and PTCDI-C8 thin-film FETs was demonstrated. An  $f_{\text{osc}}$  value exceeding 20 Hz was stably observed using a [6]phenacene or  $(\text{C}_{14}\text{H}_{29})_2$ -picene thin-film FET for p-channel operation and a PTCDI-C8 thin-film FET for n-channel operation. A parylene gate dielectric was used for the ring oscillator. Moreover, the ring oscillator using CMOS inverters composed of [6]phenacene and PTCDI-C8 FETs with  $\text{ZrO}_2$  showed a low-voltage operation. The value of  $f_{\text{osc}}$  obtained was the same as that using the parylene gate dielectric. The durability experiment on the ring oscillator clarified the presence of the bias stress effect in the ring oscillator, *i.e.*, the  $f_{\text{osc}}$  and  $V_{\text{out}}$  amplitude decreased significantly. However, the performance of the ring oscillator was restored by storing the device





without applying a  $V_{DD}$  for two months. The successful operation of the ring oscillator demonstrated the potential application of phenacene molecules in integrated logic gate circuits, and a workable fabrication process for the ring oscillator was shown clearly in this study. Therefore, this is of significance as the initial stage of the development of high-performance integrated logic gate circuits using phenacene molecules, even if the oscillation frequency is still low. Thus, this study can serve as a basis for the fabrication of RFIDs using phenacene molecules.

## Author contribution

All the authors contributed to the writing of this manuscript. All authors have given their approval to the final version of the manuscript.

## Conflicts of interest

There are no conflicts to declare.

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