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Gate-bias instability of few-layer WSe_2 field effect transistors†

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Semiconducting two-dimensional (2D) layered materials have shown great potential in next-generation electronics due to their novel electronic properties. However, the performance of field effect transistors (FETs) based on 2D materials is always environment-dependent and unstable under gate bias stress. Here, we report the environment-dependent performance and gate-induced instability of few-layer p-type WSe_2-based FETs. We found that the hole mobility of the transistor drastically reduces in vacuum and further decreases after *in situ* annealing in vacuum compared with that in air, which can be recovered after exposure to air. The on-current of the WSe_2 FET increases with positive gate bias stress time but decreases with negative gate bias stress time. For the double sweeping transfer curve, the transistor shows prominent hysteresis, which depends on both the sweeping rate and the sweeping range. Large hysteresis can be observed when a slow sweeping rate or large sweeping range is applied. In addition, such gate-induced instability can be reduced in vacuum and further reduced after *in situ* vacuum annealing. However, the gate-induced instability cannot be fully eliminated, which suggests both gases adsorbed on the device and defects in the WSe_2 channel and/or the interface of WSe_2/SiO_2 are responsible for the gate-induced instability. Our results provide a deep understanding of the gate-induced instability in p-type WSe_2 based transistors, which may shed light on the design of high-performance 2D material-based electronics.

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1. Introduction

Two-dimensional (2D) materials have attracted tremendous attention in recent years due to their excellent electrical and optoelectrical properties.[1–3] Among the family of 2D materials, semiconducting transition metal dichalcogenides (TMDCs) are the most intensively studied materials beyond graphene due to their suitable bandgap, novel optical properties, large carrier mobility, *etc.*[4–8] Due to the weak van der Waals (VDW) interaction between layers, TMDCs can be easily thinned down to monolayer without any dangling bonds on the surfaces. Theoretically, the carrier mobility of the monolayer TMDCs is larger than that of the Si in the same thickness, which is promising for solving the short channel effect in Si-based transistors.[9–11] Thus, much effort has been carried out in TMDC-based field effect transistors (FETs). Furthermore, TMDC transistors are also explored in flexible thin film transistors due to their ultrathin thickness and outstanding electrical properties.[12–14]

As a member of TMDCs, WSe_2 has modulated carrier types and relatively large carrier mobility,[15–18] which is essential for the realization of high-performance complementary metal oxide semiconductor (CMOS) logic devices. For example, recent experiments have shown that the carrier type of WSe_2 can be modulated to p-type, n-type, or even bipolar by controlling the thickness of WSe_2 and contact electrode metal.[15] In addition, the monolayer WSe_2 in contact with indium has an electron-mobility of about 142 $cm^2\ V^{-1}\ s^{-1}$, and the hole-mobility of NO_2-doped WSe_2 is 140 $cm^2\ V^{-1}\ s^{-1}$.[19]

However, due to the high specific surface area, the performance of many 2D-TMDC-material-based electronic devices is strongly affected by the atmospheric environment.[20,21] For example, Qiu *et al.* confirmed that the chemisorption of oxygen and water from the ambient causes degradation of MoS_2 transistors' conductance by up to 100 times;[22] Chow *et al.* showed that the electron and hole mobilities of a 9 nm-thick $PdSe_2$ FET are ~7 and 5.9 $cm^2\ V^{-1}\ s^{-1}$ respectively, with an on/off ratio of $\sim 10^2$. After vacuum annealing, it exhibited electron-dominated transport with a high electron mobility of ~216 $cm^2\ V^{-1}\ s^{-1}$ and a decent on/off ratio of 10^3.[23] In addition, owing to the complex of the growth thermodynamics and kinetics, surface defects are unavoidable in the VDW 2D materials.[24] When they are

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processed into transistors, the appearance of gate bias stress instability and hysteresis effect associated with their transfer characteristics are unavoidable, which hinders their practical applications.[25–27] Till now, reported gate bias stress instability and hysteresis effects are focused on the on n-type 2D material-based FETs, such as MoS_2,[22,28,29] WS_2,[24] InSe.[30] The study on the gate bias instability and hysteresis effect on complementary p-type 2D material-based FETs is scarce, which is an important factor for the practical device implementation.

In this work, we fabricated few-layer WSe_2 based p-type FET and found that the carrier mobility of the few-layer WSe_2-FET is environment-dependent, and we systematically investigated the gate bias stress instability of the device under different environments. Due to the existence of charge traps, the transfer characteristic curves of the device cannot be fitted by a linear relationship, which indicates that the carrier mobility depends on the gate voltage. In addition, the mobility of the transistor drops drastically in vacuum and further decreases after *in situ* annealing in vacuum, which can be recovered after exposing in air. In addition, the performance of the device is even better when increasing the humidity of the environment. In contrast to previous reports on gate bias instability of TMDCs, our results show that the gate bias instability cannot be only attributed to the water and oxygen adsorption/desorption on the surface of the channel, but also the existence of intrinsic and/or interface defects in the few-layer WSe_2. Our research not only discovered the origin of gate bias stress instability and hysteresis in WSe_2, but also would be a helpful guidance for the design and preparation of WSe_2 gas or chemical sensors.

2. Methods

Few-layer WSe_2 flakes were mechanically peeled from the bulk WSe_2 crystals (6carbon Tech. Shenzhen) and transferred onto the silicon substrate that coated with 285 nm SiO_2. Then, global back-gate FETs were fabricated on the processed substrate. UV lithography was used to define the source/drain regions, followed by the thermal evaporation deposition of Au (80 nm) electrodes and lift-off process. Raman measurements were conducted on Andor SR-500i-A-R Raman spectrometer system with a 532 nm excitation laser. The thickness of the WSe_2 thin film was determined by atomic force microscope (AFM, FM-Nanoview 1000). All electrical measurements were carried out in a vacuum probe station. Keithley 2636B semiconductor analyzer was utilized to measure the electrical properties of fabricated transistors. The device was *in situ* annealed up to 373 K by a Pico-Femto stage heater for 5.5 h.

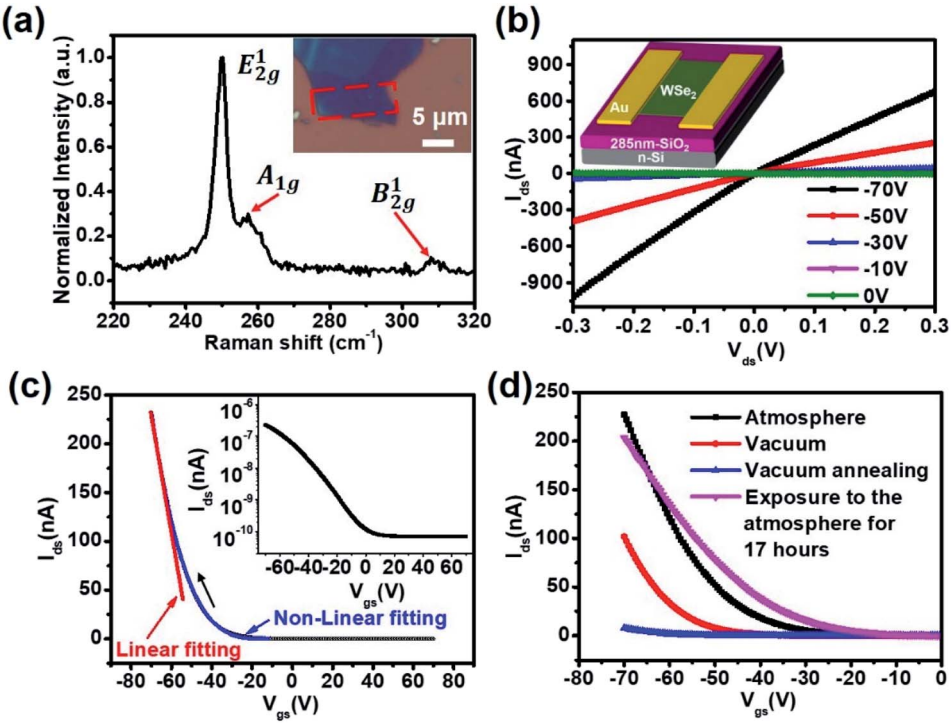

Fig. 1 Raman spectrum, optical microscopy image, schematic diagram, and electrical properties of the typical few-layer WSe_2 FETs. (a) Raman spectrum of few-layer WSe_2, where 250.2 cm^{-1}, 257.3 cm^{-1}, and 308.0 cm^{-1} correspond to the, A_{1g} and B^1_{2g} Raman modes, respectively. (Inset) Optical image of a few-layer WSe_2 exfoliated on Si/SiO_2 substrate. The red dashed outline represents the channel region of the device. (b) Output characteristics with the gate voltage varied from −70 to 0 V. (Inset) Schematic diagram of back-gated few-layer WSe_2-FET. (c) Transfer characteristics with the source-drain voltage of 0.1 V and sweeping rate of 8.2 V s^{-1} (black curves). The inset shows the logarithmic plot of the device transfer curve presented in (c). (d) Transfer curves of the device in the atmosphere (black curves), vacuum (red curves), vacuum annealing environment (blue curves), and re-exposed to the atmosphere for about 17 hours (pink curve), where the source-drain voltage and sweeping rate are the same as (c).

3. Results and discussion

The few-layer WSe_2 is obtained by the conventional tape-assisted mechanical exfoliation, which is shown in the inset of Fig. 1a. The region marked with red dashed rectangular is the channel area before device fabrication. As shown in Fig. 1a, the Raman spectrum of this region exhibits three characteristic peaks of 250.2, 257.3, and 308.0 cm^{-1} corresponding to the E^1_{2g}, A_{1g} and B^1_{2g} Raman modes of WSe_2, respectively.[31] In fact, the characteristic peak at 257.3 cm^{-1} is controversial. Some literature tentatively attributed it to the to the A_{1g} mode,[31,32] while others assigned it to second order Raman processes.[33,34] It is worth noting that the B^1_{2g} Raman mode might arise from the interlayer interaction and the red shift of the Raman peak was observed as the layer number of WSe_2 increased from 2L to 5L.[31] The characteristic peak of B^1_{2g} Raman mode in Fig. 1a is located at 308.0 cm^{-1}, indicating a layer number of about three,[31,35] which is consistent with the AFM results of thickness of about 3.63 nm (see Fig. S1b in ESI†). In a word, the sharp Raman peaks suggest the good crystallinity of the few-layer WSe_2.

To investigate the electrical properties of the few-layer WSe_2, a universal back-gated FET is fabricated as schematically shown in the inset of Fig. 1b (See the optical microscopy image of the fabricated device in Fig. S1a†). The channel length and width are 2.57 and 12.9 μm, respectively. Almost linear drain-source current *vs.* drain-source voltage (I_{ds}–V_{ds}) curves are observed in the output characteristic curves (Fig. 1b), indicating an ohmic-like contact between the channel material and the source/drain electrodes. In addition, the current increases with the decreasing of the gate voltage, suggesting a p-type conductivity of the few-layer WSe_2 FET. For further understanding the electrical properties of the WSe_2 transistor, the transfer curve was measured which are shown in Fig. 1c (black curves). The typical p-type transfer curve is consistent with the output curves. The current on/off ratio is about 4×10^3 according to the logarithmic plot shown in the inset of Fig. 1c. The mobility of the hole can be calculated from the transfer curve according to the formula:

$$I_{ds} = \mu C_{ox} \frac{W}{L} |V_{gs} - V_T| V_{ds} \quad (1)$$

where μ is the field-effect hole mobility, C_{ox} is the gate capacitance per unit area (12.1 nF cm^{-2} for 285 nm-thick SiO_2), L is the channel length (2.57 μm), W is the channel width (12.9 μm) and V_T is the threshold voltage. In this regard, the field-effect hole mobility is calculated to be 1.79 $cm^2\ V^{-1}\ s^{-1}$ with a threshold voltage of −49.8 V. It is obvious that linear fitting is only valid in the large gate voltage range (red line in Fig. 1c), which indicates that the carrier mobility depends on the gate voltage. As a matter of fact, the gate-dependent mobility has been observed in 2D material-based FETs.[24,25] Usually, a semi-empirical relationship is used to characterize the relationship between carrier mobility and gate voltage:[36]

$$\mu = \kappa |V_{gs} - V_T|^{\alpha} \quad (2)$$

where κ and α are the fitting parameters, and V_T is the threshold voltage. By substituting eqn (2) into eqn (1), there would be a non-linear relationship to describe the transfer characteristics as below:

$$I_{ds} = C_{ox} \frac{W}{L} \kappa |V_{gs} - V_T|^{1+\alpha} V_{ds} \quad (3)$$

As expected, the transfer characteristic curve can be well-fitted by eqn (3) (Fig. 1c, blue curve). From the fitting, the corresponding values of V_T, κ, and α are −11.2 V, 2.05×10^{-5} $cm^2\ V^{-(1+\alpha)}\ s^{-1}$, and 2.54, respectively. When the gate voltage is −70 V, the hole mobility is estimated to be 0.64 $cm^2\ V^{-1}\ s^{-1}$, which is smaller than the hole mobility value obtained by the linear fitting. The possible reason for the gate dependent mobility is charge traps in the channel.[25] The relatively large value of the α parameter indicates the strong dependence of mobility on the gate bias, suggesting the presence of large amounts of hole traps in the few-layer WSe_2.

Because of the ultrathin thickness of the WSe_2, the electrical properties should be sensitive to the environment. In this case, the transfer curve in vacuum and after *in situ* annealing in vacuum were measured, which are shown in Fig. 1d. The current decreases in vacuum in comparison with that in ambient, which further decreases after *in situ* annealing in vacuum. The results indicate that the adsorbents on the surface of the WSe_2, such as oxygen and water, are electron acceptors, which lead to p-type doping in WSe_2. The concentration of adsorbents reduces in vacuum and further reduces after an *in situ* annealing in vacuum. As a result, the hole concentration in vacuum also reduces and further reduces after an *in situ* annealing in vacuum, leading to the decrease of the output current. The hole mobility fitted by eqn (3) is 0.64, 0.32 and 0.02 $cm^2\ V^{-1}\ s^{-1}$ in ambient, vacuum, and after *in situ* annealing in vacuum, respectively. The decrease of the hole mobility should be attributed to the low hole concentration, which leads to large scattering by charge traps. In addition, the current can be recovered after exposing the device to air as shown in Fig. 1d. The evolution of the transfer curve with time after exposing in ambient (see Fig. S2a in ESI†) indicates that the current can be recovered after 300 minutes exposure in ambient. Furthermore, when the humidity is increased from 50% to 70%, the current shows an abrupt increasing, from 203 to 462 nA in 60 minutes (see Fig. S2b in ESI†), indicating that water molecules can lead to strong p-type doping. The result suggests the possibility of the WSe_2 transistors acting as humidity sensors and the strong p-type doping effect of water molecules.

It has been reported that gas molecules absorption and desorption processes will lead to gate bias instability and hysteresis in literature.[28,30,37,38] Therefore, the gate bias stress instability and hysteresis effect in the few-layer WSe_2 FET is studied. Fig. 2a shows the transfer characteristic curves sweeping from −70 to 70 V under different negative gate bias (−70 V) stress times. In order to recover to the initial state of the device, an idle time of about 30 min is needed between each measurement. It can be clearly seen that the transfer characteristic curve gradually shifts to the negative direction with the

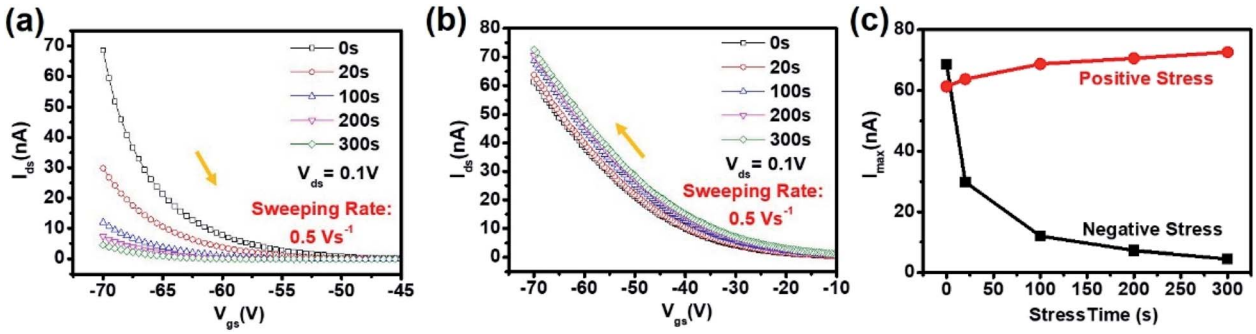

Fig. 2 Effect of gate bias stress on the electrical properties of few-layer WSe_2 FETs. (a) Negative stress under different stress time. (b) Positive stress under different stress time. (c) Maximum output current (I_{max}) as a function of stress time. During the measurement of these transfer curves under atmosphere, the source-drain voltage is fixed at 0.1 V, while the voltage sweeping rate is controlled to 0.5 V s^{-1}.

increasing negative gate bias stress time. Since the transfer characteristic curve cannot be well linearly fitted, the threshold voltage needs to be obtained through a nonlinear fitting equation. For simplicity, the relationship between the maximum output current (I_{ds}) value and different stress times is used to illustrate the effect of the gate bias stress on the device performance. The maximum output current drops quickly for the negative gate bias stress time in the first 20 s, and then decreased slowly and stabilized (Fig. 2c). On the other hand, with the increase of the positive gate bias (70 V) stress time, the transfer characteristic curve sweeping from 70 to −70 V shifts to the positive direction (Fig. 2b), and the maximum current increases slowly, which is opposite to the ones under negative gate bias stress (Fig. 2c). Gas molecules in air, such as water and oxygen, can be absorbed on the surface of the WSe_2 due to electrons transfer from WSe_2 to the gas molecules, leading to p-type doping effect in WSe_2.[39] Initially, the adsorption and desorption of gas molecules are in a balance state. Under negative gate bias, holes are induced in the channel and the balance is destroyed. As a result, electrons on the adsorbed molecules will transfer back to the WSe_2 channel, leading to the reduced hole concentration thus reduced current. Furthermore, the longer negative gate bias time, the lower hole concentration in the WSe_2 channel, which is consistent with the decrease of the maximum output current with negative gate bias stress time. However, as the adsorption gas molecules are limited, the

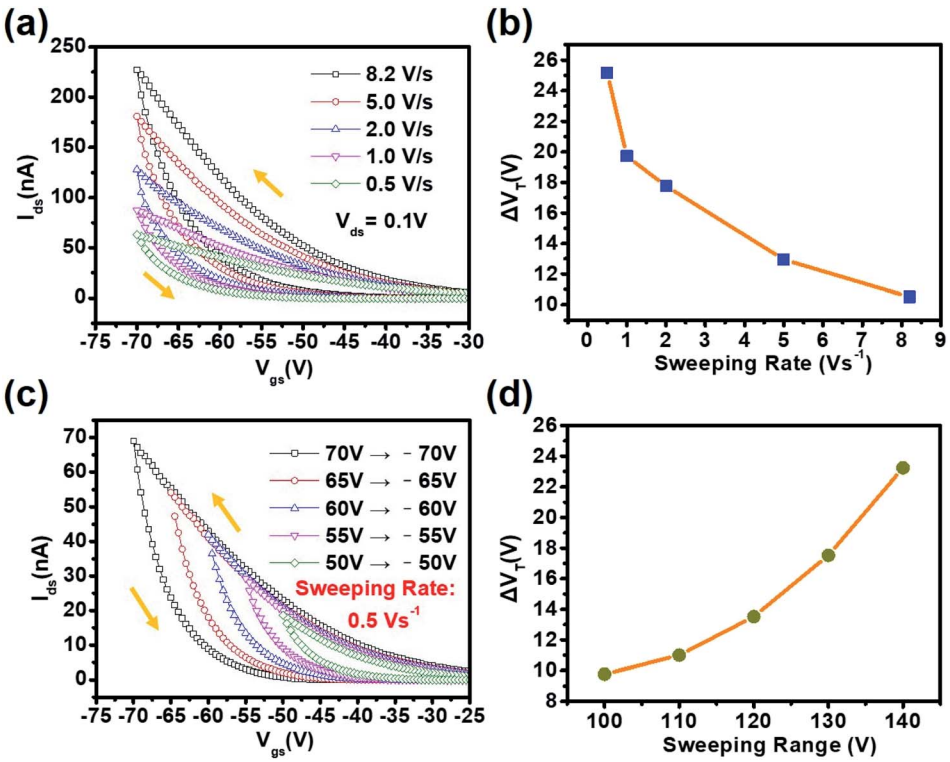

Fig. 3 Hysteresis characteristics of the few-layer WSe_2 FETs. (a) Double sweeping transfer curves with different sweeping rates. (b) Change of threshold voltage (ΔV_T) as a function of the voltage-sweeping rate. (c) Double sweeping transfer curves with different gate sweeping ranges, where the sweeping rate is 0.5 V s^{-1}. (d) Threshold voltage difference as a function of the sweeping range. The source-drain voltage is 0.1 V.

hole concentration should approach a minimum concentration when all the adsorption gas molecules desorbed, leading to the saturation of the output current. While under positive gate bias, hole concentration in the channel is reduced. More gas molecules are adsorbed on the surface of the WSe_2 channel. When the channel is in the ON state, the hole concentration is increased due to the increased adsorbed gas molecules. Due to the limited surface area, the adsorbed gas molecules have a maximum concentration, leading to a saturated maximum output current when a long positive gate bias stress is applied.

The adsorption and desorption of gas molecules will lead to hysteresis in the double sweeping transfer curves. Fig. 3a shows the double sweeping transfer curves at different sweeping rates starting from 70 to −70 V and then −70 to 70 V, in which the maximum current value decreases as the decreasing sweeping rates and obvious hysteresis can be observed. The threshold voltage difference (ΔV_T) between backward and forward sweepings is used to characterize the magnitude of the hysteresis. The relationship between ΔV_T and sweeping rates is depicted in Fig. 3b. It is apparent that the hysteresis increases with the decreasing sweeping rates. The difference of the hysteresis under different sweeping rate is caused by the equivalent gate bias stress effect.[24] The equivalent negative bias stress effect is weak for the fastest sweeping rate (8.2 V s^{-1}), which is on the opposite for the slowest sweeping rate (0.5 V s^{-1}). As a result, the maximum current of the transfer curve for the fastest sweeping rate is the largest while the hysteresis of the transfer curve for the slowest sweeping rate is the largest. To further reveal the hysteresis behavior of the few-layer WSe_2-FET, the double sweeping transfer curves with different sweeping ranges were measured and are shown in Fig. 3c. It is clear that the backward sweeping current under the same gate voltage shows a little increase with the sweeping range while the backward sweeping current shows a great difference with the sweeping range (Fig. 3c). Based on the threshold voltage difference between backward and forward sweepings obtained by nonlinear fitting, it is clear that the threshold voltage difference drops sharply as the sweeping range decreases (Fig. 3d). In other words, the hysteresis would decrease as the sweeping range decreases. The little increase of the backward sweeping current is caused by the longer equivalent positive gate bias stress when the gate voltage is larger than the threshold hold voltage during the sweeping. The faster drop of the output current with a larger sweeping range for the forward sweeping is caused by the longer equivalent negative gate bias stress effect. As a result of the equivalent gate bias stress effect, the hysteresis increases with the increase of the sweeping range.

Actually, many research teams have found that intrinsic defects and interface defects can also cause hysteresis in MoS_2 FET.[26,40–47] To check whether the adsorbed gas molecules is the only factor that leads to the gate bias instability of the transistor, similar measurements were carried out in vacuum (4×10^{-4} Pa) and after *in situ* annealing in vacuum (373 K, 5 h). Similar phenomena are observed in vacuum and after *in situ* annealing in vacuum (Fig. S3 and S4†). The most obvious difference is the output current magnitude. The output current drops in vacuum and further drops after annealing in vacuum (Fig. 4a and d). The decreasing of output current is consistent

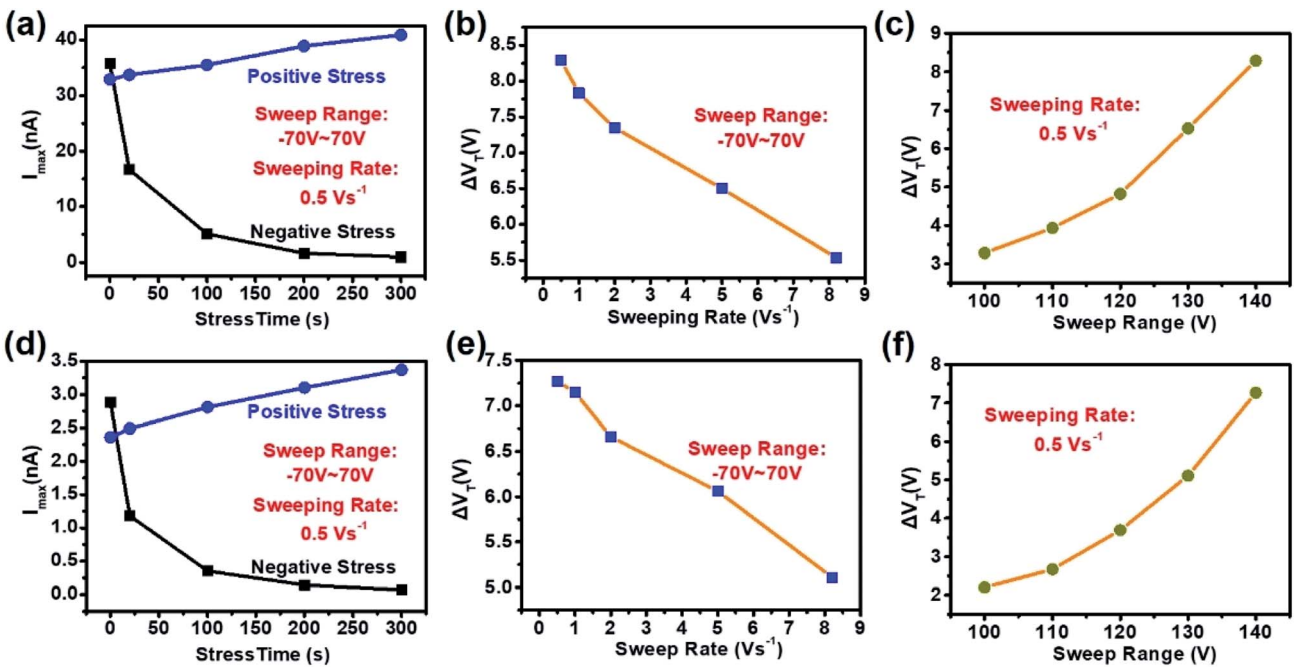

Fig. 4 Gate bias instability of the WSe_2 FETs in different conditions. (a) Maximum output current (I_{max}) as a function of stress time in vacuum. (b) Threshold voltage difference as a function of sweeping rate in vacuum. (c) Threshold voltage as a function of the sweeping range in vacuum. (d) Maximum output current (I_{max}) as a function of stress time after *in situ* annealing in vacuum. (e) Threshold voltage difference as a function of sweeping rate after *in situ* annealing in vacuum. (f) Threshold voltage as a function of the sweeping range after *in situ* annealing in vacuum.

with the environment-sensitive electrical property shown in Fig. 1d. Generally, the adsorbed gas molecules on the surface of the WSe_2 channel cannot be fully eliminated in vacuum. Thus, the existence of gate bias stress effect and hysteresis in vacuum (Fig. 4a–c, and S3†) can still be attributed to the adsorbed gas molecules on the surface of the WSe_2 channel. This can be confirmed by the further decreasing of output current after *in situ* annealing in vacuum (Fig. 4d). However, the gate bias instability still in presence after *in situ* annealing in vacuum (Fig. 4d–f). Most of the adsorbed gas molecules should be eliminated after *in situ* annealing in vacuum. This way, the appearance of the gate instability should be attributed to the presence of charge traps arising from defects in the channel and/or near the interface of the channel and dielectric. In fact, the existence of intrinsic defect in WSe_2 flake can be confirmed by the PL spectrum from single layer part, where defects related emission can be clearly seen (Fig. S5†). These results suggest that the gate bias instability in the air should not only be caused by the gas adsorption but also the defects in the WSe_2 channel and/or near the interface of the WSe_2 and SiO_2. In addition, devices with different thickness and lateral size were fabricated and measured to check the universality of the effects. We note that the above-mentioned gate bias instability effect can be found for all the measured few-layer devices (see Fig. S6–S18 in ESI†). Further works on defect engineering to eliminate the gate induced instability for digital logic devices or inversely to utilize the hysteresis in a controlled manner for memory devices are desired for achieving novel 2D materials functional devices.

4. Conclusion

The gate bias instability of the few-layer WSe_2 FET is studied in detail. The few-layer WSe_2 FET shows environment-sensitive electrical properties, suggesting the gases in air, such as oxygen and water molecules, have strong p-typing doping on the WSe_2 channel. The transfer curve of the WSe_2 FET cannot be modeled by a conventional linear relationship with gate voltage, indicating the presence of charge traps. Furthermore, the transistor shows a strong gate bias effect in which the current decreases under positive gate bias stress and increases under negative gate bias stress. The gate bias stress effect is enhanced with stress time. Under double sweeping, the transfer curve shows obvious hysteresis, which can be explained by the equivalent gate bias stress effect. The gate instability is observed in ambient, vacuum, and after *in situ* annealing in vacuum, indicating that gas molecules adsorption on the surface of the WSe_2 is not the only charge defects, defects in the WSe_2 channel and/or interface between WSe_2 and SiO_2 should also contribute to the gate bias instability of the WSe_2 transistor. This study will be helpful in understanding the gate bias instability of the WSe_2 based electronic devices and shed light on the design of novel electronic devices in the future.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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