

## CORRECTION

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## Correction: 12-state multi-level cell storage implemented in a 128 Mb phase change memory chip

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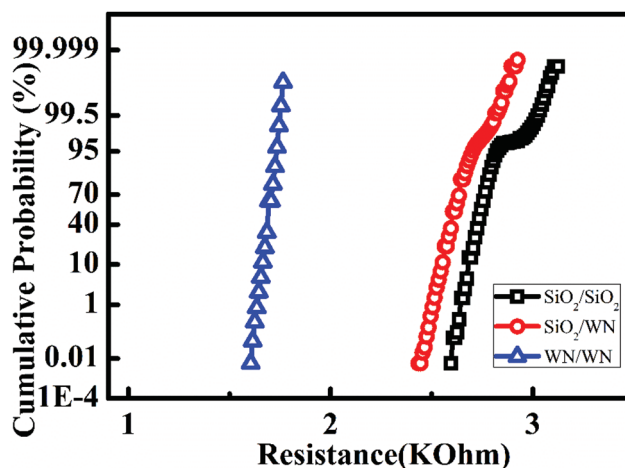
DOI: 10.1039/d1nr90100a

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Correction for '12-state multi-level cell storage implemented in a 128 Mb phase change memory chip' by Zhitang Song *et al.*, *Nanoscale*, 2021, DOI: 10.1039/d1nr00100k.

The authors regret that Fig. 2(a) and 4(a) of the original manuscript contained errors. In the previous Fig. 2(a), the blue curve was labelled as SiN/WN incorrectly – this should be changed to WN/WN. In addition, in Fig. 4(a), the red and blue curves are labelled SiO<sub>2</sub>/XY and XY/XY respectively, which contradicted the figure caption and the main text. These labels should be SiO<sub>2</sub>/WN and WN/WN instead.

Updated versions of Fig. 2(a) and 4, with associated captions, are displayed below.



**Fig. 2** TiN blade BEC electrical properties. (a) Cumulative probability distribution of resistance values for a 3 nm-thick TiN BEC with a quantity of 1k cells.

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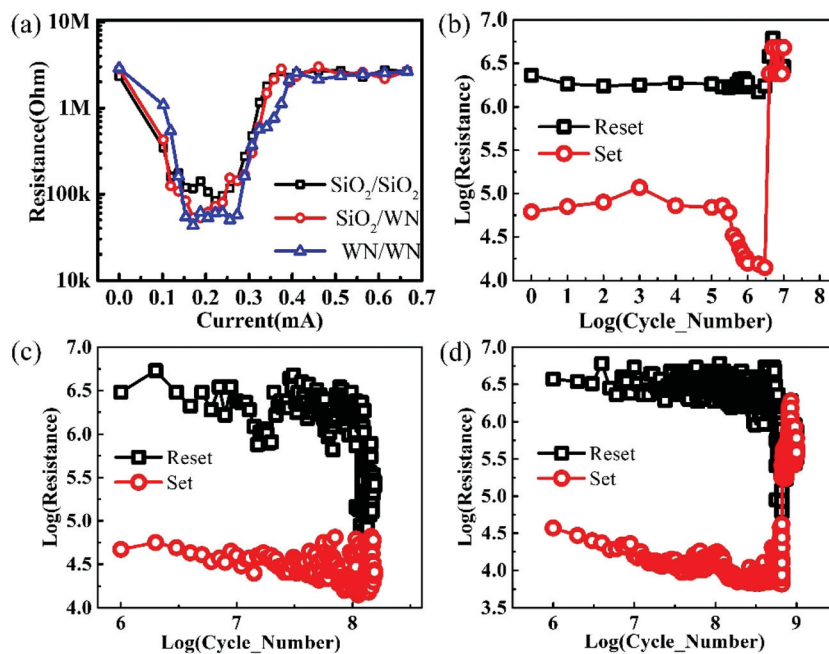


Fig. 4 128 Mb PCM chip performance. (a) Memory windows test of PCM devices with 3 types of coating layers. Endurance of PCM devices, and the BEC coating layers are: (b) SiO<sub>2</sub>/SiO<sub>2</sub>, (c) SiO<sub>2</sub>/WN, and (d) WN/WN.

The Royal Society of Chemistry apologises for these errors and any consequent inconvenience to authors and readers.

