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CORRECTION

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# Correction: 12-state multi-level cell storage implemented in a 128 Mb phase change memory chip

Zhitang Song,*[a] Daolin Cai,*[a] Yan Cheng,[b] Lei Wang,[c] Shilong Lv,[a] Tianjiao Xin[a] and Gaoming Feng[c]

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Correction for '12-state multi-level cell storage implemented in a 128 Mb phase change memory chip' by Zhitang Song *et al.*, *Nanoscale*, 2021, DOI: 10.1039/d1nr00100k.

The authors regret that Fig. 2(a) and 4(a) of the original manuscript contained errors. In the previous Fig. 2(a), the blue curve was labelled as SiN/WN incorrectly – this should be changed to WN/WN. In addition, in Fig. 4(a), the red and blue curves are labelled $SiO_2$/XY and XY/XY respectively, which contradicted the figure caption and the main text. These labels should be $SiO_2$/WN and WN/WN instead.

Updated versions of Fig. 2(a) and 4, with associated captions, are displayed below.

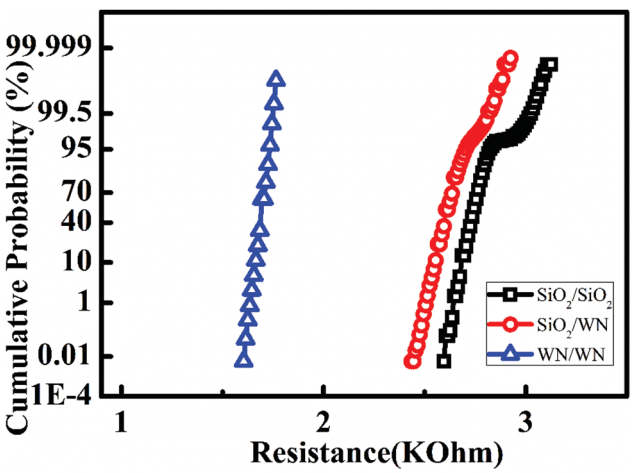


**Fig. 2** TiN blade BEC electrical properties. (a) Cumulative probability distribution of resistance values for a 3 nm-thick TiN BEC with a quantity of 1k cells.

[a]*State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China. E-mail: ztsong@mail.sim.ac.cn, caidl@mail.sim.ac.cn*
[b]*Key Laboratory of Polar Materials and Devices (MOE), Department of Electronics, East China Normal University, Shanghai 200241, China*
[c]*Semiconductor Manufacturing International Corporation, Shanghai 201203, China*



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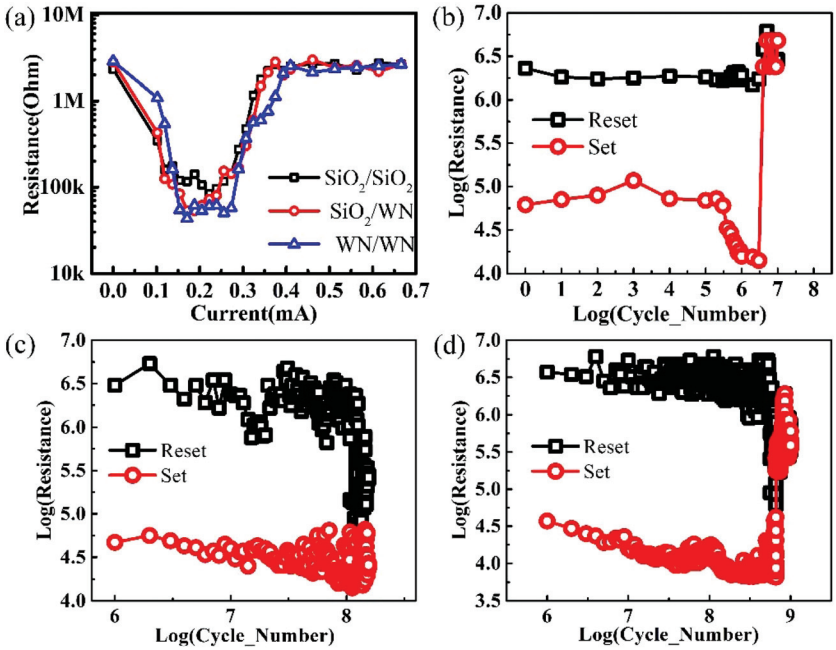


**Fig. 4** 128 Mb PCM chip performance. (a) Memory windows test of PCM devices with 3 types of coating layers. Endurance of PCM devices, and the BEC coating layers are: (b) $SiO_2/SiO_2$, (c) $SiO_2$/WN, and (d) WN/WN.

The Royal Society of Chemistry apologises for these errors and any consequent inconvenience to authors and readers.