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CORRECTION

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Correction: 12-state multi-level cell storage implemented in a 128 Mb phase change memory chip

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Correction for '12-state multi-level cell storage implemented in a 128 Mb phase change memory chip' by Zhitang Song et al., Nanoscale, 2021, DOI: 10.1039/d1nr00100k.

The authors regret that Fig. 2(a) and 4(a) of the original manuscript contained errors. In the previous Fig. 2(a), the blue curve was labelled as SiN/WN incorrectly – this should be changed to WN/WN. In addition, in Fig. 4(a), the red and blue curves are labelled SiO_2/XY and XY/XY respectively, which contradicted the figure caption and the main text. These labels should be SiO_2/WN and WN/WN instead.

Updated versions of Fig. 2(a) and 4, with associated captions, are displayed below.

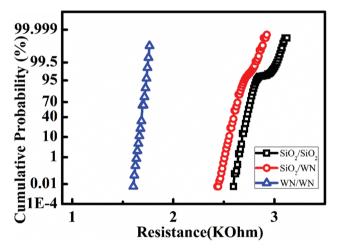


Fig. 2 TiN blade BEC electrical properties. (a) Cumulative probability distribution of resistance values for a 3 nm-thick TiN BEC with a quantity of 1k cells.

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(a) 10M (b) 7.0 Resistance(Ohm) 6.5 SiO₂/Wi 4.5 WN/WI 101 3 0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 4 5 Current(mA) Log(Cycle_Number) (c) (d) 6.5 Log(Resistance) og(Resistance) 6.0 5.5 Set 5.0 4.0 3.5

Fig. 4 128 Mb PCM chip performance. (a) Memory windows test of PCM devices with 3 types of coating layers. Endurance of PCM devices, and the BEC coating layers are: (b) SiO₂/SiO₂, (c) SiO₂/WN, and (d) WN/WN.

The Royal Society of Chemistry apologises for these errors and any consequent inconvenience to authors and readers.

Log(Cycle_Number)