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Rectifying optoelectronic memory based on WSe_2/graphene heterostructures†

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van der Waals heterostructures composed of two-dimensional materials vertically stacked have been extensively studied to develop various multifunctional devices. Here, we report WSe_2/graphene heterostructure devices with a top floating gate that can serve as multifunctional devices. They exhibit gate-controlled rectification inversion, rectified nonvolatile memory effects, and multilevel optoelectronic memory effects. Depending on the polarity of the gate voltage pulses (V_{Gp}), electrons or holes can be trapped in the floating gate, resulting in rectified nonvolatile memory properties. Furthermore, upon repeated illumination with laser pulses, positive or negative staircase photoconductivity is observed depending on the history of V_{Gp}, which is ascribed to the tunneling of electrons or holes between the WSe_2 channel and the floating gate. These multifunctional devices can be used to emulate excitatory and inhibitory synapses that have different neurotransmitters. Various synaptic functions, such as potentiation/depression curves and spike-timing-dependent plasticity, have been also implemented using these devices. In particular, 128 optoelectronic memory states with nonlinearity less than 1 can be achieved by controlling applied laser pulses and V_{Gp}, suggesting that the WSe_2/graphene heterostructure devices with a top floating gate can be applied to optoelectronic synapse devices.

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Introduction

van der Waals (vdW) materials, such as graphene, semiconducting transition metal dichalcogenides, and hexagonal boron nitride (hBN), have received considerable attention owing to their possible applications in ultrathin, flexible, and transparent electronic and optoelectronic devices.[1–4] In particular, vdW heterostructures, in which different vdW materials are vertically stacked, have been extensively studied to develop multifunctional devices.[5–7] For example, various hybrid heterostructures, such as PtS_2/h-BN/graphene,[8] graphene/hBN/MoS_2,y [9] MoS_2/hBN/graphene or MoS_2,[10] and graphene/hBN/$ReSe_2$ [11] exhibit multibit optoelectronic nonvolatile memory effects. When these heterostructures are irradiated with laser pulses, the conductance increases in a staircase behavior, enabling multilevel optical erasing, whereas multilevel programming is achieved by applying gate voltage pulses (V_{Gp}). In contrast to traditional random-access memories (RAMs), optoelectronic random-access memories (ORAMs) can store light information with an electronic readout at low programming voltages. Processing with light as an extra control parameter provides features such as optical and arithmetic logic operations and the simultaneous detection of electrical and optical signals. Furthermore, image-capturing circuits are simplified by the integration of optical sensors and memory devices in ORAMs.

Herein, we report a WSe_2/graphene heterostructure device with a photoresponsive top floating gate. The heterostructure without the top layer exhibited gate-tunable rectifying characteristics without memory effects, which is ascribed to the mismatch between the Fermi levels of graphene and WSe_2 and the ambipolar properties of WSe_2.[12] However, the heterostructure with a MoS_2 top layer exhibited rectifying nonvolatile memory effects with an on/off ratio of $\sim 10^4$ and a retention time of $>10^3$ s, indicating that the MoS_2 top layer acts as a charge trapping layer or floating gate. Kelvin probe force microscopy (KPFM) images revealed that holes and electrons were trapped in the top floating gate by applying $V_{Gp} < 0$ and $V_{Gp} > 0$, respectively, resulting in rectifying nonvolatile memory behaviors. Furthermore, our devices exhibited multilevel optoelectronic memory effects. However, unlike most of the reported optoelectronic devices,[9–11] multilevel programming was achieved by repeated illumination, whereas multilevel erasing was obtained by repeated illumination with laser pulses combined with V_{Gp}.

These gate-tunable rectified multilevel optoelectronic memory properties will pave the way for various future applications. One potential application is in optoelectronic synapse devices. Recently, a variety of two-terminal memristors[13–16] and

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three-terminal devices[17–21] have been explored as artificial synapses for emulating biological synaptic functions. More recently, optoelectronic synapses based on MoO_x,[22] phase-change materials,[23] and black phosphorous/P_xO_y [24] have also been demonstrated. However, although there are two types of biological synapses, called excitatory and inhibitory synapses, which have different neurotransmitters,[25–27] most devices emulate only excitatory synapses. If excitatory neurotransmitters bind to receptors in a postsynaptic neuron, ligand-gated ion channels open and positive ions flow into the cell, generating excitatory postsynaptic currents (EPSCs). In contrast, if inhibitory neurotransmitters bind to receptors, negative ions flow into the cell through ion channels, generating inhibitory postsynaptic currents (IPSCs). For an action potential to occur, the sum of the EPSCs and IPSCs must exceed a threshold value. The balance between excitation and inhibition is very important in the brain. If the balance is disrupted, diseases such as epilepsy can occur.[28]

To investigate whether rectified nonvolatile memory effects can be applied to emulate inhibitory synapses as well as excitatory synapses, two similar devices were connected in parallel. Similar to the addition of EPSCs and IPSCs, the total conductance increased or decreased depending on the polarity of V_{Gp} applied to the two devices. In addition, various synaptic functions, including potentiation and depression processes, and spike-timing-dependent plasticity (STDP) could be emulated, and the recognition rate was simulated to be approximately 72% using an artificial neural network (ANN) based on a single-layer perceptron (SLP) model. These results demonstrate that the WSe_2/graphene heterostructures with a top floating gate can be applied to optoelectronic synapse devices.

Results and discussion

Electrical characteristics of a WSe_2/graphene heterostructure

First, we fabricated a WSe_2/graphene heterostructure on an hBN (~11 nm)/SiO_2/p^{++}-Si substrate with prepatterned Au electrodes to avoid the high Schottky barrier,[29,30] where a gate voltage (V_G) was applied using the p^{++}-Si substrate. Mechanically exfoliated few-layer graphene (~12 nm) and WeS_2 flakes (~10 nm) were transferred onto the electrodes, resulting in a WSe_2/graphene heterostructure (Fig. 1(a)). Initially, the source-drain current (I_{SD})–voltage (V_{SD}) curve of this device showed negligible conductance (Fig. S1†). However, when the I_{SD}–V_G transfer curves were measured by sweeping V_G from −60 to +60 V and back to −60 V, p-type and n-type semiconducting behaviors were observed at V_{SD} = −1 and +1 V, respectively (Fig. 1(b)).

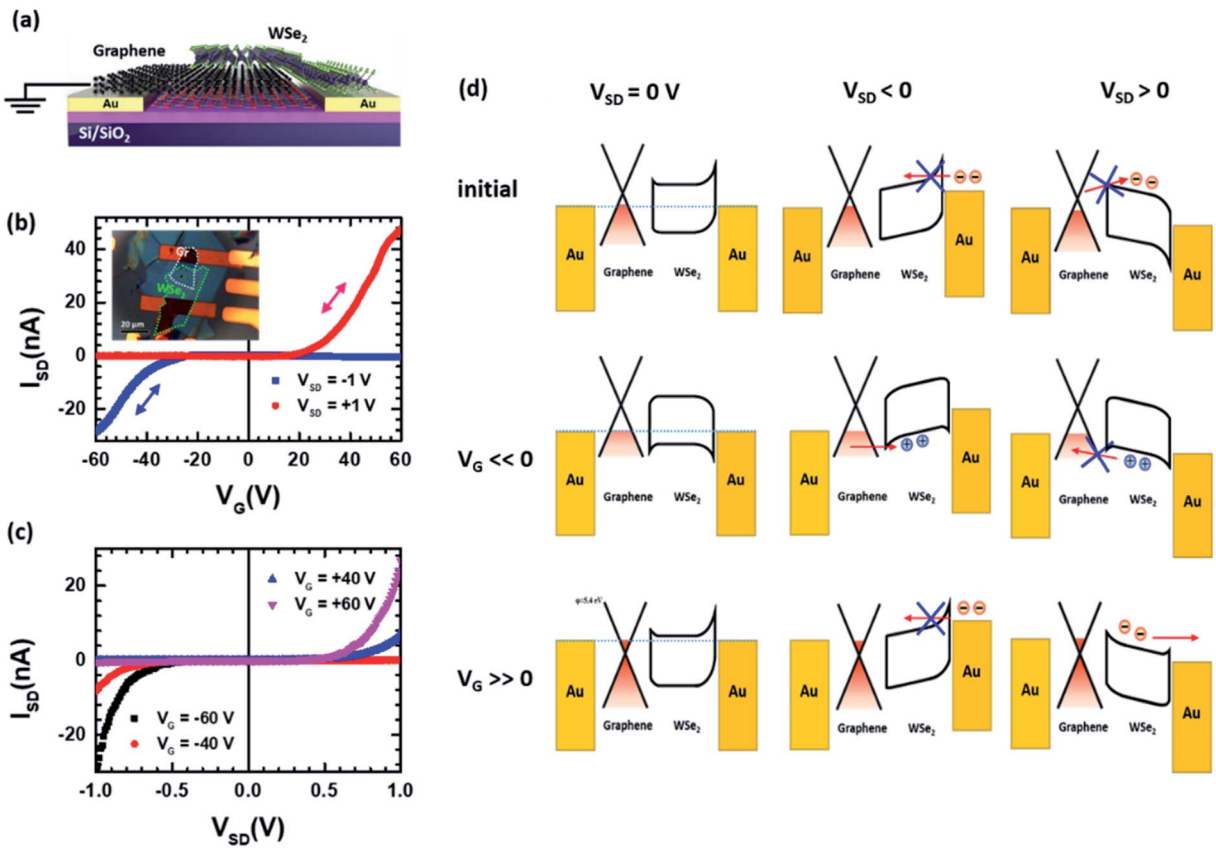

Fig. 1 (a) Schematic of a WSe_2 field-effect device with graphene and Au electrodes. (b) I_{SD}–V_G transfer curves measured at V_{SD} = −1 V (blue symbols) and +1 V (red symbols) by sweeping V_G from −60 to +60 and back to −60 V. The inset shows an optical image of the device. (c) I_{SD}–V_{SD} curves measured when different values of V_G were applied. (d) Energy band diagrams before applying V_G (top), with $V_G \ll 0$ (middle) and $V_G \gg 0$ (bottom).

Accordingly, when $V_G \ll 0$, I_{SD} exhibited finite values at $V_{SD} < 0$, whereas I_{SD} was negligible at $V_{SD} > 0$, leading to rectifying characteristics (Fig. 1(c)). In contrast, when $V_G \gg 0$, the rectification direction was inverted: I_{SD} was finite only for $V_{SD} > 0$. Similar gate-controlled rectifying behaviors have also been reported in other studies.[12,31,32]

This gate-tunable rectification inversion is explained by the energy band diagrams shown in Fig. 1(d). The bandgap (E_g) and electron affinity (χ) of the multilayer WSe_2 are approximately 1.3 and 3.5 eV, respectively,[33,34] and the workfunction (φ) is 4.56 and 5.1 eV for graphene and Au, respectively.[34,35] If $V_G \ll 0$, the Fermi level shifts downward and the major charge carriers become holes. At $V_{SD} < 0$, the holes can move from the graphene to WSe_2, leading to finite currents. However, at $V_{SD} > 0$, the holes cannot flow into the graphene because of the gate-induced Fermi level mismatch between graphene and WSe_2, resulting in a rectifying behavior. In contrast, if $V_G \gg 0$, the Fermi level shifts upward and the major charge carriers are electrons that can flow from the WSe_2 to the Au electrode only at $V_{SD} > 0$. Thus, the rectification direction is inverted.

Memory properties of a WSe_2/graphene heterostructure with a MoS_2 floating gate

Next, we fabricated a WSe_2/graphene heterostructure with a MoS_2 top layer by transferring hBN (~10 nm) and MoS_2 (~11 nm) flakes onto the heterostructure (Fig. 2(a)). The I_{SD}–V_G transfer curves, which were measured by sweeping V_G from −50 to +50 V and back to −50 V, showed n-type and p-type semiconducting behaviors at $V_{SD} > 0$ and $V_{SD} < 0$, respectively, as in the WSe_2/graphene heterostructure without the MoS_2 top layer (Fig. 2(b)). However, the I_{SD}–V_G transfer curves of this device exhibited large hysteresis for both polarities of V_{SD}, indicating that the MoS_2 top layer acted as the floating gate, although the MoS_2 layer was placed on the top of the heterostructure, unlike the conventional flash memory devices that have a floating gate

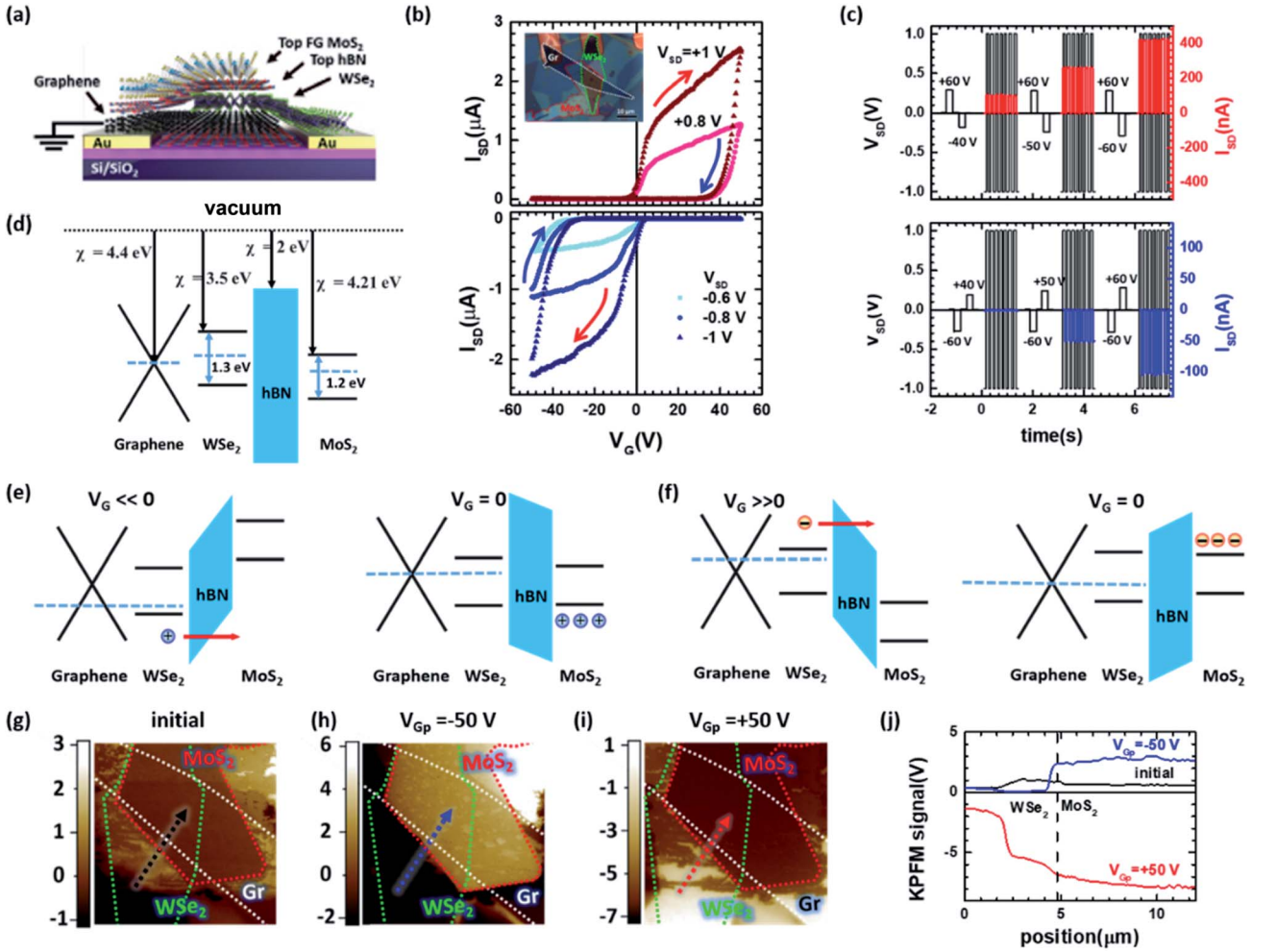

Fig. 2 (a) Schematic of a WSe_2-based device with a MoS_2 top layer. (b) I_{SD}–V_G transfer curves measured at various V_{SD} by sweeping V_G from −50 to +50 V and back to −50 V. (c) I_{SD} measured at V_{SD} of ±1 V square waves with a frequency of 5 Hz after applying various V_{Gp}. Before each measurement, the device was reset by applying $V_{Gp} = +60$ (top) or $V_{Gp} = -60$ V (bottom). Energy band diagrams in (d) a flat band, (e) with $V_{Gp} \ll 0$ and (f) $V_{Gp} \gg 0$. χ represents an electron affinity. KPFM images acquired (g) before applying V_G, (h) after applying $V_{Gp} = -50$ V and (i) $V_{Gp} = +50$ V. Green, white, and red dashed lines indicate WSe_2, graphene, and MoS_2, respectively. (j) Line profile of KPFM signals indicated by arrow lines in (g), (h), and (i).

between a channel and a control gate. To characterize the nonvolatile memory effects, V_{Gp} of −50 V or +50 V with a pulse width of 0.1 s was applied, and I_{SD} was measured at V_{SD} = +1 V (Fig. S2(a)†). The device was switched to the on state by applying V_{Gp} = −50 V and to the off state by applying V_{Gp} = +50 V. On the other hand, the application of V_{Gp} = −50 and +50 V induced the off and on states, respectively, at V_{SD} = −1 V. For both cases, the on/off ratio was ~10^4 and the retention time was estimated to be longer than 10^3 s. To further investigate the nonvolatile memory properties, I_{SD} was measured when ±1 V square waves were applied to the V_{SD} after applying V_{Gp} with different amplitudes (Fig. 2(c)). The rectified multilevel memory states were obtained. When triangular waves were applied to V_{SD} after applying different V_{Gp}, similar rectified multilevel memory effects were also observed (Fig. S2(b)†).

To explain the rectified nonvolatile memory effects, we propose the energy band diagrams shown in Fig. 2(d)–(f). If a negative voltage pulse with a large amplitude is applied to V_G, the Fermi level shifts downward, and the tunneling barrier is lowered (Fig. 2(e)). Consequently, holes can tunnel from the WSe_2 channel to the MoS_2 layer through the hBN. However, when V_G returns to 0 V, the tunneling barrier increases again, and the holes become trapped in the MoS_2 layer. The trapped holes shift the Fermi level upward, and the device is switched to the on state at V_{SD} > 0 and to the off state at V_{SD} < 0, as shown in Fig. 1(d). In contrast, if a positive voltage pulse with a large amplitude is applied to V_G, electrons tunnel from the WSe_2 channel to the MoS_2 layer *via* the Fowler–Nordheim tunneling mechanism, and are trapped in the MoS_2 floating gate (Fig. 2(f)), which results in the on state at V_{SD} < 0 and the off state at V_{SD} > 0.

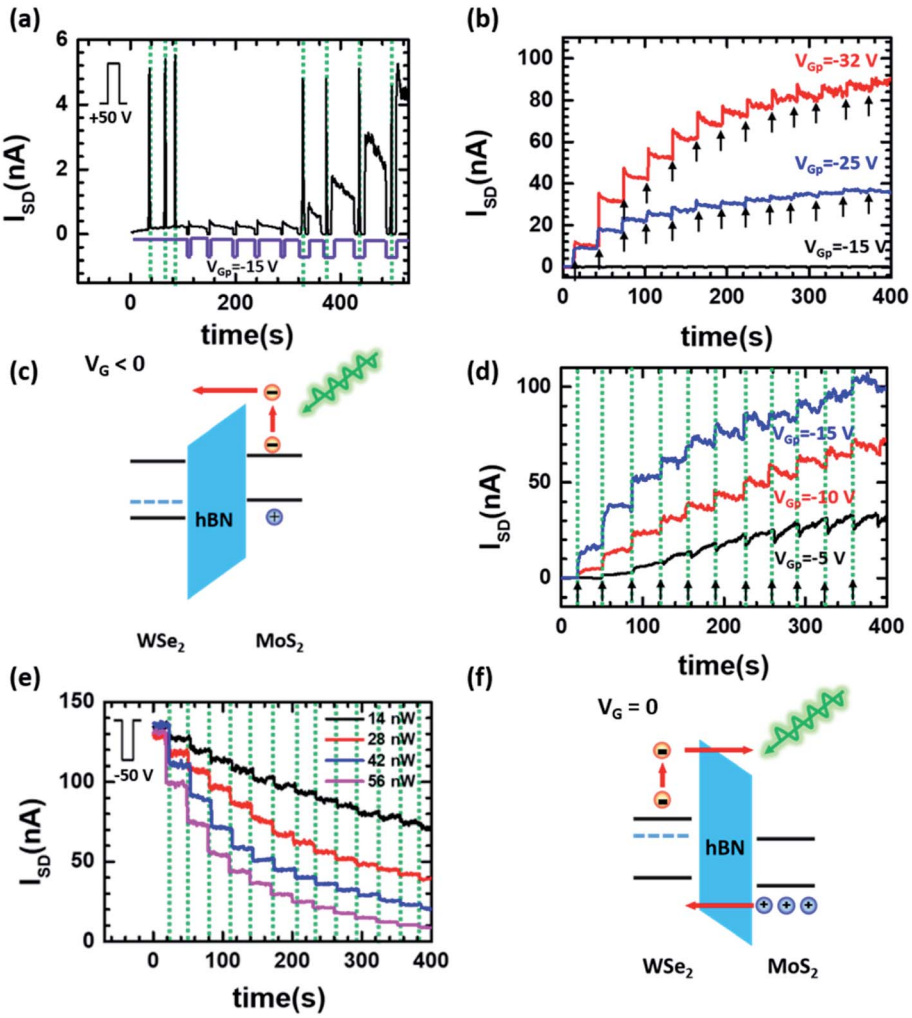

Fig. 3 (a) I_{SD} measured at V_{SD} = +1 V when 532 nm laser pulses, V_{Gp} = −15 V, or 532 nm-laser pulses with V_{Gp} = −15 V were applied after applying V_{Gp} = +50 V. The dotted lines indicate when the laser pulses were applied. (b) I_{SD} measured at V_{SD} = +1 V when V_{Gp} = +50 V was applied to switch the device to the off state and then, V_{Gp} = −15, −25, or −32 V was repeatedly applied. The arrows indicate the time at which V_{Gp} was applied. (c) Energy band diagram proposed to explain the positive stepwise photoconductance. (d) I_{SD} measured at V_{SD} = +1 V when V_{Gp} = +50 V was applied to switch to the off state and then, 532 nm laser pulses (13 nW) and V_{Gp} = −5, −10, or −15 V were simultaneously applied. The dotted lines indicate when the laser pulses were applied, while the arrows indicate the time at which V_{Gp} was applied. (e) I_{SD} measured at V_{SD} = +1 V when V_{Gp} = −50 V was applied to switch the device to the on state and then, 532 nm laser pulses with a pulse width of 0.1 s and different powers were applied every 30 s. The dotted lines indicate the time when the laser pulses were applied. (f) Energy band diagram proposed to explain the negative stepwise photoconductance by light.

Fig. 2(g)–(i) show KPFM images acquired before applying V_{Gp} and after applying $V_{Gp} = -50$ and +50 V, respectively. Positive/negative KPFM signals indicate the accumulation of positive/negative charges,[36,37] and these KPFM images support that the rectified nonvolatile memory effects are attributed to the trapping of holes and electrons in the MoS_2 top floating gate induced by the application of $V_{Gp} = -50$ and +50 V, respectively (Fig. 2(j)).

Optoelectronic performances of a WSe_2/graphene heterostructure with a MoS_2 floating gate

Illumination with laser pulses was reported to induce multilevel memory states in MoS_2-based devices with a floating gate;[9,10] hence, we also investigated whether our WSe_2/graphene device with the MoS_2 top layer exhibited multilevel optical memory effects. First, the device was switched to the off state at $I_{SD} = +1$ V by applying $V_{Gp} = +50$ V, which induced electrons trapped in the MoS_2 layer and led to p-type behaviors. The light pulses were then illuminated (Fig. 3(a)). I_{SD} increased during irradiation but returned to the off state in dark, unlike most reported electronic memory devices, in which I_{SD} increased stepwise upon repeated illumination with laser pulses. In the case of our devices, holes should be trapped in the MoS_2 floating gate to obtain a stepwise increase in I_{SD} at $V_{SD} = +1$ V. These results imply that hole trapping was not induced by illumination. To make holes tunnel from WSe_2 to MoS_2, $V_{Gp} \ll 0$ is required (Fig. 2(e)). When $V_{Gp} = -25$ or -32 V was repeatedly applied, I_{SD} increased in a staircase behavior (Fig. 3(b)). However, when $V_{Gp} = -15$ V was applied, the I_{SD} did not increase at all, implying that the tunneling barrier was not sufficiently lowered by $V_{Gp} = -15$ V.

To facilitate the trapping of holes in the MoS_2 layer, the device was illuminated with 532 nm laser pulses while $V_G = -15$ V was applied (Fig. 3(a)). Although the tunnel barrier is not sufficiently low, electrons are excited upon illumination and can tunnel from the MoS_2 floating gate to the WSe_2 channel (Fig. 3(c)). Consequently, more electrons are released from and holes become trapped in the MoS_2 floating gate, leading to an increase in I_{SD} at $V_{SD} = +1$ V. When the device was irradiated with light pulses with $V_{Gp} = -15$ V, I_{SD} returned to a value higher than the initial value in the dark at $V_G = 0$ V, supporting that photoexcited electrons can tunnel from the MoS_2 layer to the WSe_2 channel by illumination with light pulses and $V_{Gp} = -15$ V. Fig. 3(d) shows I_{SD} measured at $V_{SD} = +1$ V when various values of $V_{Gp} < 0$ and 532 nm laser pulses with a width of 0.1 s and a power of 13 nW were simultaneously applied at the off state. I_{SD} increased stepwise even with $V_{Gp} = -5$ V, indicating that positive stepwise photoconductance can be obtained by the simultaneous application of small negative V_{Gp} and laser pulses. Moreover, these optoelectronic multilevel states were dependent on the laser power and wavelength (Fig. S3†).

Next, the device was switched to the on state at $I_{SD} = +1$ V by applying $V_{Gp} = -50$ V, which induced trapping of holes in the

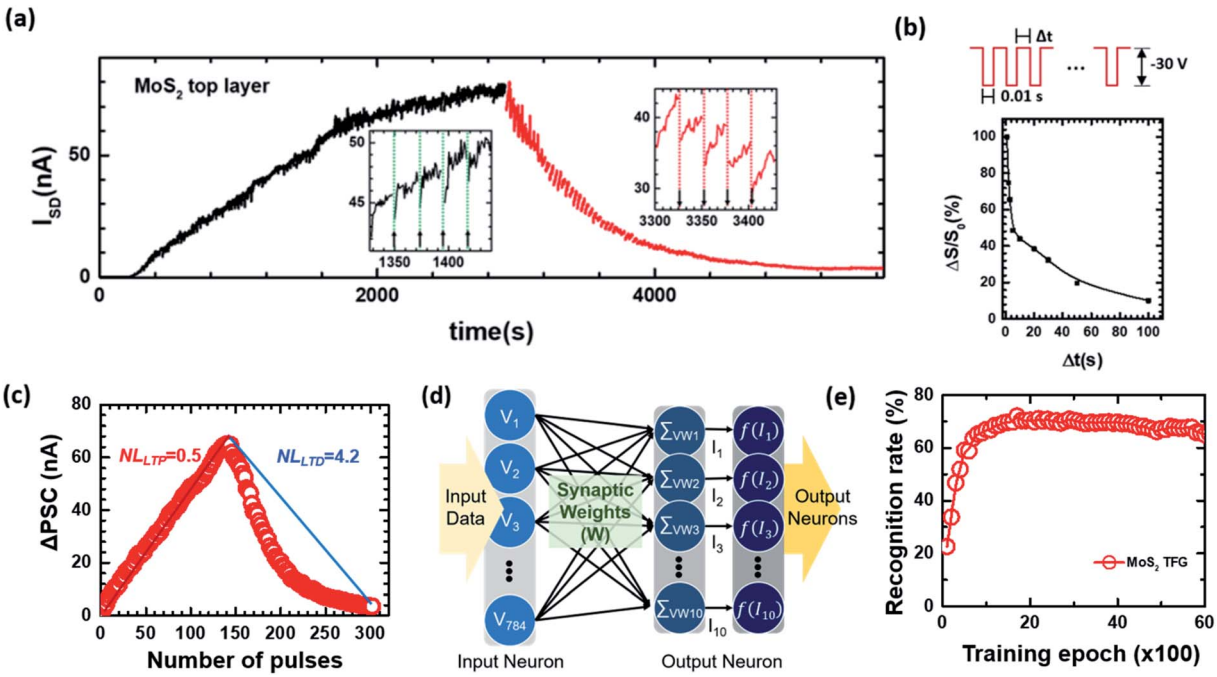

Fig. 4 (a) I_{SD} measured at $V_{SD} = +1$ V for the WSe_2-based device with the MoS_2 top layer when $V_{Gp} = +50$ V was applied to switch the device to the off state and then, potentiation pulses (532 nm laser pulses (54 nW, 1 s) and $V_{Gp} = -10$ V) and depression pulses (635 nm laser pulses (1 nW, 0.03 s) and $V_{Gp} = +11$ V) were repeatedly applied. The insets show enlarged plots. Green and red dotted lines indicate the times when 532 nm and 635 nm laser pulses were applied, respectively, and the arrows indicate when V_{Gp} was applied. (b) Normalized conductance change ($\Delta S/S_0$) measured at $V_{SD} = +1$ V after a 10 pulse train with an amplitude of -30 V and different spacing times (Δt) was applied to V_G, demonstrating spike-rate-dependent plasticity. (c) PSC measured according to number of pulses applied. The NL was estimated to be 0.5 and 4.2 for potentiation and depression, respectively. (d) Schematic of ANN model for analyzing post synaptic learning and recognizing processes of the device. (e) Recognition rate according to the number of learning processes.

MoS_2 layer and led to n-type behaviors. Then, I_{SD} was measured at $V_{SD} = +1$ V, while a 532 nm laser was repeatedly turned on for 0.1 s and then turned off for 30 s (Fig. 3(e)). Interestingly, I_{SD} exhibited a stepwise decrease upon repeated exposure to laser pulses, and it decreased more rapidly with increasing laser power. This negative stepwise photoconductance can be explained by the tunneling of photoexcited electrons from the WSe_2 channel to the MoS_2 floating gate or the tunneling of holes from the MoS_2 floating gate to the WSe_2 channel, because the application of $V_{Gp} = -50$ V lowered the tunneling barrier to allow photoexcited electrons to tunnel from the WSe_2 to the MoS_2 (Fig. 3(f)). Similar measurements were performed upon repeated illumination with laser pulses with different exposure times and wavelengths (Fig. S4†). As the exposure time increased or the laser wavelength decreased, the I_{SD} decreased more rapidly owing to an increase in the number of photoexcited electrons.

To switch the device to the on state at $V_{SD} < 0$, $V_{Gp} = +50$ V was applied, which led to p-type behaviors. Upon repeated illumination with 635 nm laser pulses, the I_{SD} measured at $V_{SD} = -1$ V exhibited a stepwise negative photoconductance (Fig. S5(a)†). In this case, the tunneling barrier was lowered to allow photoexcited electrons to tunnel from the MoS_2 to the WSe_2 (Fig. S5(b)†); thus, illumination with laser pulses resulted in a decrease in $|I_{SD}|$ at $V_{SD} = -1$ V. Although MoS_2 is nearly transparent, more photoexcited electrons might be created in the MoS_2 top layer than in the WSe_2 channel during irradiation. Thus, compared to the results with $V_{Gp} = -50$ V and $V_{SD} = +1$ V, a similar stepwise decrease in I_{SD} was obtained using laser pulses with a longer wavelength.

Application of rectifying optoelectronic memory devices to optoelectronic synapse devices

Fig. 4(a) shows the I_{SD} measured at $V_{SD} = +1$ V, when $V_{Gp} = -10$ V and 532 nm laser pulses (width of 1 s, power of 54 nW) were repeatedly and simultaneously applied after applying $V_{Gp} = +50$ V. I_{SD} exhibited 128 optoelectronic memory states. Subsequently, for depression, $V_{Gp} = +11$ V and 635 nm laser pulses with a width of 0.03 s and a power of 1 nW were simultaneously applied. Although I_{SD} was decreased by 532 nm laser pulses without V_{Gp} (Fig. 3(e)), more symmetric potentiation and depression curves could be obtained by the application of $V_{Gp} = +11$ V and 635 nm laser pulses. Fig. 4(b) shows the normalized conductance change ($\Delta S/S_0$) measured at $V_{SD} = +1$ V after applying a 10-pulse train with an amplitude of -30 V and different spacing times (Δt) to V_G. As Δt decreased, $\Delta S/S_0$ increased, implying that STDP can be realized using this device. We also performed theoretical learning and recognition tasks using an ANN with a size of 784×10 based on the SLP model. The recognition rate was estimated to be

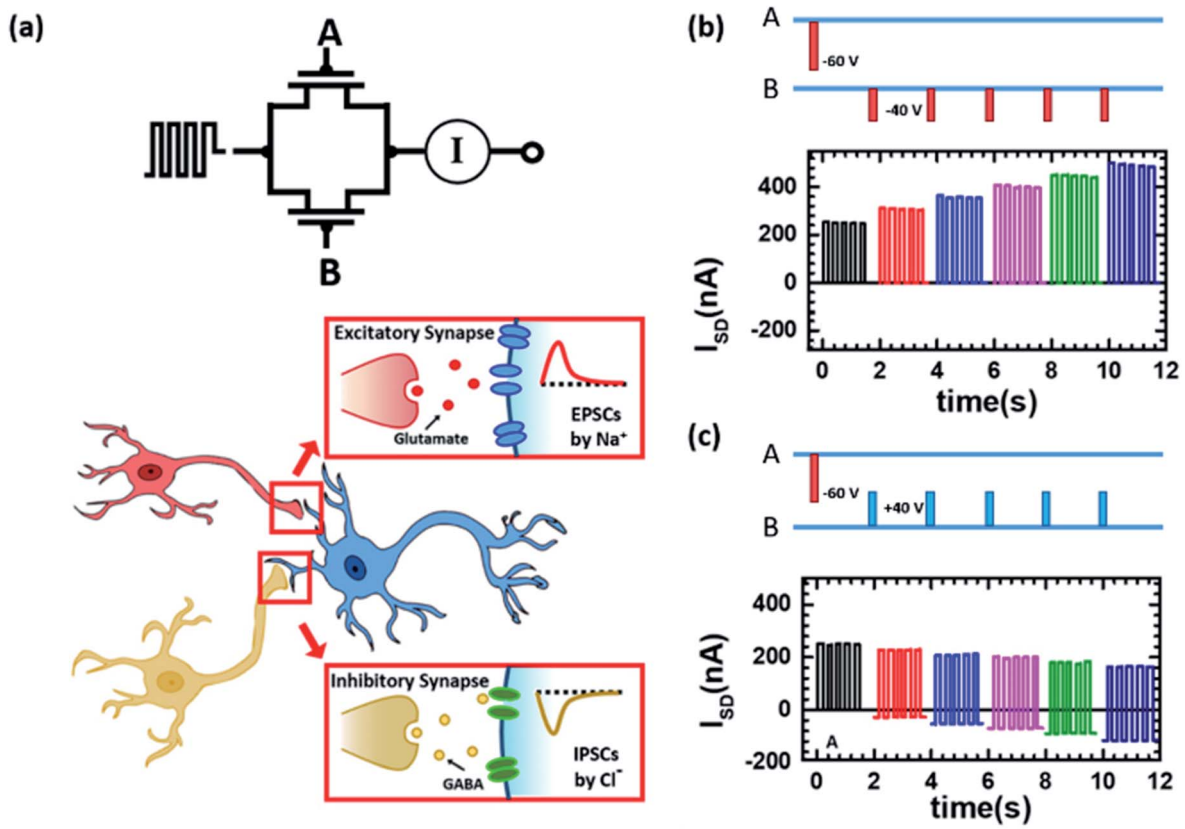

Fig. 5 (a) A circuit consisting of two devices (A and B) connected in parallel (top) and a schematic of excitatory and inhibitory synapses connected to a postneuron (bottom). *I* measured at *V* of ±1 V square waves with a frequency of 5 Hz when $V_{Gp} = -60$ V was applied to device A, followed by repeatedly applying (b) $V_{Gp} = -40$ V or (c) $V_{Gp} = +40$ V to device B.

approximately 72%, which is comparable to the previously reported values (Fig. 4(e)).[38–40]

In addition to the WSe_2/graphene device with the MoS_2 top layer, we fabricated a device with a WSe_2 top layer. It also exhibited gate-tunable rectification inversion, rectified nonvolatile memory properties, and multilevel optoelectronic memory effects (Fig. S6†). Furthermore, quite symmetric and linear potentiation and depression processes could be implemented using single-wavelength laser pulses with different powers (Fig. S7†). The NL was estimated to be 1.0 and 0.6 for potentiation and depression, respectively, which is more symmetric in comparison with the device with the MoS_2 top layer. These results suggest that the linearity and symmetry of the potentiation and depression curves may be improved by controlling the energy band structure.

Application of rectifying memory effects to mimicking excitatory and inhibitory synapses

The indicating that hole or electron tunneling can occur depending on the polarity of V_{Gp} suggests that this device may be applied to mimic excitatory and inhibitory synapses that involve different neurotransmitters. Glutamate is the most common neurotransmitter for excitatory synapses that brings the membrane potential of the postsynaptic neuron toward the threshold for generating action potentials, whereas GABA is the neurotransmitter for inhibitory synapses that drive the membrane potential of the postsynaptic neuron away from the threshold for generating action potentials.[41,42] To explore the feasibility of mimicking excitatory and inhibitory synapses, two similar devices were connected in parallel, as shown in Fig. 5(a). When $V_{Gp} = -60$ or +60 V was applied to both devices, the *I*–*V* curves showed rectifying characteristics with increasing current (Fig. S8(a) and (b)†). However, when $V_{Gp} = -60$ V was applied to one device and $V_{Gp} = +60$ V to the other device, the *I*–*V* curve was almost symmetric (Fig. S8(c)†).

Fig. 5(b) and (c) show *I* measured at *V* of ±1 V square waves when $V_{Gp} = -60$ V was applied to device A, followed by repeatedly applying $V_{Gp} = -40$ and +40 V for 0.1 s to device B, respectively. Upon the application of $V_{Gp} = -60$ V to device A, rectified *I* was measured and its value was nearly unchanged due to the nonvolatile memory effects. Subsequently, when $V_{Gp} = -40$ V was repeatedly applied to device B, *I* gradually increased and the rectifying characteristics were maintained. In contrast, when $V_{Gp} = +40$ V was repeatedly applied to device B, *I* gradually decreased. We also performed similar measurements, in which $V_{Gp} = +60$ V was applied to device A and then $V_{Gp} = -40$ or +40 V was repeatedly applied to device B. Similar behaviors were observed although the polarity of *I* was changed (Fig. S9(a) and (b)†). These results demonstrate that the application of $V_{Gp} = -40$ and +40 V causes effects similar to activating excitatory and inhibitory synapses, respectively.

Conclusions

We fabricated WSe_2/graphene heterostructures with a photoresponsive floating gate of MoS_2 or WSe_2, and investigated their multifunctional properties including gate-controlled rectification inversion, rectified nonvolatile memory effects with an on/off ratio of 10^4 and a retention time $>10^3$ s, and multilevel optoelectronic memory effects. When $V_{Gp} \ll 0$ was applied, the device was switched to the on state at $V_{SD} > 0$ and the off state at $V_{SD} < 0$ as electrons were trapped in the floating gate. In contrast, when $V_{Gp} \gg 0$ was applied, the device was switched to the off state at $V_{SD} > 0$ and to the on state at $V_{SD} < 0$ as holes were trapped in the floating gate. Furthermore, upon repeated illumination with laser pulses, I_{SD} decreased or increased stepwise depending on the history of V_{Gp}, which was ascribed to the tunneling of photoexcited electrons between the WSe_2 channel and the floating gate through the hBN layer *via* the Fowler–Nordheim tunneling mechanism. In particular, 128 optoelectronic memory states with the NL < 1 could be achieved, suggesting that these multifunctional devices can be applied to optoelectronic synapse devices. Learning and recognition tasks were also performed using the ANN based on SLP model and the recognition rate was calculated to be approximately 72%. In addition, we demonstrated that WSe_2/graphene heterostructures with a floating gate may be applied to artificial synaptic devices that emulate inhibitory as well as excitatory synapses.

Experimental section

Device fabrication

Devices were fabricated, as shown in Fig. S10.† First, hBN flakes (15–21 nm) were mechanically exfoliated from an hBN single crystal (HQ graphene) using scotch tape and a selected hBN flake (~11 nm) was transferred onto a SiO_2/Si substrate using a polydimethylsiloxane (PDMS) stamping method. The Au electrode (50 nm) was fabricated using electron-beam lithography and lift-off techniques and the graphene electrode (~15 nm) was made by transferring a graphene flake (HQ graphene) onto the hBN. Next, a WSe_2 flake (~10 nm) was transferred onto the prepared electrodes, resulting in a WSe_2 field-effect transistor (FET). After heating at 85 °C for 30 min on a hot plate, the FET was characterized. Subsequently, hBN (~11 nm) and MoS_2 (~11 nm) flakes were transferred onto the WSe_2 FET, and polystyrene was spin-coated to improve the contact between the vdW materials. WSe_2 and MoS_2 flakes were exfoliated from commercially available crystals (2D semiconductors).

Measurements

To characterize their optoelectronic properties, the devices were placed in a homemade vacuum chamber with an optical window. Electrical measurements were carried out using a semiconductor characterizer (4200-SCS, Keithley). Laser pulses were applied through the optical window and the exposure time was controlled using an optical shutter (SB5/M Aperture and SC10 controller, Thorlabs). SKPM images were acquired using an atomic force microscope (Park NX10, Park System) with a Cr–Au conducting cantilever.

Weight update method

A large-scale neural network with a size of 784 × 10 were constructed theoretically based on the single-layer perceptron model. The hand-written images of the MNIST database were pixelated with 255 levels of black and white contrast and then input as a form of a voltage matrix ($V_1 - V_i$, V). This input voltage was multiplied by a synaptic weight vector ($W_{1,1} - W_{i,j}$, W) to be converted to an output current vector ($I_1 - I_j = \sum V_i \times W_{ij}$). Here, the synaptic weight refers to the difference ($W = G^+ - G^-$) between the conductance state of potentiation (G^+) and depression (G^-) regions of the LTP/LTD curve. Next, the net current (net_j) collected at the output neuron was converted using the sigmoid function ($f(\text{net}_j)$) to have values between "0" and "1". The $f(\text{net}_j)$ was then subtracted to a label value (k_j) to define the weight-update determining factor 'δ_j' ($\delta_j = k_j - f(\text{net}_j)$). Finally using a sign function, when $\text{sgn}(\delta_j \times V_i)$ was positive, we increased the synaptic weight between i_{th} input neuron and j_{th} output neuron and decreased the corresponding synaptic weights when $\text{sgn}(\delta_j \times V_i)$ was negative. Finally, weight update was not processed when $\text{sgn}(\delta_j \times V_i)$ is 0.

Author contributions

S. H. Kim proposed the idea, design the experiments and wrote the manuscript, M. U. Park, C. J. Lee and S. G. Yi helped perform electric and optical measurements, M. Kim helped optimize the scheme and figures and Y. Choi performed the SLP simulation.

Conflicts of interest

There are no conflicts to declare.

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