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A wafer-scale synthesis of monolayer MoS_2 and their field-effect transistors toward practical applications

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Molybdenum disulfide (MoS_2) has attracted considerable research interest as a promising candidate for downscaling integrated electronics due to the special two-dimensional structure and unique physicochemical properties. However, it is still challenging to achieve large-area MoS_2 monolayers with desired material quality and electrical properties to fulfill the requirement for practical applications. Recently, a variety of investigations have focused on wafer-scale monolayer MoS_2 synthesis with high-quality. The 2D MoS_2 field-effect transistor (MoS_2-FET) array with different configurations utilizes the high-quality MoS_2 film as channels and exhibits favorable performance. In this review, we illustrated the latest research advances in wafer-scale monolayer MoS_2 synthesis by different methods, including Au-assisted exfoliation, CVD, thin film sulfurization, MOCVD, ALD, VLS method, and the thermolysis of thiosalts. Then, an overview of MoS_2-FET developments was provided based on large-area MoS_2 film with different device configurations and performances. The different applications of MoS_2-FET in logic circuits, basic memory devices, and integrated photodetectors were also summarized. Lastly, we considered the perspective and challenges based on wafer-scale monolayer MoS_2 synthesis and MoS_2-FET for developing practical applications in next-generation integrated electronics and flexible optoelectronics.

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1. Introduction

In recent years, 2D transition metal dichalcogenides (TMD), especially molybdenum disulfide (MoS_2), have attracted widespread attention for a variety of next-generation electronic and optoelectronic device applications.[1–3] Compared with conventional silicon-based semiconductors, monolayer MoS_2 is envisioned as an alternate building block for the next-generation electronic device and integrated circuit with short channel, thin thickness, small volume, light weight, fast speed, and high sensitivity.[4–12] However, it is still very challenging to achieve large-area, high-quality MoS_2 for practical applications. Since the traditional mechanical exfoliation method is difficult to

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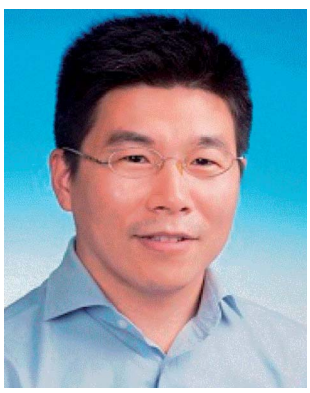

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meet the needs of wafer-scale MoS_2 synthesis in terms of the yield, size, thickness, and uniformity, most MoS_2 investigations synthesis have focused on developing the vapor phase growth of monolayer MoS_2.[13–15] Generally, synthetic methods for large-area monolayers and few-layer MoS_2 films include traditional chemical vapor deposition (CVD), thin film sulfurization, metal–organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), and vapor–liquid–solid (VLS) method.[16–28] Due to the development of synthetic methods, the large-area, high-quality continuous monolayer MoS_2 films have been successfully reported, with a wafer-scale even up to 8 inch,[18] suggesting great potential in integrated devices compatible with silicon-based micro-fabrication processes.

In the past decade, 2D MoS_2 with atomic thickness is considered one of the most promising candidates for the downscaling trend in integrated electronics, which leads to continuing demands for minimizing the channel thickness. The wafer-scale 2D MoS_2 films can be reliably transferred and heterogeneously integrated onto a variety of substrates with the aid of polymethyl methacrylate (PMMA) or olydimethylsiloxane (PDMS), demonstrating many important applications in environment-friendly transient devices.[11–13,31] Since the fabrication process of wafer-scale MoS_2-based devices can be more compatible with the traditional complementary metal oxide semiconductor (CMOS) fabrication process, many investigations have focused on developing wafer-scale monolayer MoS_2 and high-performance MoS_2 field-effect transistors (MoS_2-FET) to significantly promote their future device applications, especially electronic and optoelectronic applications.[11–13] The fabricated MoS_2-FET have achieved attractive performance with high on/off ratios up to 10^{10} and a high mobility of about 167 ± 20 $cm^2\ V^{-1}\ s^{-1}$.[13,14] Even though the reported field effect mobility of MoS_2-FET is still behind that of Si-based transistors, explorations are promising to advance one step further from a single MoS_2-FET to complex devices, such as basic logic gate circuits, basic memory devices, and integrated phototransistors. With the development of MoS_2 synthesis and FET techniques, 2D MoS_2 would play a great role in next-generation integrated circuits and flexible electronics.

In this review, we focus on wafer-scale synthesis of monolayer MoS_2 film and the high-performance MoS_2-FET toward practical applications. We first introduce the recent progresses in MoS_2 synthesis by different methods, including Au-assisted exfoliation, CVD, thin film sulfurization, MOCVD, ALD, VLS method, and the thermolysis of thiosalts. Then, an overview of the MoS_2-FET developments will be provided based on different device configurations. The basic characterization and device performance of different MoS_2-FET will also be summarized. Furthermore, we will present recent advances in applications of logic circuits, memory devices, and photodetectors based on 2D wafer-scale monolayer MoS_2 and MoS_2-FET. Lastly, we will discuss the perspective and challenges based on wafer-scale MoS_2 synthesis and MoS_2-FET for developing practical applications in integrated electronics and flexible optoelectronics. The recent advances in monolayer MoS_2 synthesis and MoS_2-FETs emphasize the opportunity and potential of the wafer-scale MoS_2 in terms of achieving the practical application in modern large-scale integrated devices based on the existing silicon-based micro-fabrication processes.

2. Wafer-scale MoS_2 synthesis

2D MoS_2 film can be synthesized by the top-down strategy and the bottom-up strategy. In the top-down strategy, the commercialized MoS_2 bulk crystal is physically peeled into the monolayer or few-layer MoS_2 flakes by mechanical exfoliation methods. In the bottom-up strategy, the MoS_2 film is prepared through chemical reaction on a specific substrate by CVD, MOCVD, ALD, *etc.* In order to realize wafer-scale monolayer MoS_2 synthesis, continuous efforts have been made to develop the synthetic method and synthetic system based on the top-down strategy and the bottom-up strategy.

2.1 Au-assisted exfoliation method

Due to the unique layered geometry and van der Waals (vdW) interactions in 2D materials, mechanical exfoliation provides a low-cost way to produce the monolayer and few-layer highly crystalline layered 2D materials. In a typical mechanical exfoliation process, appropriate thin MoS_2 crystals were first peeled off from the bulk crystal using adhesive scotch tape and then transferred onto a target substrate. After the scotch tape is removed, monolayer or few-layer MoS_2 can be obtained on the substrate. Generally, the sizes and thicknesses of 2D MoS_2 from scotch-tape exfoliation are limited, which is not suitable for mass-production and scaled-up applications. Gold is known to have a strong affinity for sulfur and can be exploited to exfoliate monolayer from the bulk crystal as a result of strong vdW interactions between Au and the topmost MoS_2 layer.[26–28]

Recently, Liu *et al.*[29] developed a facile method by developing ultraflat gold layers on polymer supports to disassemble vdW single crystals layer by layer into monolayers with near-unity yield, which can be applied to a broad range of vdW single crystals on various substrates. The ultraflat gold film on a polymer substrate was first evaporated on an ultraflat surface with an Å scale roughness and was then stripped off the substrate with a thermal release tape and an interfacial layer. Due to the intimate and uniform vdW contact between the ultraflat gold and 2D vdW crystal surface, a complete monolayer was exfoliated from the crystal and transferred onto the desired substrate. After removing the thermal release tape and the interfacial layer, the gold was etched in a mild etchant solution (I_2/I^-), resulting in a large-area monolayer film. In the Au-assisted method, MoS_2 monolayer in the centimeter scale was exfoliated from the bulk crystal and the dimensions are only limited by bulk crystal sizes. Similarly, Huang *et al.*[30] reported a universal Au-assisted exfoliation of large-area 2D crystals, as shown in Fig. 1. Firstly, a thin layer of Au was deposited onto a substrate covered with a thin Ti or Cr adhesion layer. Then, a freshly cleaved layered bulk crystal on tape was brought in contact with the Au layer with a gentle pressure applied to establish a good layered crystal/Au contact. One or few large-area monolayer flakes were left on the Au surface after peeling off the tape and removing the major portion of the crystal.

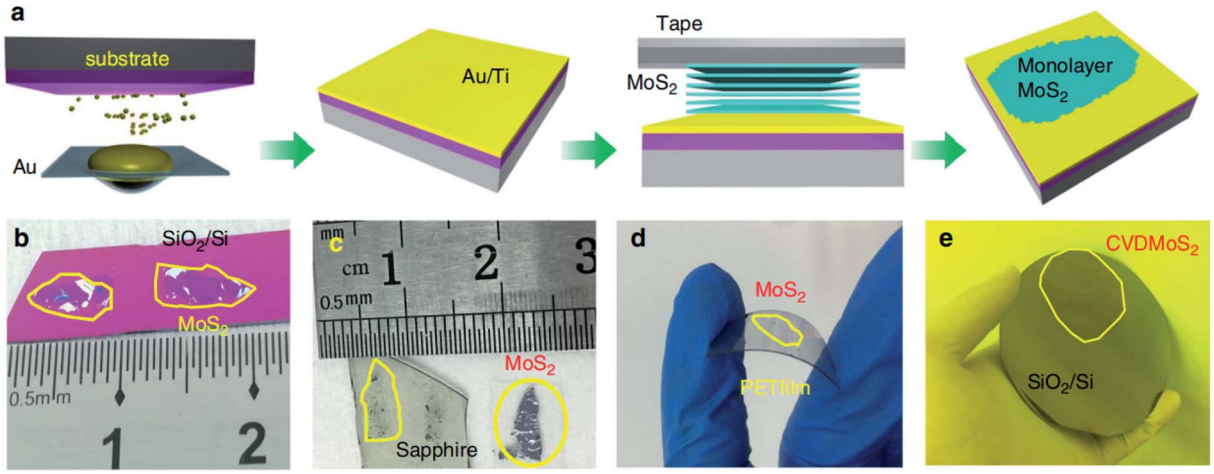

Fig. 1 Mechanical exfoliation of different monolayer materials with macroscopic size. (a) Schematic of the exfoliation process. (b–d) Optical images of exfoliated MoS_2 on SiO_2/Si, sapphire, and plastic film. (e) 2-inch CVD-grown monolayer MoS_2 film transferred onto a 4-inch SiO_2/Si substrate.[30] Reproduced with permission from ref. 30, copyright 2020 Springer Nature.

Limited only by the size of the available bulk crystals, these monolayer flakes are usually macroscopic with a size in millimeters. This method can also be applied to CVD-grown wafer-scale MoS_2 and the exfoliated monolayer flakes can be intactly transferred onto arbitrary substrates after removing the gold layer by the KI/I_2 etchant.

2.2 CVD method

In the traditional CVD synthesis of 2D MoS_2, the solid-state precursors of MoO_3 powder and sulfur (S) powder were first evaporated into gaseous states and then reacted with each other in a low-pressure chamber, and MoS_2 nuclei formed and gradually enlarged into grains with the aid of carrier-gas flow on the downstream substrates. To achieve large-area continuous monolayer MoS_2 films, many efforts have been devoted for improving the CVD synthesis of 2D MoS_2, as shown in Fig. 2.[31–41]

One strategy is to overcome the CVD setup limitations. Yu *et al.*[31] reported a three-temperature-zone CVD system that employs independent carrier gas pathways for sulfur and MoO_3 sources to successfully fabricate 2-inch wafer-scale uniform monolayer MoS_2 films on sapphire. During the growth, the temperatures for the sulfur source, MoO_3 source, and wafer substrate are 115, 930, and 530 °C, respectively, with a typical growth duration of 40 min. Xu *et al.*[32] reported an improved wafer-scale growth of continuous MoS_2 film based on atmospheric pressure within a two-temperature-zone CVD setup. As low pressure of 300 Pa can effectively promote the evaporation rate and provide a uniform concentration of the gaseous precursor in the tube to increase the lateral growth rate; thus, a uniform and continuous monolayer MoS_2 film can be achieved by increasing the sulfurization time to 15 min. Recently, Wang *et al.*[33] realized the epitaxy of highly oriented and large-domain monolayer MoS_2 films at a 4-inch wafer scale *via* a facile multisource CVD growth method. In this setup, MoO_3 sources are evenly loaded within the six minitubes and the S source is loaded within the center minitubes. The carrier gases for S and MoO_3 sources are independently delivered through the minitubes. This multisource design provides homogeneous cross-sectional source supply, leading to uniform growth with only 0° and 60° oriented domains and domain size >180 μm. He *et al.*[34] demonstrated a layer-by-layer scalable growth of MoS_2 films on a moving sapphire substrate by local-feeding atmospheric-pressure CVD. By the linear moving of the substrate across the cone-shaped diffusion concentration gradient of Mo-containing species and controlling the moving cycles, large-scale growth, uniform monolayer, and few-layer MoS_2 with sizes up to ~4.7 cm × 6 mm can be obtained. The 4-, 7-, and 9-cycle growth corresponding to dwelling times of 8, 14, and 18 min can form complete monolayer, bilayer, and trilayer MoS_2 films, respectively. Durairaj *et al.*[35] utilized SiO_2 as a mechanical barrier to moderate the Mo flux so as to allow better controllability and high position selectivity for the CVD growth of homogeneous MoS_2 monolayers. The barrier offered great control in controlling the Mo precursor vapor concentration at the substrate position, mitigating the secondary and intermediate phases as well as second layer nucleation, thus leading to a continuous monolayer with high surface homogeneity.

Another strategy for improving the CVD synthesis is to adjust the precursor or the substrate. Aside from elemental sulfur powder, hydrogen sulfide (H_2S) gas has also proven to be a good sulfur source, which exhibits high vulcanization ability. Liu *et al.*[36] demonstrated that a reproducible and low-cost method for growing wafer-scale (approximately 9.5 × 4.5 cm^2) high-quality monolayer MoS_2 by using H_2S gas as the sulfur source and to stabilize the sulfur vapor pressure during the growth process. In addition, two independent carrier gas pathways for H_2S and MoO_3 sources were employed to prevent MoO_3 poisoning and achieve an improved and stable growth condition. Yang *et al.*[37] reported the epitaxial growth of wafer-scale single-crystal MoS_2 monolayers on vicinal Au(111) thin film by a facile ambient-pressure CVD with MoO_3 and S as the

precursors. Single-crystal Au(111) substrate was obtained by melting and resolidifying the commercial Au foils at a designated temperature (~1050 °C) for 10 min on cleansed W foils. During the growth, the unidirectional oriented MoS_2 domains on the Au(111) film with an area of ~3 × 3 cm^2 started to merge and eventually coalesced into a continuous film after 8 min at ~720 °C.

Besides these planer substrates, 2D MoS_2 can also be synthesized on non-planar substrates. Liao *et al.*[42] firstly proposed single-crystal monolayer MoS_2 growth on tapered silica micro/nanofibers

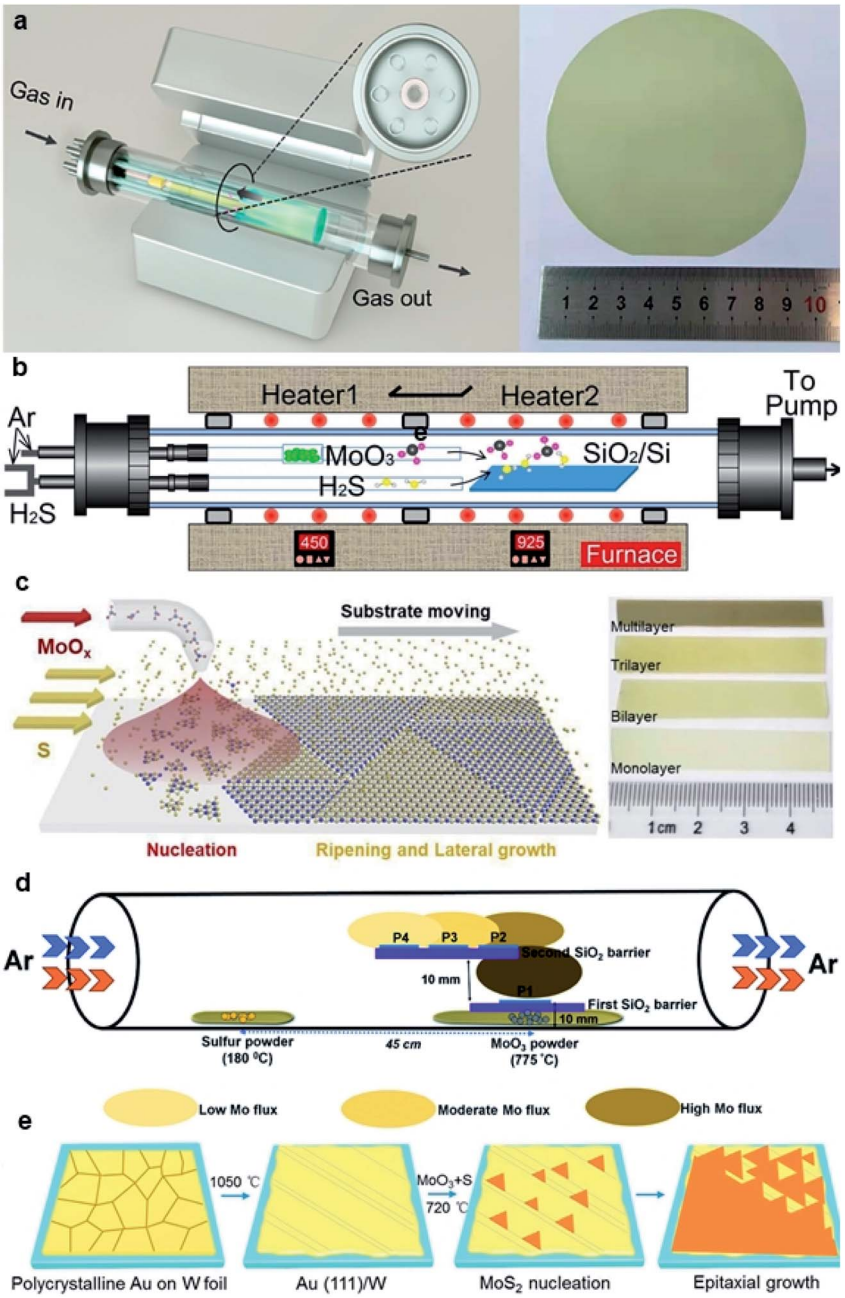

Fig. 2 (a) Schematic diagram of the multisource CVD setup and the photograph of a 4-inch sapphire wafer uniformly covered by the monolayer MoS_2 film;[33] reproduced with permission from ref. 33, copyright 2020 American Chemical Society. (b) Schematic illustration of a homemade two-temperature zone CVD setup and the as-synthesized monolayer MoS_2 film;[36] reproduced with permission from ref. 36, copyright 2020 IOP Publishing, Ltd. (c) Schematic diagram of substrate-moving atmospheric pressure CVD and the photograph of large-scale MoS_2 films;[34] reproduced with permission from ref. 34, copyright 2019 IOP Publishing, Ltd. (d) Schematic of the experimental setup showing the side-view geometry of the stair-case-like barrier with different substrate positions and the images for the MoS_2 sample were acquired from P2;[35] reproduced with permission from ref. 35, copyright 2020 The Royal Society of Chemistry. (e) Schematic illustration of Au(111) formation and the MoS_2 growth process, and the photograph of a CVD-grown MoS_2 monolayer on the Au(111)/W foil substrate (area ~3 × 3 cm^2).[37] Reproduced with permission from ref. 37, copyright 2020 American Chemical Society.

(MNFs) and realized photoluminescence (PL) enhancement by high-density oxygen dangling bonds released from the tapered MNFs surface, as shown in Fig. 3. The monolayer MoS_2 grown on silica MNF exhibits a PL quantum yield from ~30% to 1% in a wide pump intensity range from 10^{-1} to 10^{4} W cm^{-2} at room-temperature. Due to the taper-drawing process and high-intensity light irradiation, the Si–O bonds of silica can be broken directly and high-density oxygen dangling bonds can be released on the MNFs surface. These reactive oxygen dangling atoms then fill the sulfur vacancies or bridge with neighboring sulfur atoms in monolayer MoS_2, forming stable localized sites through electron transfer in MoS_2. Thus, the taper-drawing process and high-intensity light irradiation process will reduce the non-radiative carrier-recombination centers and strongly enhance the PL of the monolayer MoS_2 in a wide pump dynamic range at room temperature. These unique advantages based on the taper-drawing process enable the direct realization of low-threshold lasing without high-quality factor optical microcavities, which demonstrated great potential in different optical and optoelectronic applications.[42–44]

2.3 Thin film sulfurization method

Large-area 2D MoS_2 with excellent uniformity can be obtained by sulfuring the deposited Mo or MoO_x in a chamber with a sulfur-rich environment. This thin film sulfurization method refers to a two-step process, namely, thin film deposition and the followed sulfurization, which is also classified into two-step CVD methods. As shown in Fig. 4, the Mo precursors can be deposited by various deposition techniques, including electron-beam evaporation, pulsed laser deposition, magnetron sputtering, spin-coating, and ALD. The sulfur source includes S vapor, H_2S, and carbon disulfide (CS_2).

Kim *et al.*[45] demonstrated wafer-scale 2D MoS_2 growth *via* the sulfurization of transition metals deposited on the SiO_2/Si substrates using a home-built chamber. High-quality molybdenum (Mo) was deposited on cleaned SiO_2/Si wafers with a typical dimension of 1×3 cm^2 using an e-beam evaporation system and then placed at the center zone of the CVD furnace for sulfurization by sulfur vapor at 800 °C. Jo *et al.*[46] developed the two-step synthesis of large-area MoS_2 thin film by depositing Mo metal films by electron-beam and sulfurizing the Mo film in mixtures of H_2S and O_2 gas. It was found that the presence of trace levels of O_2 accelerates the crystallization of MoS_2 and affects the layer orientation, without changing the kinetics of mass transport or the final film composition. Large-area MoS_2 films grown on 2-inch wafer, Al, glass, and indium tin oxide (ITO) at 400 °C were realized by this two-step method. Recently, Park *et al.*[47] fabricated MoS_2 device arrays constructed on large-dimensional MoS_2 films grown using a radio-frequency (RF) magnetron sputtering deposition method combined with post-treatment processes. High-quality centimeter-scale trilayer MoS_2 was achieved by sputtering, EBI, and sulfurization. The post-treatments that rearrange the atoms in the MoS_2 films can result in an improvement of the MoS_2 crystallinity. Almeida *et al.*[48] presented wafer-scale MoS_2 growth at arbitrary integer layer number by a technique based on the decomposition of CS_2

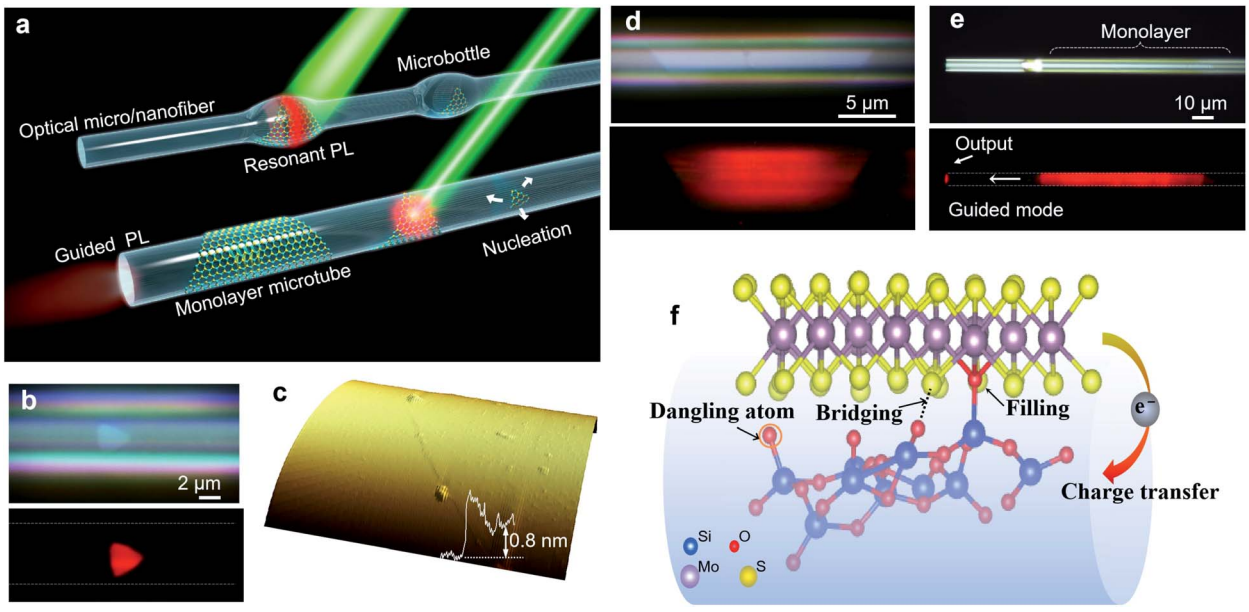

Fig. 3 Monolayer MoS_2 grown on MNFs. (a) Conceptual illustration of monolayer MoS_2 grown on MNFs with uniform diameters and with microbottle structures. A single-crystal triangular domain first nucleates on the MNF surface and then laterally grows into a large-area monolayer structure. A 532 nm CW laser is used to excite the PL emissions. (b) Optical and PL images of a triangular layered MoS_2 on a microfiber ($D_{fiber} = 6.1$ μm) with (c) a thickness of ~0.8 nm, as confirmed by an AFM scan. (d) Optical and PL images showing the clean surface and two sharp boundary edges of the MoS_2 monolayer/microfiber structure ($D_{fiber} = 5.5$ μm). (e) Optical and PL images showing a large-area monolayer/microfiber ($D_{fiber} = 5.4$ μm). Some guided emission is emitted at the distal end of the microfiber. (f) The generated oxygen dangling atoms can fill the sulfur vacancies, bridge with neighboring sulfur atoms, and form localized sites by transferring electrons from MoS_2, leading to enhanced PL emission.[42] Reproduced with permission from ref. 42.

on a hot Mo filament. As CS_2 molecules decompose at the Mo filaments, MoS_x precursors evolve, evaporate from the rods, and deposit onto the substrate at 650 °C, where they obtain stoichiometric sulfur contents from the environmental CS_2 and form into extended islands or evaporate again. Since the hue value of light from the hot Mo filaments reflected from the wafer substrate changes as the film grows layer by layer, the concomitant measurement of this hue was employed to control the growth process, which allows the precise targeting of any integer layer number.

Besides Mo films, oxidized Mo film is also a precursor source in the sulfurization method. Choi *et al.*[49] synthesized the 2-inch-scale

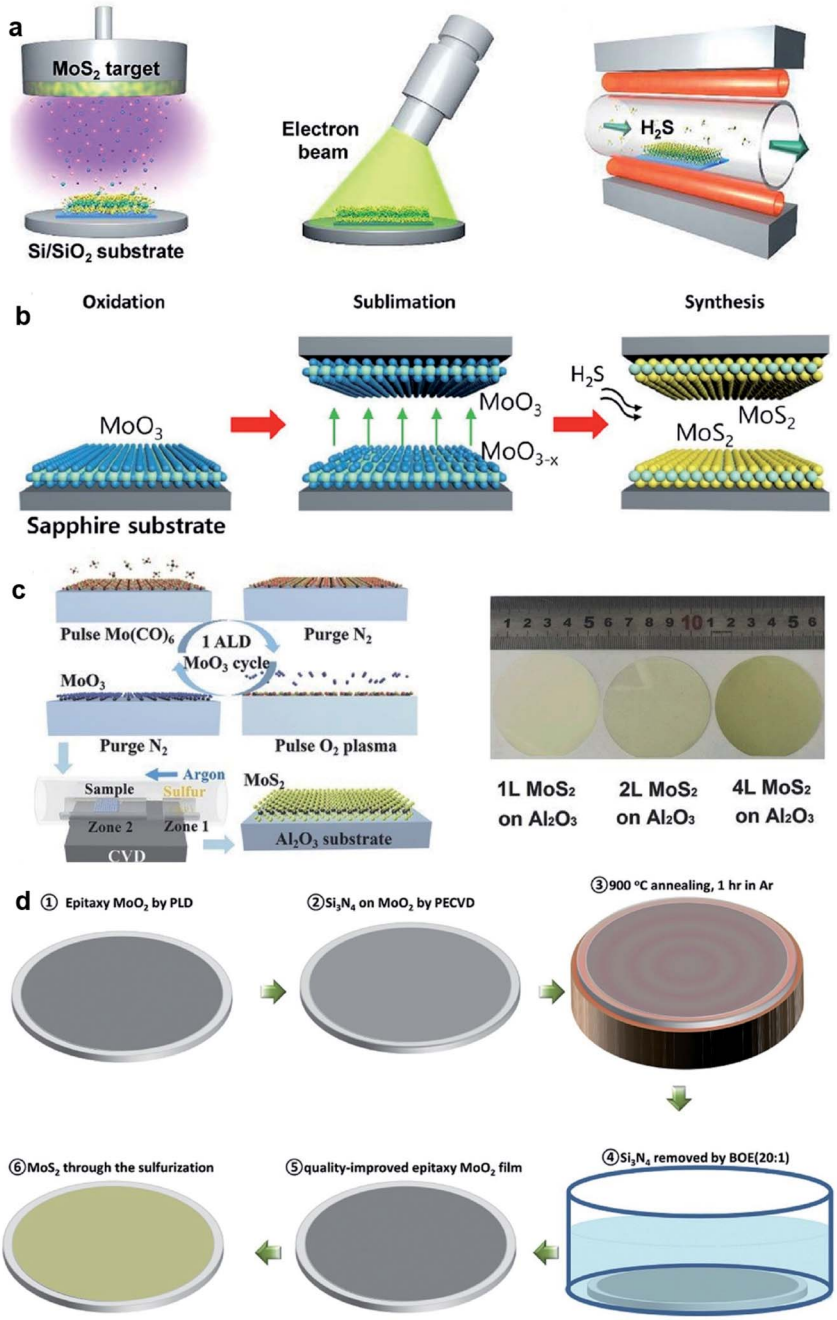

Fig. 4 (a) Schematic illustration of the synthetic process of the MoS_2 film: sputtering, EBI treatment, and sulfurization;[47] reproduced with permission from ref. 47, copyright 2020 American Chemical Society. (b) Schematic illustrations of the reaction sequence of monolayer MoS_2 *via* proximity evaporation of the Mo film precursor with the three steps (oxidation, sublimation, and synthesis);[49] reproduced with permission from ref. 49, copyright 2020 American Chemical Society. (c) Schematic of one cycle ALD process for the MoO_3 film and the sulfurization process for MoS_2, and the photo of the MoS_2 film on a 2-inch sapphire wafer;[52] reproduced with permission from ref. 52, copyright 2017 John Wiley and Sons. (d) Flow diagram showing the synthesis of single-crystal MoS_2 films converted from CLAP-treated precursor MoO_2 films.[51] Reproduced with permission from ref. 51, copyright 2020 John Wiley and Sons.

monolayer MoS_2 film using an atmospheric pressure reaction process as the result of the reaction between the oxidized Mo and gaseous H_2S at a peak temperature of 780 °C. The growth is based on a unique reaction mechanism due to the self-limiting precursor source in a proximity reaction environment with a distance of only ~0.5 mm from the reaction zone, which provides a unique advantage of uniformity with the self-limiting reaction due to the limited MoO_{3-x} supply. Xu *et al.*[50] realized high-quality MoS_2 synthesis over 2-inch wafers through the two-step vapor-solid phase reaction (VSPR) process using MoO_2 as the precursor. The epitaxial MoO_2 film was firstly deposited on 2-inch wafers by pulsed laser deposition (PLD), then loaded into a tube furnace and annealed in a mixture of Ar and S at 900 °C for 1 h at low pressure, resulting in 2D epitaxial MoS_2 films. This quasi-single-crystalline MoS_2 film deposited over the 2-inch wafer was ~3 nm in thickness and can be successfully transferred onto different substrates. Xu *et al.*[51] introduced a new capping layer annealing process (CLAP) to improve the crystalline quality of the as-deposited MoO_2 films and minimized its defects in the synthesis of single-crystalline MoS_2 films on 2-inch wafers. The epitaxial MoO_2 sample was covered with a protective capping layer, such as SiO_2 or Si_3N_4 with a thickness of 50 nm, and then annealed in the PLD chamber at 900 °C for 1 h. After annealing, the capping layer on MoO_2 can be totally removed by buffered oxide etching (20 : 1) solution. Through the sulfurization of the CLAP-treated epitaxial MoO_2 film in a CVD system with sulfur powder source, wafer-scale single-crystalline MoS_2 films were obtained without texture. The MoO_3 films with desired thickness deposited by ALD is a good candidate for the Mo source in the thin film sulfurization method. Shi *et al.*[52] demonstrated the two-step growth of MoS_2 on sapphire substrates by depositing the MoO_3 film by ALD using $Mo(CO)_6$ and oxygen plasma as the precursors. The MoO_3 film was sulfurized at 500 °C for 20 min, and followed by 20 min annealing at 900 °C in the sulfur vapor to improve the crystallinity of MoS_2.

2.4 MOCVD method

The MOCVD technique using metal–organic sources (as shown in Fig. 5), such as $Mo(CO)_6$ and $(C_2H_5)_2S$, is generally favorable due to highly uniform and accurately layer-controlled, thus avoiding the need for post-deposition treatment and benefiting large-area MoS_2 synthesis.[53–55] Mun *et al.*[21] reported the kinetics-controlled low-temperature MOCVD method for the direct growth of spatially homogeneous 2D MoS_2 film on a polyimide (PI) substrate at a record low process temperature of 250 °C with the precursors of $Mo(CO)_6$ and high-purity H_2S. As an alkali-metal catalyst, sodium chloride (NaCl) was precisely controlled in the MOCVD reactor along with the growth substrate. It takes 8 h to successfully obtained 4-inch scale monolayer MoS_2 film on PI at 250 °C by the precise and continuous feeding of the alkali-metal catalyst during the MOCVD process. The fabricated flexible MoS_2-FET based on directly grown MoS_2 demonstrate the excellent stability of the electrical properties following a 1000-cycle bending test with a 1 mm radius. Kalanyan *et al.*[53] presented MoS_2 film growth by pulsed MOCVD in a single-wafer reactor using the precursors of $(NtBu)_2(NMe_2)_2Mo$ and Et_2S_2. Each reaction cycle consisted of 1.5 s co-injections of $(NtBu)_2(NMe_2)_2Mo$ centered on 2 s injections of Et_2S_2 and then the reactor was purged with 400 sccm Ar for 4 s, resulting in a 6 s cycle time. Pulsed injections of the precursor vapors facilitated excellent control over the film thickness with a growth rate of 0.12 nm/pulse. The layered wafer-scale MoS_2 films with thickness from ~1 nm to ~25 nm on the SiO_2/Si substrates can be achieved at comparatively low reaction temperatures of 591 °C at short deposition times, from tens of seconds to several minutes. Shinde *et al.*[54] proposed a gas-phase CVD approach for the synthesis of atomically thin MoS_2 films over 2-inch sapphire wafers with suitable precursors of $(NtBu)_2(NMe_2)_2Mo$ and hydrogen sulfide (H_2S). A graphite susceptor was designed for handling a 2-inch wafer facing at a 15° angle to the Ar gas flow. The homogeneous MoS_2 films was obtained at 850 °C under 10 Torr with an H_2S flow of 3 sccm. In this approach, the growth rate of continuous MoS_2 was found to be 1 monolayer (S–Mo–S) per 4 min. Recently, Shinde *et al.*[55] also realized the rapid and large-scale fabrication of the MoS_2 layers directly on SiO_2/Si (3.5×3.5 cm^2) using $(NtBu)_2(NMe_2)_2Mo$ and H_2S *via* gas-phase CVD. The seamless growth process allowed the deposition of monolayer MoS_2 films in 4 min with excellent spatial homogeneity and optical quality.

Cun *et al.*[56] developed the wafer-scale growth of high-quality monolayer MoS_2 on single crystalline sapphire and SiO_2 substrates at the 2-inch wafer scale by a facile MOCVD with a spin-coated Mo precursor and a non-toxic sulfur precursor. An aqueous solution of sodium molybdate (Na_2MoO_4) was provided as the Mo precursor by spin-coating on the substrates prior to the growth, and the amount of Mo can be controlled by the concentration of Na_2MoO_4 and the spin-coating speed. The single sulfur precursor was supplied by the non-toxic liquid organic compound diethyl sulphide $(C_2H_5)_2S$, which is stored in a stainless-steel bubbler and connected to the quartz tube with a mass flow controller (MFC) to precisely control the amount of the required sulfur precursor during the growth. The obtained wafer-scale MoS_2 films exhibit crystallinity and good electrical performance.

Seol *et al.*[57] realized high-throughput production of 6-inch wafer-scale monolayer MoS_2 and WS_2 *via* a pulsed MOCVD technique. A scalable shower-head-type cold-wall reactor system was used and the gas-phase precursors included molybdenum hexacarbonyl ($Mo(CO)_6$), $(C_2H_5)_2S$, and H_2. Each reaction cycle consisted of 2 min of co-injection of all the precursors, followed by interrupting the precursors' supply and purging with N_2 for 1 min. Periodic interruption of the precursor supply allowed the successful regulation of secondary nucleation even under high growth rates; as a result, wafer-scale monolayer MoS_2 and WS_2 were obtained within 12 min on 6-inch quartz substrates. Moreover, the as-grown TMD films show excellent spatial homogeneity and well-stitched grain boundaries, enabling facile transfer to various target substrates without degradation.

2.5 Vapor–liquid–solid (VLS) method

The reported CVD of 2D MoS_2 is generally conducted through a typical vapor–solid–solid mechanism or a vapor–gas–solid

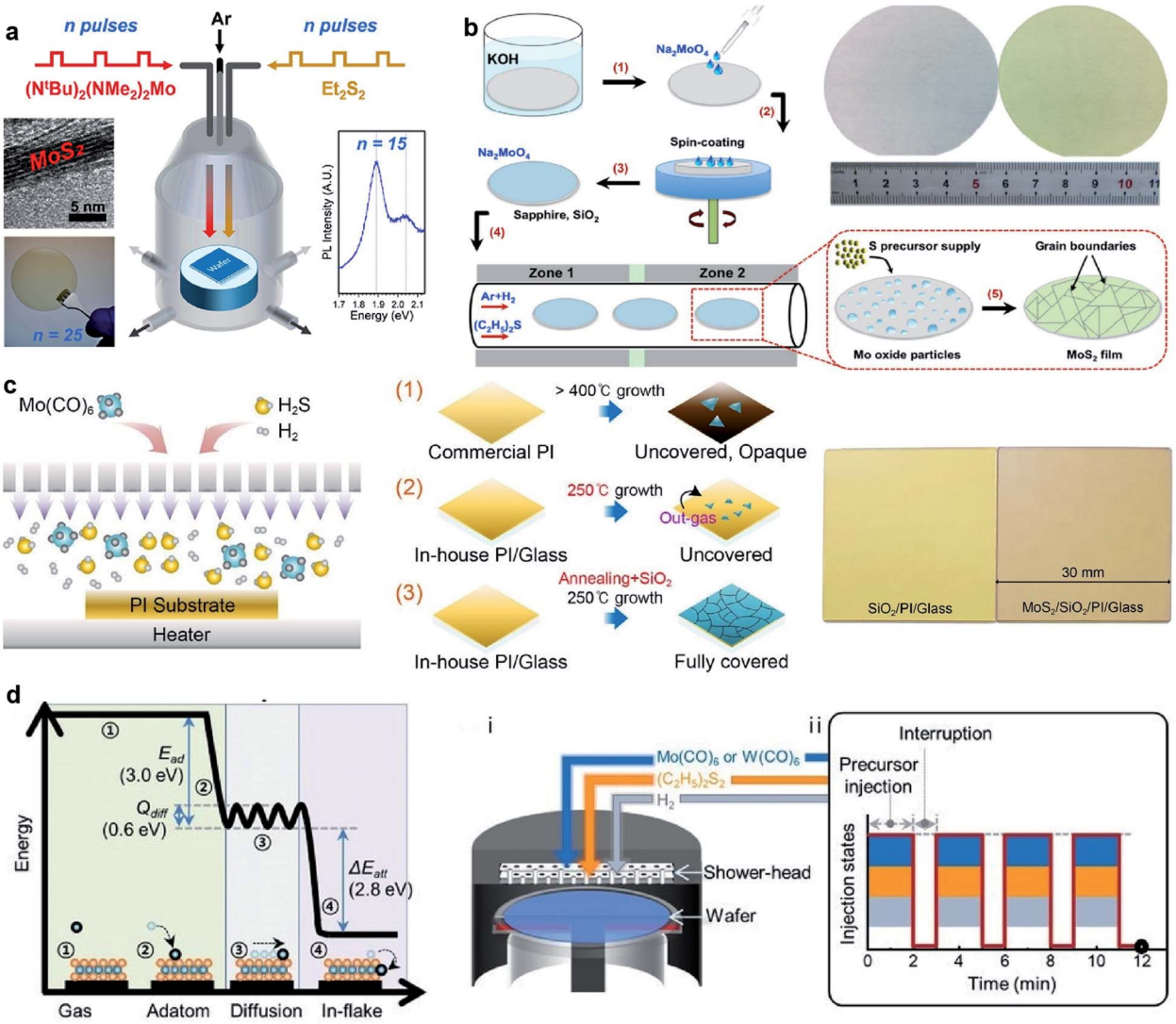

Fig. 5 (a) Schematic of pulsed MOCVD growth for 2H-MoS_2 in a single-wafer reactor geometry *via* pulsed injections of $(NtBu)_2(NMe_2)_2Mo$ and Et_2S_2.[53] Reproduced with permission from ref. 53, copyright 2017 American Chemical Society. (b) Schematic illustration of wafer-scale MoS_2 film growth process and photos of the 2-inch wafers of clean sapphire substrate (left) and the as-grown MoS_2/sapphire (right).[56] Inset: The proposed mechanism for MoS_2 growth on the substrates. Reproduced with permission from ref. 56, copyright 2019 Springer Nature. (c) Schematic of the direct growth process of MoS_2 on the PI substrate: (1) PI is changed to opaque and sparse MoS_2 islands are grown; (2) the growth of MoS_2 at 250 °C. (3) The heat-annealing and capping procedures prevent the outgassing phenomenon and further absorption in the ambient environment, forming fully-covered MoS_2.[21] Reproduced with permission from ref. 21, copyright 2019 American Chemical Society. (d) Calculated reaction energy diagram of Mo adsorbed on the basal plane of MoS_2 and the schematic illustration of (i) the reactor geometry and (ii) injection sequence of the precursors for growing wafer-scale monolayer TMD by pulsed MOCVD.[57] Reproduced with permission from ref. 57, copyright 2020 John Wiley and Sons.

mechanism using powdered precursors (MoO_3 and S) or mixed precursors (MoO_3 powders and H_2S gas), respectively. The vapor–liquid–solid (VLS) growth method often involves molten precursors (*e.g.*, non-volatile Na_2MoO_4) at growth temperatures higher than their melting points, which presents great promise in large-area MoS_2 synthesis with large single crystals for electronics.[58–60]

Recently, Li *et al.*[59] demonstrated the VLS growth of uniform monolayer MoS_2 flakes on 4-inch SiO_2/Si wafers and continuous MoS_2 films with the grain size exceeding 100 μm on 2-inch sapphire substrates using non-volatile precursors. Na_2MoO_4 particles were first dispersed on the growth substrate by spin-coating its aqueous solution. Then, Na_2MoO_4 on the substrates was loaded in the tube furnace and started to melt into a liquid, wetting the substrate surface when the temperature was higher than its melting point (687 °C). Sulfur vapor dissolves into the Na–Mo–O droplets, and the MoS_2 monolayer nucleated and grew from the sulfur over-saturated Na–Mo–O–S liquid on the substrate at 750 °C. Moreover, the Na_2MoO_4 particles can be patterned on the substrate with the aid of the photolithography process; patterned MoS_2 monolayers with desired sites were grown on the substrate after sulfurization.

Chang *et al.*[60] also utilized a self-capping vapor–liquid–solid (SCVLS) reaction for the growth of large single crystals and full-

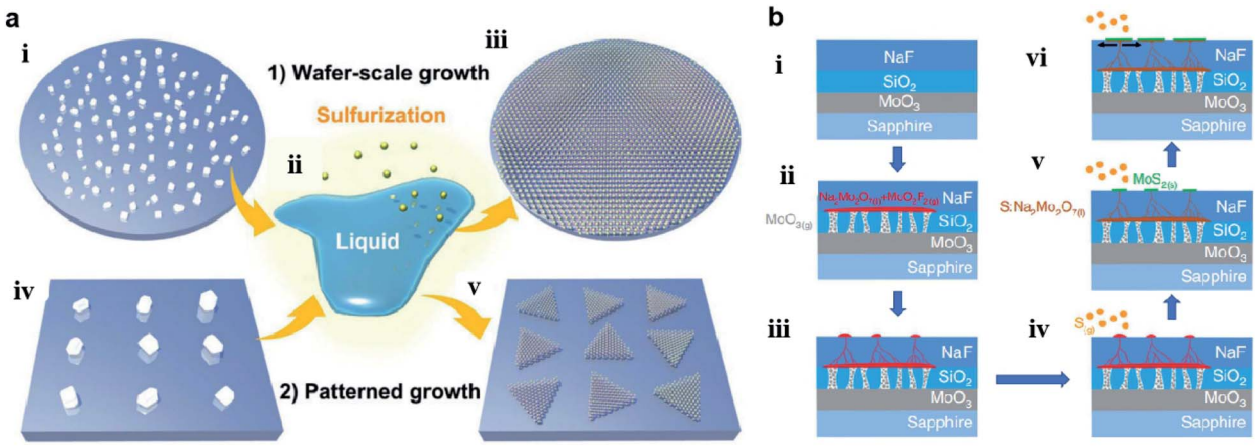

Fig. 6 (a) Schematics of wafer-scale and patterned growth of MoS_2 monolayers *via* the VLS method: (i) dispersed Na_2MoO_4 particles on sapphire wafer; (ii) molten Na_2MoO_4 droplet starts to wet the substrate surface; (iii) sulfurization of the molten Na_2MoO_4 droplets leads to the nucleation and growth of the VLS-MoS_2 film on the whole wafer; (iv) patterned Na_2MoO_4 particles on the growth substrate with the aid of photolithography; (v) patterned growth of monolayer VLS-MoS_2 flakes by the sulfurization of the site-specific non-volatile Na_2MoO_4 droplets.[59] Reproduced with permission from ref. 59, copyright 2019 The Royal Society of Chemistry. (b) Schematics of the SCVLS growth mechanism and the grown MoS_2: (i) structure of the solid precursor; (ii) MoO_3 vaporized and penetrated through the SiO_2 diffusion membrane. MoO_3 and NaF reacted to form liquid-phase $Na_2Mo_2O_7$ (colored in red) at the growth temperature; (iii): the liquid precursor gradually rose to the NaF matrix surface; (iv) sulfur vapor started to dissolve into the $Na_2Mo_2O_7$ liquid. (v) Liquid precursor sulfurized into the MoS_2 seed layer; (vi) capped by the MoS_2.[60] Reproduced with permission from ref. 60, copyright 2020 Springer Nature.

coverage TMD films. As shown in Fig. 6, a solid precursor comprising ultra-thin MoO_3, SiO_2, and NaF layers was used for the controllable eutectic reaction of MoO_3 and NaF at high temperature. Firstly, MoO_3 vapor broke the SiO_2 layer, diffused upward, and reacted with the NaF layer at a temperature higher than 500 °C to form liquid-phase $Na_2Mo_2O_7$ and gas-phase MoO_2F_2. Simultaneously, the consumption of NaF generated holes and pathways in the NaF layer, which allowed $Na_2Mo_2O_7$ and MoO_2F_2 to gradually rise to the top surface of the NaF. The as-formed eutectic liquid ($Na_2Mo_2O_7$) rose to the surface and was sulfurized into MoS_2 seeds, which acted as a self-capping layer and redirected the rising liquid into a horizontal direction. The residual liquid was continuously pushed along the growth direction and eventually sulfurized to form new MoS_2 at the edge of the MoS_2 seeds, thus making millimeter-sized MoS_2 single crystals formed on a *c*-plane sapphire.

2.6 ALD method

ALD exhibits advantages in the precise control of the film thickness, uniformity, and homogeneity over large-scale wafers due to the self-limiting growth mechanism. MoS_2 films with desired thickness can be obtained by varying the ALD cycles. The ALD procedure combines precursor exposure, purging, reactant exposure, and a final purging into a single cycle. The layers of the ALD MoS_2 films can be determined by the deposition temperatures and the ALD cycles. Large-area MoS_2 directly onto SiO_2/Si substrates have been achieved through the ALD method using molybdenum pentachloride ($MoCl_5$) and H_2S as the precursor and the reactant, respectively.[61] In different reports, the ALD growth temperatures of MoS_2 ranges from 350 °C to 900 °C.[61–64] Another well-investigated precursor pair for ALD MoS_2 is $Mo(CO)_6$/H_2S. This ALD process features the high vapor pressure of $Mo(CO)_6$ at room temperature and relatively low growth temperature. Jang *et al.*[65] reported MoS_2 film grown uniformly, reliably, and directly on a 4-inch wafer by ALD using an $Mo(CO)_6$ precursor and H_2S plasma as the precursor and reactant without a post-sulfurization process. The growth rate of MoS_2 on SiO_2/Si was approximately 0.05 nm per cycle and the deposition temperature ranged from 175 to 225 °C. Pyeon *et al.*[66] presented wafer-scale synthesis of MoS_2 layers on a 4-inch SiO_2/Si wafer with precise thickness controllability and excellent uniformity by ALD in the narrow ALD window of 155–175 °C, with $Mo(CO)_6$ and H_2S as the Mo and S precursors, respectively. Post-annealing in the range of 500–900 °C under an H_2S atmosphere efficiently improved the film properties, including the crystallinity and chemical composition. Extremely uniform film growth was achieved even on a 4-inch SiO_2/Si wafer. The growth temperature can be reduced in an ALD process using tetrakis(dimethylamido)-molybdenum(IV) (TDMA-Mo, $Mo(NMe_2)_4$) and H_2S as the precursors with an ALD growth rate of 1.2 Å per cycle at 60 °C.[67] Then, the obtained amorphous MoS_2 was treated at 1000 °C under sulfur vapor to improve the crystallinity. Recently, Liu *et al.*[68] developed thickness-controlled MoS_2 synthesis using $MoCl_5$ and hexamethyldisilathiane (HMDST) as the ALD precursors; the films were uniformly deposited on a sapphire and SiO_2/Si substrate after different ALD cycles from 20 to 90. As shown in Fig. 7, the thickness of the as-grown MoS_2 film after 50 ALD cycles was measured for 2.9 nm on sapphire and ~5 nm on the SiO_2/Si wafer with high uniformity.

2.7 Thermolysis of thiosalts

MoS_2 synthesis by the thermolysis of thiosalts is based on the thermal decomposition of ammonium thiomolybdates

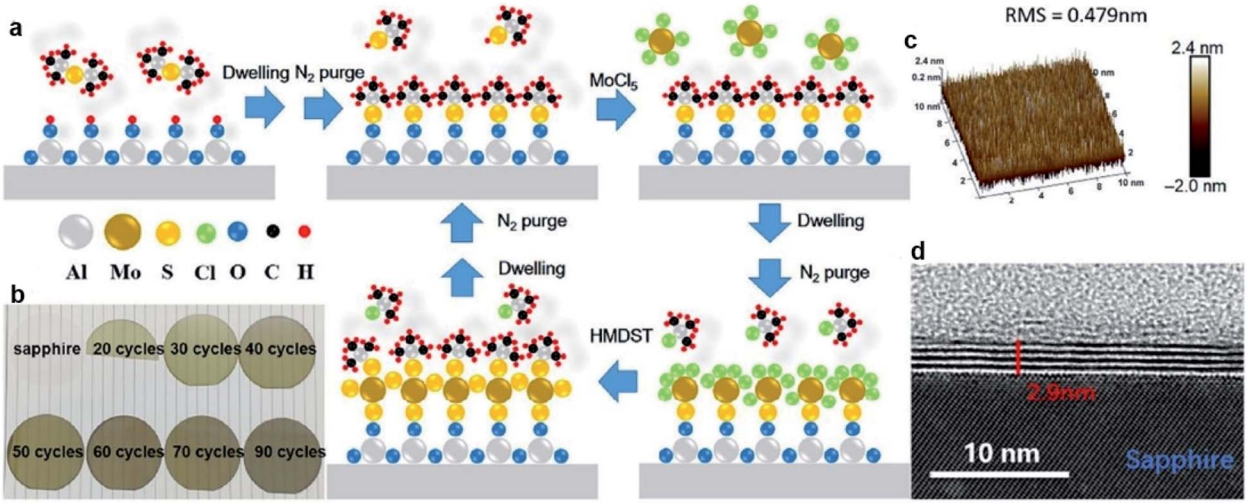

Fig. 7 ALD-grown MoS_2 on the sapphire substrate. (a) Schematic of our ALD-grown MoS_2 films, with $MoCl_5$ and hexamethyldisilathiane (HMDST) as the precursors. (b) Images of sapphire substrate; 20, 30, 40, 50, 60, 70, and 90 cycles of ALD-grown MoS_2 on sapphire. (c) 3D AFM image of ALD-grown MoS_2 film on a 10 μm × 10 μm area, with the roughness RMS of this region being 0.479 nm. (d) TEM images of an annealed 50-cycle MoS_2 film of 2.9 nm thickness on the sapphire substrate.[68] Reproduced with permission from ref. 68, copyright 2020 Springer Nature.

$(NH_4)_2MoS_4$ in a specific environment, which results in the conversion of $(NH_4)_2MoS_4$ to MoS_2 at a higher temperature. The precursor solution of $(NH_4)_2MoS_4$ can be deposited on different substrates and highly crystalline centimeter-scale MoS_2 can be synthesized after thermal decomposition in a N_2 or sulfur-rich atmosphere.[69–72] Lim *et al.*[71] reported large-area MoS_2 layers by the simple coating of single source precursor with subsequent roll-to-roll-based thermal decomposition with N_2 at 600 °C under 1.8 Torr pressure. An $(NH_4)_2MoS_4$ solution was bar--coated onto a Ni foil and subsequently thermally decomposed using the roll-to-roll process, resulting in 50 cm long MoS_2 layers synthesized on Ni foils with excellent long-range uniformity and optimum stoichiometry. The number of MoS_2 layers can be simply adjusted by optimizing the concentration of $(NH_4)_2MoS_4$ and the solvent conditions. Park *et al.*[72] introduced a direct and rapid method for the layer-selective synthesis of patterned MoS_2 at the wafer-scale using a pulsed laser annealing system ($\lambda = 1.06$ μm, pulse duration ~100 ps) in ambient conditions. The $(NH_4)_2MoS_4$ precursor was spin-coated on a Si/SiO_2 wafer and annealed at 150 °C for 3 min to evaporate the residual solvents. Then, a pulsed fiber laser was used to induce a local photothermal reaction under sulfur-rich conditions to thermally decompose into MoS_2. The heat treatment area was precisely defined and the precursor layer in the non-treated area was simply removed by the DMF solvent, leaving a patterned MoS_2 film. Fig. 8(c) and (d) provide the mechanism of selective conversion of $(NH_4)_2MoS_4$ precursors into MoS_2. Moreover, the ultrafast and selective synthesis of individual patterned MoS_2, WS_2 layers, and stacked WS_2/MoS_2 heterojunction structure can be directly realized on a 4-inch wafer.

3. Application in basic MoS_2-FET

The downscaling trend of integrated electronics based on silicon-based micro-fabrication processes lead to continuing demands for minimizing the channel thickness. 2D MoS_2 with atomic thickness is considered as one of the most promising candidates for advanced electronics with minimum channel thickness. The wafer-scale 2D MoS_2 films synthesized from different methods can be transferred and integrated onto a variety of substrates by PMMA and PDMS, demonstrating many important applications in electronic and optoelectronic devices.[11–13,31] Thus, the fabrication process of wafer-scale MoS_2-based devices can be more compatible with the traditional CMOS fabrication process. In order to be compatible with typical transistor requirements for electronic applications, many investigations have focused on developing wafer-scale monolayer MoS_2 and high-performance MoS_2-FET.[11–13] Generally, a typical 2D MoS_2-FET involves three terminals (namely gate, drain and source), with a basic configuration consisting monolayer or few-layer MoS_2 channel, electrical contacts for the source and drain, dielectric layer, and gate electrode. Jing *et al.*[73] summarized the different 2D FET configurations reported in the previous study for research purposes: (i) back-gated FET with Si as the gate; (ii) back-gated FET with a manufactured metal gate electrode; (iii) top-gated FET; (iv) dual gate FET structure with an Si back gate, (v) dual-gated FET with a patterned back gate; (vi) liquid-gated FET structure. Considering the Schottky barrier and interface scattering effect, the dielectric layer is known to be a key factor for all these configurations, which should be compatible with the 2D channel to suppress extrinsic scattering. Commonly used dielectric layers include inorganic materials and some polymers, such as SiO_2, Al_2O_3, HfO_2, ZrO_2, PVDF, PMMA, and CaF_2.[74–81] Few-layer graphene, h-BN and $MoSe_2$ are also considered as dielectrics to improve the field effect mobility in MoS_2-FET.[82–84] Another key issue is contact and channel engineering in the FET device fabrication based on large-area 2D MoS_2 films. The terminals of the drain and the source refer to the metal electrode, such as Au, Cr/Au, Ti/Au, Pd/

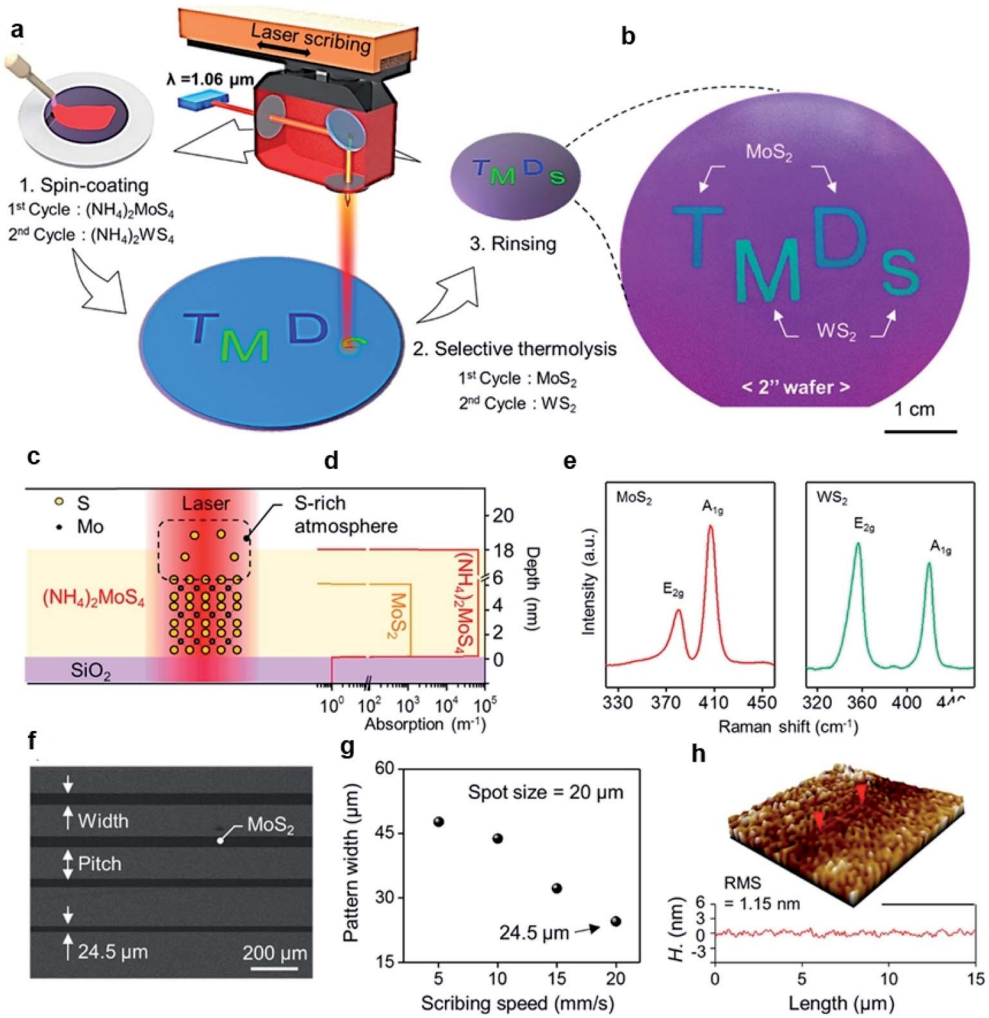

Fig. 8 Layer-selective synthesis of MoS_2 and WS_2. (a) Schematic illustration of the selective synthesis of MoS_2- and WS_2-based homostructures. (b) Photograph of patterned MoS_2 and WS_2 on the 2-inch SiO_2/Si substrate. (c and d) Synthetic mechanism of MoS_2 and the absorption coefficient profile of each layer. (e) Raman spectra of synthesized MoS_2 and WS_2. (f) SEM image of the line-patterned MoS_2 with different scribing speeds. (g) Pattern width and pitch variation as a function of the scribbling speed. (h) Three-dimensional surface morphology of MoS_2.[72] Reproduced with permission from ref. 72, copyright 2020 American Chemical Society.

Au, Ni/Au, and Cr/Pt, which is deposited and patterned *via* electron beam evaporation and the lithography process. Due to the Schottky barrier and Fermi level pinning at the metal/semiconductor interface, different investigations in MoS_2-FET have been made to minimize the contact resistance and realize near-ohmic contacts by choosing appropriate work function metals, creating an ultra-clean interface, inserting a buffer layer, *etc.*[85–91] In this regard, extensive efforts have been devoted to investigate 2D MoS_2-FET based on wafer-scale monolayer or few-layer MoS_2 with different device configurations and dielectric layers.

3.1 Configurations and fabrications

Similar to that of traditional silicon-based FET, different configurations of FET based on 2D MoS_2 have been studied in recent years. The most common configurations include: (1) back-gated MoS_2-FET, (2) top-gated MoS_2-FET, (3) dual-gated MoS_2-FET. These MoS_2-FET devices can be fabricated through a series of general processes with different processing sequences, including MoS_2 patterning, dielectric layer deposition, metal electrode deposition, and patterning. Most MoS_2 channels are patterned by controlled plasma etching or the lithographic method after MoS_2 synthesis or transfer, while other MoS_2 channels can be realized from the patterned thin-film Mo precursor after sulfurization.[76,91–97] The dielectric layer of Al_2O_3, HfO_2, and ZrO_2 are usually deposited by ALD, while PVDF and PMMA are prepared by the spin-coating method. The metal electrodes can be defined and deposited by e-beam evaporation after the photolithography process or e-beam evaporation with shadow masks.

(i) Back-gated MoS_2-FET. Back-gated MoS_2-FET with Si as the gate is the most widely used configuration in basic studies, with SiO_2 as a typical dielectric layer. In this configuration, 2D MoS_2 is directly grown or transferred on the SiO_2/Si substrate and then selectively etched to form the channel by plasma.

Finally, the source/drain contacts are prepared by a sequential lithography process, including photolithography, e-beam evaporation, and lift-off. For instance, Kim *et al.*[75] presented the successful integration of the devices based on ~1200 back-gated MoS_2-FET arrays with a yield of 95% on 4-inch SiO_2/Si wafers. As shown in Fig. 9, large-area MoS_2 films were synthesized by MoO_3 pre-deposition on a sapphire substrate *via* radio frequency (RF) sputtering and following sulfurization *via* CVD. The as-synthesized four-layered MoS_2 film was transferred from the sapphire substrates onto the SiO_2/Si substrates by PMMA and then patterned for the channel region of the FET array devices *via* reactive ion etching. Au/Cr metallic electrodes were fabricated by a sequential lithography process. This growth technique could yield wafer-scale MoS_2 thin film such that an array of approximately 1200 MoS_2 transistors occupying a 2-inch active area of a 4-inch silicon wafer could function well, with excellent electrical characteristics.

Back-gated FET with patterned metal or semiconducting gate electrode is another configuration used in MoS_2-FET. Seol *et al.*[55] fabricated back-gate MoS_2-FETs on a 6-inch wafer with Ti/Au as the back-gate contact and ALD-Al_2O_3 as the gate dielectric. The as-grown MoS_2 film was transferred by PMMA and patterned using photolithography and O_2 plasma etching after the deposition of Ti/Au and Al_2O_3. Wei *et al.*[87] developed a flexible back-gated MoS_2-FET fabricated on low-cost polyethylene terephthalate (PET) substrates by 2D MoS_2 and dielectric ceramic $Bi_2MgNb_2O_9$ (BMN). Recently, Li *et al.*[13] reported flexible MoS_2-FET arrays on the PET substrate with an improved device density of 1518 per cm^2. The wafer-scale MoS_2 monolayers grown on sapphire were transferred onto PET substrates with pre-deposited ITO and Al_2O_3, which serve as the back-gate electrode and dielectric layer. It is also demonstrated that Au/Ti/Au rather than Ti/Au is an excellent contact structure to reduce contact resistance in the monolayer MoS_2 devices. Lan *et al.*[88] demonstrated both N-type and P-type MoS_2-FET by directly growing MoS_2 on the fin oxide structure by the CVD method. The fin oxide structures selectively-implanted Si contacts lead to N-type and P-type MoS_2 film growth on a wafer/chip, which can be compatible with the Si-based fabrication process. The SiO_2 interfacial layer and HfO_2 high-k dielectric were deposited on CVD-grown MoS_2 by ALD, followed by metal-gate deposition. The Fin-FET based on MoS_2 synthesized from the P^+–Si and N^+–Si contact presented P-type and N-type performance, respectively, which can be integrated as a complementary MoS_2 inverter for basic integrated circuit complementary device applications.

(ii) Top-gated MoS_2-FET. The structure of the top-gated FET is similar to that of the back-gated one, with the main difference that the patterned gate electrode is placed above the 2D channel. In this configuration, the top gate insulator can

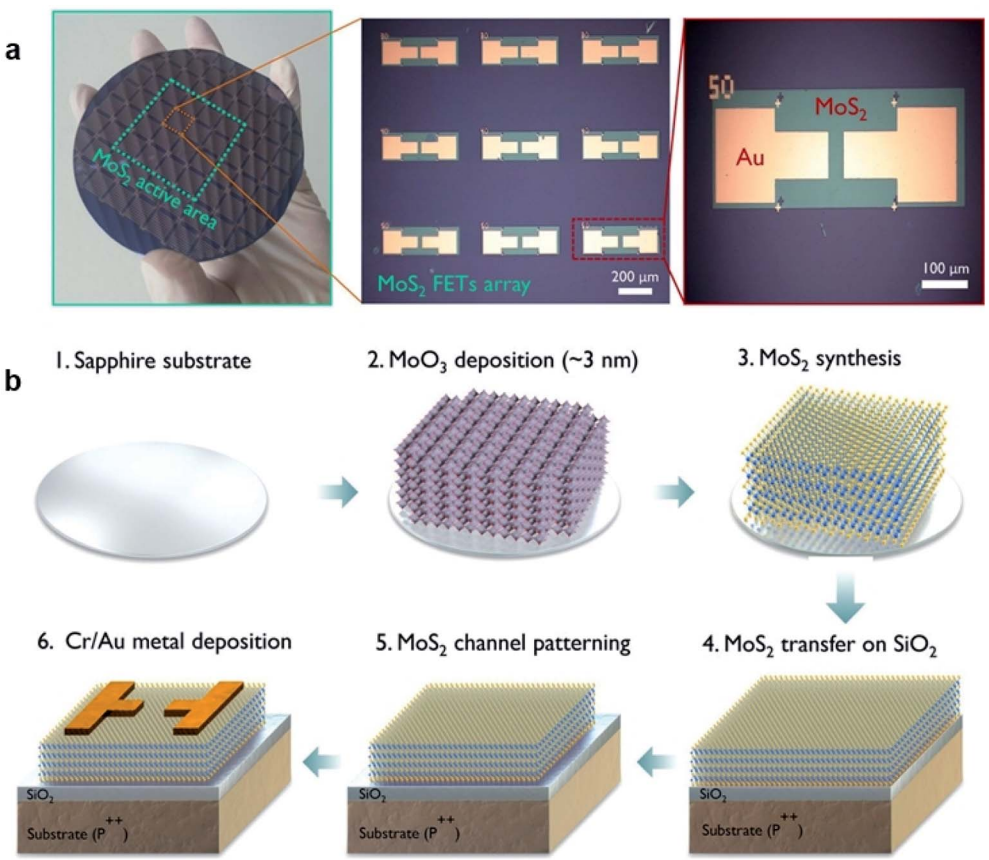

Fig. 9 (a) Optical image of the 2D MoS_2-FET array devices integrated on a 4-inch SiO_2/Si wafer and (b) the sequence of the fabrication process for MoS_2 array devices.[75] Reproduced with permission from ref. 75, copyright 2017 American Chemical Society.

also work as an encapsulating layer covering the entire MoS_2 channel, which can both improve the stability and the mobility of MoS_2-FET.

Zhang *et al.*[76] successfully fabricated top-gated MoS_2-FET arrays based on wafer-scale continuous MoS_2 film using wafer-scale Si shadow masks (Si-SMs) with customized patterns. Metal deposition and plasma etching by the Si-SMs exhibit well-defined patterns with sharp edges. As shown in Fig. 10, top-gated MoS_2-FET arrays were fabricated using two different processing strategies assisted by the Si-SMs: 'etching-last' and 'channel-first'. For the 'etching-last' strategy, the metal contacts were deposited with the Si-SMs at the beginning, followed by the plasma etch to isolate a continuous film with Si-SM as the protective layer. For the 'channel-first' method, a layer of Mo metal defined by Si-SM was deposited on the sapphire substrate. Then, the patterned Mo was subsequently sulfurized in a sulfur-rich atmosphere at 900 °C to form a patterned polycrystalline MoS_2 film. The MoS_2-FET arrays can be obtained after dielectric growth and top gate deposition, without suffering from photoresist residue and long-time immersion in the photoresist remover.

Wang *et al.*[33] built top-gated FET with a high-κ HfO_2 directly fabricated from the CVD-grown monolayer MoS_2. The MoS_2 active regions for the transistors were defined in a patterning step, followed by a CHF_3-based reactive ion etching process. After that, Ti/Au source/drain electrodes were formed by electron beam evaporation, following the patterning step. The gate dielectric of HfO_2 was grown by ALD and the top-gate Ti/Au was deposited, followed by a standard lift-off process. Similar to the back-gate FET, P(VDF-TrFE) and PMMA were also reported as the gate dielectric by spin-coating in the top-gated MoS_2-FET.[79]

(iii) Dual-gated MoS_2-FET. This device configuration with both back-gate and top-gate can provide the highest degree of controllability of the charge carriers in the 2D channel, which can use a doped-Si substrate or patterned back-gate. Zhang *et al.*[99] demonstrated a dual-gated FET structure to improve the electrostatic control of MoS_2-FET with bilayer MoS_2. In this configuration, a patterned Au electrode array and 15 nm HfO_2 layer were deposited on the SiO_2/Si substrate to form the back gate and the back gate dielectric layer, respectively, as shown in Fig. 11. The bilayer-MoS_2 film was then transferred onto this substrate and patterned by plasma etching. After source/drain electrode deposition, a second layer of 15 nm HfO_2 layer as the top dielectric layer and Au top gate electrodes were deposited, leading to a dual-gated FET structure to the back and top gates with a symmetric high-k dielectric layer. Compared with the single-gated MoS_2-FET, the array with 81 dual-gated bilayer MoS_2-FETs exhibits an excellent solution to compensate for the degradation of electrostatic control. Liao *et al.*[100] reported similar dual-gated MoS_2-FET with symmetric back-gated and top-gated architecture based on exfoliated MoS_2 and CVD-

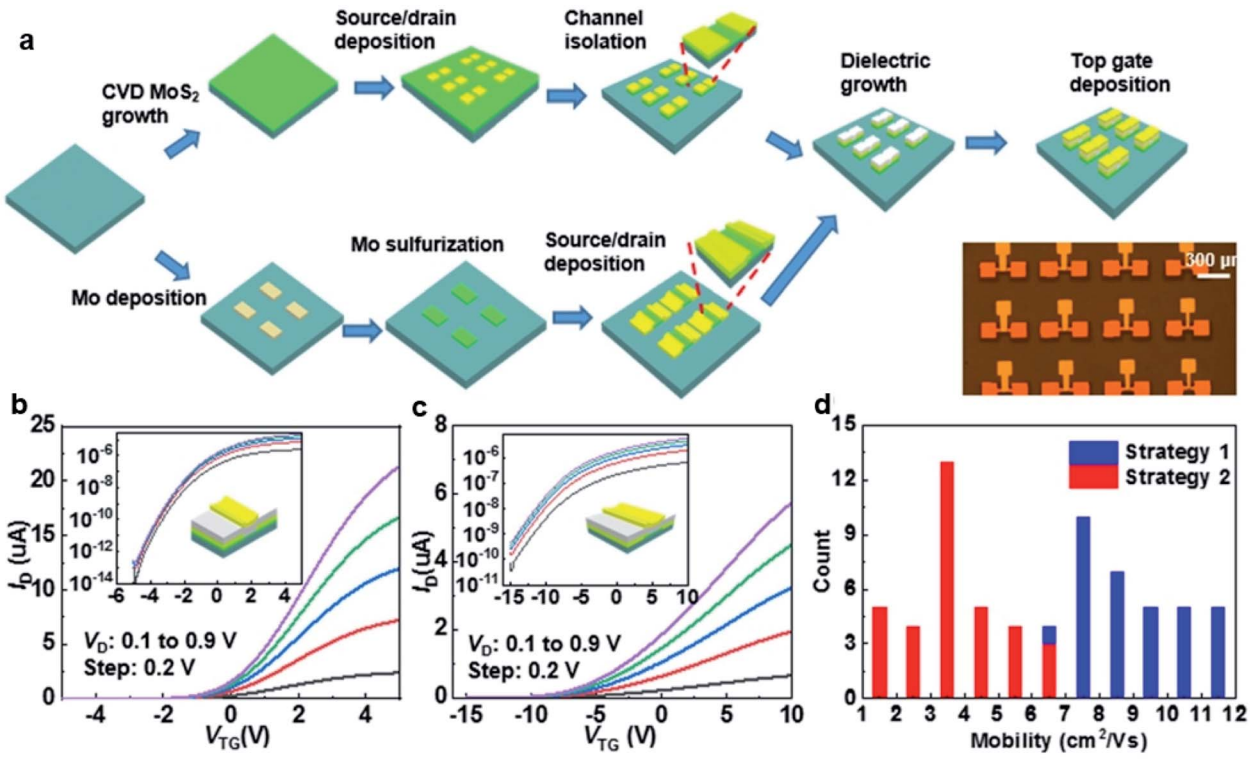

Fig. 10 (a) Schematic illustration of strategy 1: 'etching-last' and strategy 2: 'channel-first'. The bottom right corner shows an optical image of the as-fabricated MoS_2-FET device arrays. The transfer characteristics of the top-gated transistor fabricated using (b) 'etching-last' and (c) 'channel-first' at different V_{ds}. The insets show the corresponding transfer curves on a log-scale. (d) Histograms of the effective mobility of the CVD arrays fabricated with the two strategies.[76] Reproduced with permission from ref. 76, copyright 2020 IOP Publishing, Ltd.

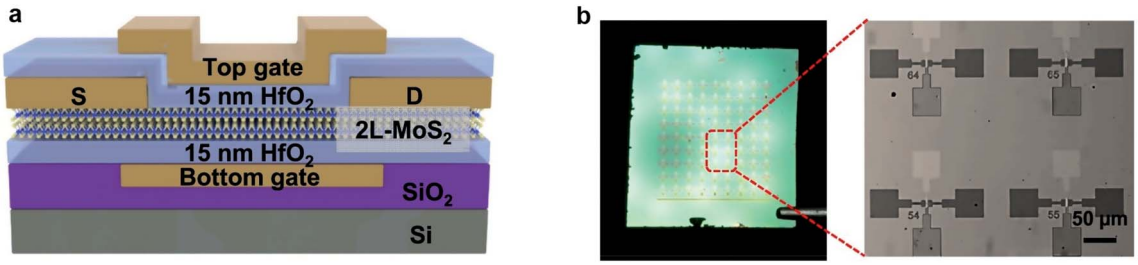

Fig. 11 Schematic illustration, optical images, and electrical characteristics of the dual-gated MoS_2 device. (a) Cross-sectional schematic of the dual-gated MoS_2 device. (b) Photograph of a dual-gated bi-layer MoS_2 transistor array on a 1 × 1 cm^2 wafer (left) and an optical microscopic image (right) of the zoom-in area at the left.[99] Reproduced with permission from ref. 99, copyright 2019 IOP Publishing, Ltd.

synthesized MoS_2 continuous film. Furthermore, dual-gated MoS_2-FET with multi-layer graphene floating gate (FG) and ionic top gate are also reported in multiple operating conditions to demonstrate different electronic applications.[84,101]

3.2 Characterization and performances

The characterization of synthesized MoS_2 films and fabricated MoS_2-FETs is essential for both fundamental research and practical application. The basic characterization of 2D MoS_2 consists of lateral size, thickness, morphology, PL spectroscopy, and Raman spectroscopy, which can be measured by optical microscopy, atomic force microscopy (AFM), photoluminescence spectrometry, and Raman spectroscopy, as shown in Fig. 7(c), (d) and 8(e), (h). Further information of the 2D MoS_2 film, such as grain size, grain boundaries, lattice orientations, phase composition, and structural defect determination, can be inferred from various microscopy techniques, such as scanning tunneling microscopy (STM), high-resolution transmission electron microscopy (HRTEM), and low-energy electron diffraction (LEED). In addition, the X-ray diffraction (XRD) technique, X-ray photoelectron spectroscopy (XPS), and ultraviolet-visible (UV-vis) spectrophotometry were also applied for the investigation of the film quality and the optoelectronic property based on 2D MoS_2.

The typical characterization of 2D MoS_2-FETs refers to the current flowing between the drain and the source (I_{ds}), which can be controlled by tuning the gate voltage (V_g) and the drain–source voltage (V_{ds}). The main figures of merit of an FET are the transfer characteristic (I_{ds} *vs.* V_g, for a specific V_{ds}) and the output characteristic (I_{ds} *vs.* V_{ds}, for various V_g). The measurement transfer characteristic ($I_{ds} - V_g$) and the output characteristic ($I_{ds} - V_{ds}$) of the 2D MoS_2-FET were usually carried out on a semiconductor parameter analyzer (such as Keithley 4200-SCS) at room temperature. From the transfer characteristic, several important operational parameters of the FET can be extracted, such as the current ratio between the ON and OFF states (I_{on}/I_{off}), threshold voltage (V_{th}), field effect mobility (μ_{FE}), and subthreshold slope (SS). The value field effect mobility and subthreshold slope can be evaluated using eqn (1) and (2)

$$\mu_{FE} = \left[\frac{dI_{ds}}{dV_g}\right] \times \left[\frac{L}{WC_g V_{ds}}\right] \quad (1)$$

$$SS = \frac{d(\log I_{ds})}{dV_g} = \left[\frac{dV_g}{d(\log I_{ds})}\right] \quad (2)$$

in which L is the channel length, W is the channel width, and C_g is the capacitance between the channel and the gate per unit area.

Since the performance is directly affected by the MoS_2 quality and device configuration, different factors should be considered in 2D MoS_2-FETs, such as film thickness, grain size, defect situation, electrode/channel contact resistance, dielectric layer, channel length, and channel width. The improved quality of the wafer-scale MoS_2 films with larger grain size and less defects is preferred in MoS_2-FET with different configurations. The resistance of the electrode/channel contact caused by the Schottky barrier and Fermi-level pinning at the metal/channel interface can be reduced by the post-annealing process, optimizing the stacked metal electrode, and inserting a buffer layer.[85–87,90–92] Since the large dielectric constant of the high-k material contributes to the reduction of the effective size of the Coulomb impurities, different dielectric layers, such as SiO_2, HfO_2, Al_2O_3, $LiNbO_3$, CaF_2, PMMA, PVDF, h-BN, and graphene, have been utilized as the gate dielectric to improve the mobility of 2D MoS_2-FET.[75–84] The dielectric layer can also be used on the top of the MoS_2 channel, function as the encapsulation layer, and to provide a dielectric environment to improve the device performance and reliability. The performance of different 2D MoS_2-FETs based on the monolayer and few-layer MoS_2 films are summarized in Table 1.

From Table 1, it can be inferred that the performance of MoS_2-FET varies considerably from device to device. Different factors, such MoS_2 thickness, device configuration, dielectric choice, channel size, and fabrication process, interact and simultaneously affect the performance of MoS_2-FET. Even though the field effect mobility is still behind the highest reported value (167 ± 20 cm^2 V^{-1} s^{-1}) from the exfoliated MoS_2,[14] the I_{on}/I_{off} ratio and field effect mobility of MoS_2-FET based on wafer-scale monolayer MoS_2 is encouraging. Considering the complicated fabrication procedures and different repeatability, it is difficult to make simple comparisons between different devices based on the monolayer MoS_2 film from different synthetic methods. Overall, more developments are needed for realizing high-performance MoS_2-FET with larger mobility,

Table 1 Performance parameters of 2D MoS_2-FETs based on wafer-scale MoS_2 films

MoS_2	Configurations	Dielectrics	L (μm)	μ_{FE} ($cm^2\ V^{-1}\ s^{-1}$)	I_{on}/I_{off} ratio	SS ($mV\ dec^{-1}$)	Ref.
Monolayer on sapphire by CVD	Top-gated	HfO_2	3.5	0.1–3	$>10^6$	130	8
4-Inch monolayer by CVD	ITO back-gated	Al_2O_3	6	~55	10^{10}		13
Few-layer by exfoliation	Back-gated	SiO_2	2	167 ± 20			14
8-Inch monolayer by MOCVD	Back-gated	SiO_2	10	0.47	5.4×10^4		18
4 inch-scale by MOCVD	Back-gated	SiO_2		7–12	10^4–10^7		21
6-Inch monolayer by CVD	Back-gated	SiO_2	1	6.3–11.4	10^5–10^6		24
Monolayer by Au-assisted exfoliation	Top-gated	SiO_2		22.1–32.7	~10^7	100	30
2-Inch monolayer by CVD	Back-gated	SiO_2	30–60	~40	~10^6		31
2-Inch continuous by CVD	Top-gated	HfO_2	10–100	70	10^7	150	32
4-Inch monolayers by CVD	Back-gated	SiO_2	10	~70	~10^9		33
Monolayer by APCVD	Back-gated	Al_2O_3		0.033	5.8×10^5		34
Wafer-scale monolayer by CVD	Back-gated	SiO_2	20	1.2			35
Monolayers on Au by CVD	Back-gated	SiO_2	5	~11.2	7.7×10^5		37
Continuous monolayer by CVD	Back-gated	SiO_2	1	~9.8	3.1×10^6		40
2-Inch by PLD and sulfurization	Top-gated	HfO_2	90	8.85	~10^5		50
Monolayer by MOCVD	Back-gated	SiO_2	10	21.6			51
Monolayer on 2-inch sapphire	Top-gated	Al_2O_3	15	~0.76	~10^4		52
$3.5 \times 3.5\ cm^2$ monolayer by CVD	Back-gated	SiO_2	20	1.3×10^{-2}	~10^4	8300	55
2-Inch monolayer by MOCVD	Back-gated	SiO_2	10	21.6			56
Monolayer by MOCVD	Ti/Au back-gated	Al_2O_3	10	3.4 ± 0.3	10^7		57
Monolayers by VLS	Back-gated	SiO_2		21.1	10^7–10^9		59
$1.5 \times 1.5\ cm^2$ monolayer by VLS	Back-gated	SiO_2	1.48	33	$>10^8$	980	60
Few-layer on sapphire by ALD	Top-gated	Al_2O_3	25	0.56	10^6		68
Continuous monolayer by CVD	Top-gated	Al_2O_3		6.44	$>10^8$		76
$10 \times 10\ mm^2$ monolayer by CVD	Back-gated	HfO_2	6	118	10^8		77
Monolayer and bilayer by CVD	Dual-gated	Y_2O_3/HfO_2	10	1–9	$>10^6$		90
Monolayer by CVD	Back-gated	SiO_2		2.87	3.2×10^6		96
Bilayer by CVD	Dual-gated	HfO_2	10	32.5		~800	99

higher I_{on}/I_{off} ratio, steeper subthreshold slope, and better stability. With the development of MoS_2 synthesis and MoS_2-FET engineering, the improved basic performance of wafer-scale MoS_2 devices will render the wafer-scale MoS_2 film to be a promising candidate for next-generation electronics, which can be compatible with the traditional silicon-based fabrication process.

4. Toward practical application

Although the charge carrier mobility of 2D MoS_2-FET is not directly comparable to that of Si-based devices, the high I_{on}/I_{off} ratios and low stand-by power suggests suitable application for low-power electronics and optoelectronics. To advance one step further from a single FET to a complex device, the explorations of electronic devices and optoelectronic devices based on 2D MoS_2, such as N-metal-oxide-semiconductor (NMOS) inverters, logic gate circuits (NAND, NOR, NOT, AND), content-addressable memory (TCAM), and integrated photodetectors, presents great potential application of 2D MoS_2-FET for future integrated electronics and flexible optoelectronics.[13,68,98,101–142]

4.1 Logic devices

To build a working logic device, basic requirements are necessary for voltage switching and high frequency operation, such as high I_{on}/I_{off} ratio (>1000) and moderate mobility. In practical applications, different individual MoS_2-FET can be integrated with necessary designs for realizing an inverter. Shin *et al.* realized a logic inverter and NAND gate based on the GaS/MoS_2 heterostructure comprising a switching transistor and a load resistor. The upper transistor is the load resistor with the transistor gate connected to the output electrode, while the lower transistor acts as a switch by applying an input signal to the gate.

Liu *et al.*[68] realized an inverter from two top-gated MoS_2-FETs and constructed several complex logic devices from 3 or 5 MoS_2-FETs. The top-gated FETs based on the wafer-scale MoS_2 synthesized by the ALD method show a high on/off ratio at 10^6 and a carrier mobility of 0.56 $cm^2\ (V^{-1}\ s^{-1})$. An inverter with a fast response was fabricated using two N-type MoS_2-FETs (a load FET and a pull-down FET) with a different width of the channel, while the gate electrode of the pull-down FET serves as the input terminal. The NAND and NOR gates with three or five FETs were built successfully based on the load FET and the pull-down FET with channel sizes of $L = 5$ μm, $W = 50$ μm, and $L = W = 5$ μm. Two different input voltages, −5 V and 8 V, correspond with the input state of '0' and '1', respectively. Then, the AND and OR gates were realized by connecting the NAND and NOR gates with the inverter logic afterwards.

Li *et al.*[13] fabricated flexible top-gated MoS_2-FETs with different channels and demonstrated the application in integrated flexible logic devices. The devices exhibit on/off ratios of ~10^{10}, carrier mobilities of ~55 $cm^2\ V^{-1}\ s^{-1}$, and good stability and strong tolerance under strain. As shown in Fig. 12, flexible

logic devices such as inverters, NOR gates, NAND gates, SRAMs, AND gates, and five-stage ring oscillators can be realized by integrating 2, 2, 3, 4, 5, and 12 MoS_2-FETs, respectively. The inverter shows high voltage gains of 43 and 107 at bias voltages of $V_{dd} = 2$ V and 4 V, respectively. The outputs of the NOR and NAND gates are in two states (0 V and 2 V) by combining two input voltages logically at $V_{dd} = 2$ V and are stable after bending. Two different input voltages, 0 V and 5 V, correspond to the input state of '0' and '1', respectively. The flip-flop memory cell (SRAM) consisting of two inverters exhibit two stable output states, 0 V and 2 V, at $V_{dd} = 2$ V. The AND gate is constructed from a NAND gate and an inverter at $V_{dd} = 2$ V, with a settable state 0 V or 2 V by modifying the two input voltage states. A five-stage ring oscillator was integrated by five inverters and an additional inverter as the output buffer to eliminate the interference. Oscillation frequencies of 860 kHz and 13 MHz were achieved in the flexible ring oscillator when applying $V_{dd} = 5$ V and $V_{dd} = 15$ V, respectively.

4.2 Memory devices

Memory devices, such as dynamic random access memory (DRAM), static random access memory (SRAM), and resistive RAM (RRAM), are essential for digital data storage. 2D MoS_2-

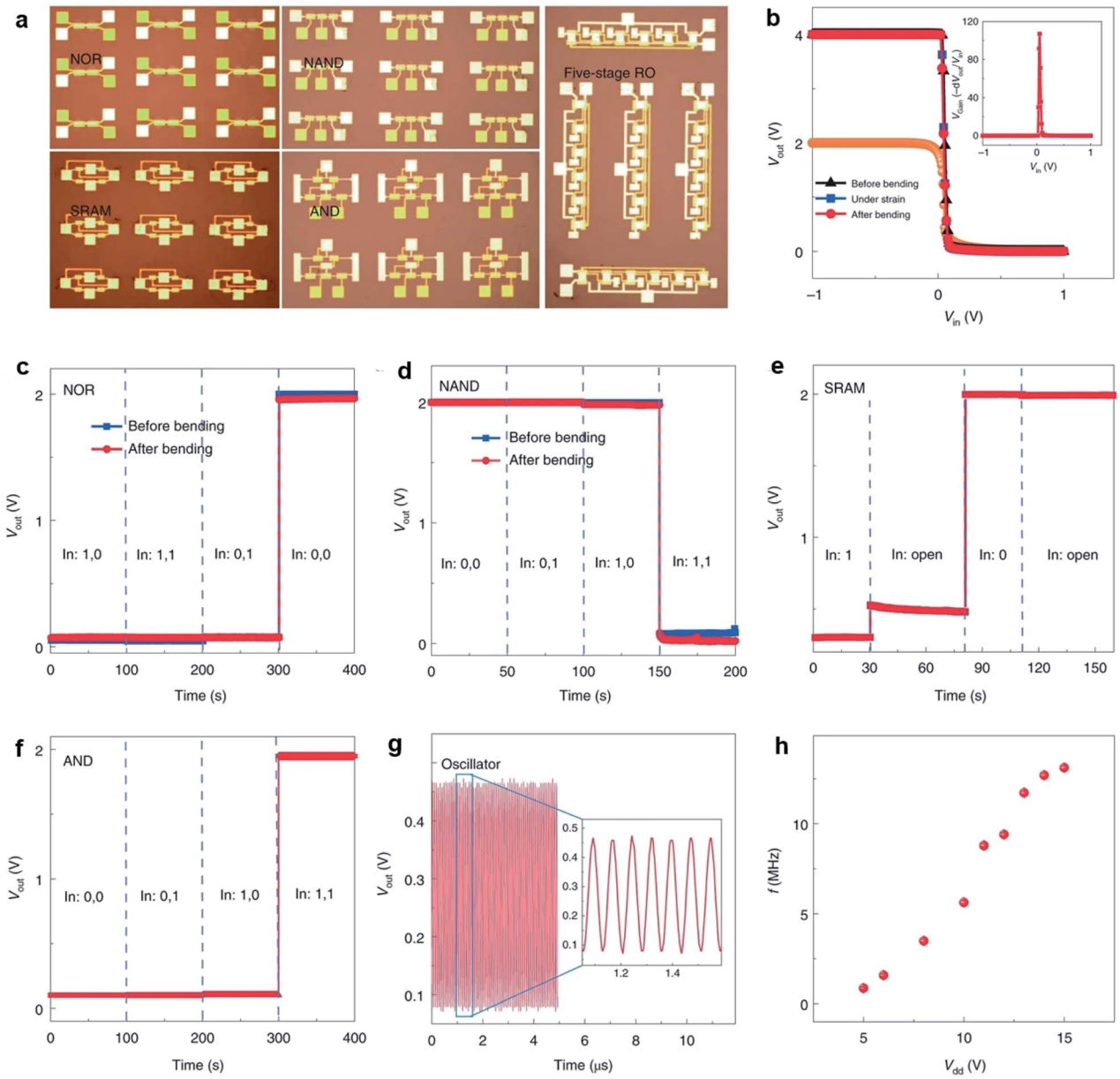

Fig. 12 (a) Photographs of different MoS_2 integrated devices on flexible substrates. (b) Output voltage of an inverter as a function of input voltage when under different bending states. Inset: voltage gain of the inverter under an input of 4 V. Output characteristics of flexible NOR (c) and NAND (d) gates before and after bending at $V_{dd} = 2$ V. Logic '0' and '1' mean 0 V and 5 V, respectively, for these and all the following logic devices. Output characteristics of flexible SRAM (e) and AND (f) gates at $V_{dd} = 2$ V. (g) Output waveform of a five-stage ring oscillator at $V_{dd} = 15$ V. (h) Output frequency as a function of supply voltage V_{dd}.[13] Reproduced with permission from ref. 13, copyright 2020 Springer Nature.

FET is also advantageous in the applications of memory devices. The low leakage currents and high off state in monolayer MoS_2-FET can reduce the total power consumption and lead to high speed. Meanwhile, MoS_2 with atom thickness is immune to short channel effects suitable for large-scale and tight integration with small footprints. Liao *et al.*[100] reported DRAM applications based on dual-gated MoS_2-FET with excellent electrostatic control of the channel current. A 1T1C DRAM unit cell consisting of a metal–insulator–metal capacitor and a dual-gated MoS_2-FET was fabricated on a sapphire substrate. Yang *et al.*[112] demonstrated a TCAM architecture formed by integrating monolayer MoS_2-FET with HfO_x-RRAM in a two-transistor-two-resistor (2T2R) layout, as shown in Fig. 13. The MoS_2-FETs are based on continuous, CVD-grown monolayer MoS_2 and have 5 nm HfO_x and 22 nm Al_2O_3 as the top gate dielectric, with channel width $W = 50$ μm and channel length $L = 0.8$ μm. The high on/off ratio up to 2×10^7 not only provides enough current drive to the RRAMs but also sustains sufficiently large voltages for programming the RRAMs. In a device with one-transistor-one-resistor (1T1R) configuration, when the FET turned on, the programming voltage is applied on the top electrode of the RRAM. Then, the RRAM is repeatedly reset/set to HRS/LRS by applying negative/positive voltages on TE (V_{TE}) while grounding the source.[113] The monolayer MoS_2-FET drives enough current to the RRAM and reliably controls the current compliance during the RRAM set process. Due to the low off-state current of MoS_2-FET and the robust current control in the 1T1R driving scheme, the MoS_2-TCAM cells show very large R-ratios up to 8.5×10^5. These results represent a key application of transistors based on the CVD-grown monolayer MoS_2, taking advantage of their high performance yet low leakage. MoS_2-FET is highly promising for data-intensive applications involving high-throughput matching and searching, and the TCAM array can be potentially integrated into the 3D circuits for energy-efficient computing.

4.3 Photodetectors

Owing to the atomic thickness, tunable bandgap, and strong light interaction, the practical application of 2D MoS_2 is attractive in environment-friendly optoelectronic devices, especially in photodetectors. For instance, Zhang *et al.*[120] demonstrated high gain phototransistors based on CVD-grown monolayer MoS_2 with a photoresponsivity up to 2200 A/W under the irradiation of 532 nm laser. Lim *et al.*[121] fabricated MoS_2--based visible-light photodetector arrays based on top-gated MoS_2-FETs on a 4-inch SiO_2/Si wafer with a 1-buty-3-methylimidazolium (BmimPF6) liquid dielectric. As shown in Fig. 14, these 100 devices exhibit a narrow photocurrent distribution (0.05–0.1 nA) at an illumination power of 12.5 mW cm^{-2} and a voltage bias of 20 V. Under periodic illumination using a halogen lamp with a tunable power, the photocurrent demonstrated abrupt switching behavior, regardless of the bias voltages. The photocurrent is linearly dependent on the voltage and illumination power due to the increase in the carrier drift velocity and the carrier generation rate, suggesting excellent tunability for multifaceted optoelectronic applications. Liu *et al.*[36] developed MoS_2/PbS hybrid device arrays based on the CVD-synthesized monolayer MoS_2 and PbS quantum dots. The hybrid devices were obtained by spin-coating PbS quantum dots on the MoS_2-FET array and exhibited broad spectral photoresponse (457–1064 nm), rapid response rate, and high responsivity of approximately 1.8×10^4 A W^{-1}. Kim *et al.*[120] demonstrated phototransistors based on the monolayer MoS_2 film with uniform substitutional doping on the 2-inch wafers. The Nb-doped MoS_2 devices exhibited improved optoelectronic performance and stable electrical properties in ambient

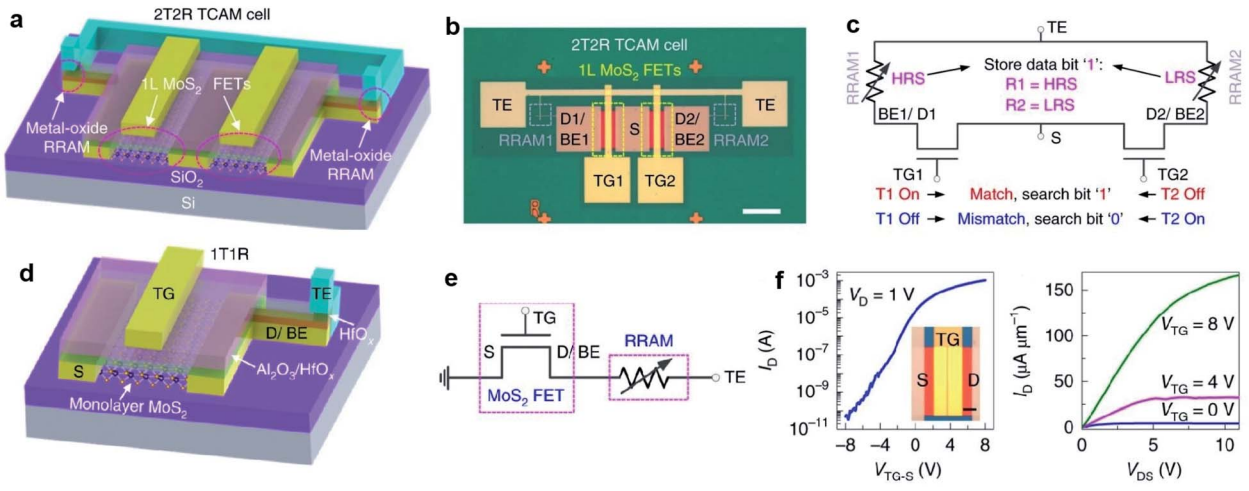

Fig. 13 2T2R TMD-TCAM and 1T1R component with MoS_2-FET. (a) 3D schematic illustration of the 2T2R TCAM cell, with two MoS_2 FETs and two HfO_x-based RRAMs. (b) Top-view optical image of the 2T2R TCAM cell 1. Scale bar: 50 μm. (c) Circuit diagram of the 2T2R TCAM cell showing the definition of match and mismatch states, with the stored data bit '1'. (d) 3D schematic of the 1T1R structure, as a component of the 2T2R TCAM cell. (e) Circuit diagram of the 1T1R structure. Measured representative $I_d - V_{TG\text{-}S}$ (f) and $I_d - V_{ds}$ (g) characteristics of the top-gated monolayer MoS_2-FET with 25 nm HfO_x as the gate dielectric, with $W = 50$ μm, $L = 0.8$ μm, measured at $V_{BG} = 0$ V and with the source grounded.[112] Reproduced with permission from ref. 112, copyright 2019 Springer Nature.

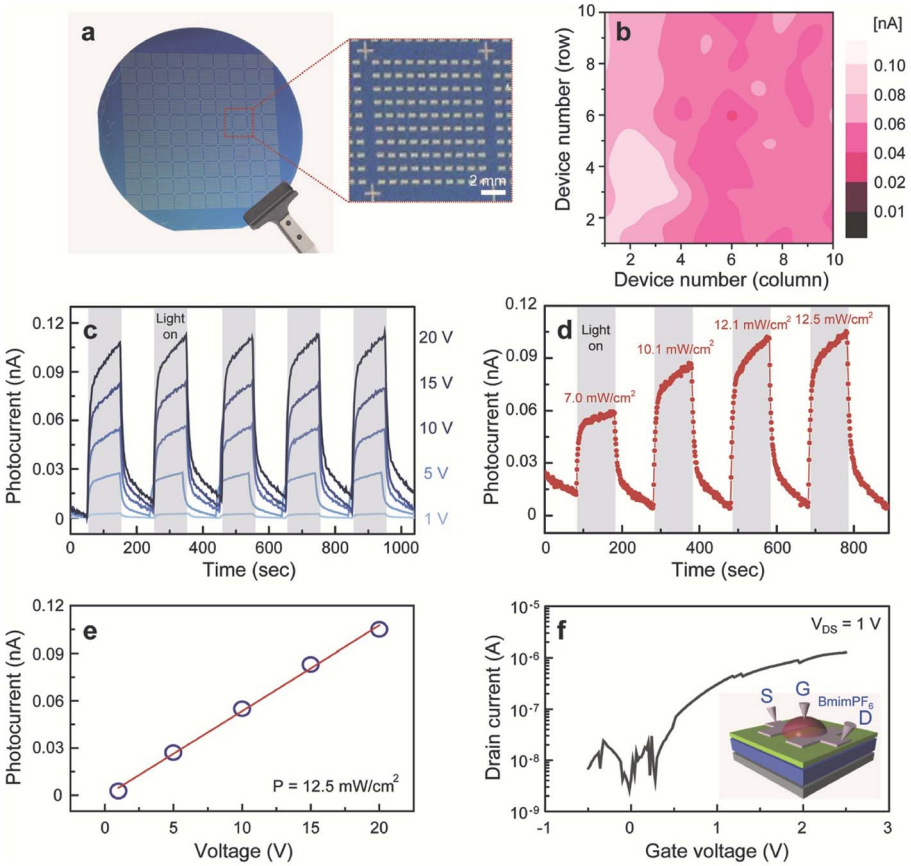

Fig. 14 (a) A photograph of homogeneous MoS_2-based visible-light photodetector arrays on a 4-inch SiO_2/Si wafer. (b) A spatially resolved photocurrent map of the 100 devices recorded at $P = 12.5$ mW cm^{-2} and $V = 20$ V. (c) Representative time-resolved photocurrents of the device recorded at $P = 12.5$ mW cm^{-2} for different bias voltages. (d) Time-dependent photocurrents of the device at $V = 20$ V for different illumination light powers. (e) A plot of device photocurrents as a function of applied voltage. (f) A typical transfer curve of the electrochemically gate-tuned MoS_2-FET at $V_{ds} = 1$ V and (inset) a schematic illustration of MoS_2-FET.[121] Reproduced with permission from ref. 121, copyright 2016 John Wiley and Sons.

conditions. The obtained photoresponsivity, detectivity, and response rate were 5×10^5 A W^{-1}, 5×10^{12} Jones, and 5 m s, respectively, suggesting great feasibility of practical applications based on functionalized 2D MoS_2. Kim *et al.*[123] reported fully printed transparent MoS_2 phototransistor arrays on flexible polyethylene-naphthalate (PEN) substrates. The patterned CVD-synthesized MoS_2 film was transferred onto a PEN substrate, followed by sequentially inkjet-printed poly(3,4-ethylenedioxythiophene) polystyrenesulfonate (PEDOT:PSS) source/drain electrodes, a cross-linked PVP gate dielectric layer, and a PEDOT:PSS top-gate electrode. The printed transparent MoS_2 phototransistors exhibited not only comparable photoresponsivity and photodetectivity over the entire visible range from 400 to 800 nm but also good stability under repetitive bending cycle tests. Furthermore, the performance of MoS_2 photodetectors can be dramatically improved and optimized by forming MoS_2 hybrid heterostructures with graphene, other TMD, *etc.*[124–132] The photoresponsivity, detectivity, and photoresponse of the MoS_2-based hybrid photodetectors can vary by several orders of magnitude depending on the nature of the heterostructures, doping situation, wavelengths, and intensity of the applied incident power. The flexible photodetectors developed from MoS_2 and MoS_2-based hybrid heterostructures provide great potential for the future application in integrated nano-optoelectronic systems and wearable devices.

5. Conclusion and outlook

This review focused on the recent advances in the wafer-scale monolayer MoS_2 synthesis and 2D MoS_2-FET for practical application in electronics and optoelectronics. Wafer-scale monolayer MoS_2 have been realized by different methods, including Au-assisted exfoliation, CVD, thin film sulfurization, MOCVD, VLS method, ALD, and the thermolysis of thiosalts. However, these synthetic methods show different advantages and shortcomings in MoS_2 productions and related costs. Au-assisted exfoliation is convenient in laboratory research, but the repetition rate and size uniformity are difficult to control. CVD is relatively low-cost and possible to mass produce for wide applications, although the growth rate and repetition rate should be improved. The thin film sulfurization method is low-cost but leaves behind some problems, such as difficulty in

controlling the thickness of Mo and the MoO_x layer. MOCVD exhibits great advantages in producing high quality MoS_2 monolayers with high repetition rate, but the long production cycle and special production conditions lead to the high cost. The VLS method seems low-cost in wafer-scale MoS_2 monolayers syntheses, but it is still at the earlier stages of research. ALD can realize wafer-scale MoS_2 monolayers with high repetition rate and good uniformity but in complex production processes with high cost. Thermolysis of thiosalts based on the thermal decomposition of thiosalts results in low cost, but the thickness is difficult to control, leading to low repetition rate for MoS_2 synthesis. Based on the overall consideration of above synthetic methods, CVD and MOCVD present obvious advantages in the synthesis of wafer-scale MoS_2 monolayers with large quantities. Even though there is considerable room for improvement in monolayer MoS_2 synthesis, more and more efforts are being made to optimize the growth conditions and reduce the costs. Thus, wafer-scale high-quality MoS_2 monolayers could be obtained in the near future with the desired thickness, good uniformity, large grain size, and less defects.

The 2D MoS_2-FET array with different configurations utilizes high-quality MoS_2 as the channel and exhibits favorable performance. The MoS_2-FET fabricated from the wafer-scale monolayer MoS_2 demonstrates a mobility of several tens and an on/off ratio even up to 10^{10}, demonstrating great potential in practical applications based on basic MoS_2-FET for modern integrated electronics and flexible optoelectronics, such as logic circuits, memory devices, and photodetectors. Although significant progress has been made in research laboratories for monolayer MoS_2 synthesis and MoS_2-FET devices, the mass production of wafer-scale and high-quality 2D MoS_2-FET is still challenging. In the future, more new investigations are needed to fulfill the usage demands of fundamental studies and practical applications, especially different circuit-level applications. The repeatability of wafer-scale uniform MoS_2 synthesis should be improved for device applications. Functionalization and strain engineering based on wafer-scale monolayer MoS_2 are needed to be considered for the improvement of carrier mobility and PL quantum yields. The precise control of MoS_2 transfer and MoS_2-channel patterning is required for integrated devices fabrication. Further study on the effect of photolithography and the lift-off process on monolayer MoS_2 is also necessary for the performance improvement in basic MoS_2-FET. Looking forward, with more comprehensive advancement in both fundamental research and practical application, 2D MoS_2 film and MoS_2-FET will demonstrate great potential and prospect in realizing MoS_2-based integrated electronics and flexible optoelectronics for modern applications.

Conflicts of interest

There are no conflicts to declare.

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