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Multi-scale analysis of radio-frequency performance of 2D-material based field-effect transistors†

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Two-dimensional materials (2DMs) are a promising alternative to complement and upgrade high-frequency electronics. However, in order to boost their adoption, the availability of numerical tools and physically-based models able to support the experimental activities and to provide them with useful guidelines becomes essential. In this context, we propose a theoretical approach that combines numerical simulations and small-signal modeling to analyze 2DM-based FETs for radio-frequency applications. This multi-scale scheme takes into account non-idealities, such as interface traps, carrier velocity saturation, or short channel effects, by means of self-consistent physics-based numerical calculations that later feed the circuit level via a small-signal model based on the dynamic intrinsic capacitances of the device. At the circuit stage, the possibilities range from the evaluation of the performance of a single device to the design of complex circuits combining multiple transistors. In this work, we validate our scheme against experimental results and exemplify its use and capability assessing the impact of the channel scaling on the performance of MoS_2-based FETs targeting RF applications.

1 Introduction

The emergence of two-dimensional (2D) crystals has raised the expectations for radio-frequency (RF) electronics to move into the THz range. This territory is especially suitable for graphene thanks to its high mobility and saturation velocity which provide an excellent basis for RF operation. In fact, graphene field-effect transistors (GFETs) with several hundreds of GHz cut-off frequencies (f_T) have already been demonstrated.[1,2] Their maximum-oscillation frequency (f_{max}), however, is still low, ≤200 GHz,[3–5] due to the high output conductance produced by the absence of a bandgap.[6] Other 2D materials (2DMs) are postulated as candidates to overcome this problem, being MoS_2, with a bandgap sizable with the number of stacked layers, one of the most appealing and studied alternatives.[7–13]

The possibility to transfer 2DMs in almost any substrate expands the range of applications with respect to conventional RF technologies. Indeed, measurements of MoS_2 devices fabricated on flexible substrates show values of $f_T = 13.5$ GHz and $f_{max} = 10.5$ GHz,[12] not that far from RF performances achieved with the same material on rigid oxides, $f_T = 42$ GHz and $f_{max} = 50$ GHz.[12] Better RF performance would be achievable as further improvements come in MoS_2 and other promising 2DMs such as $PdSe_2$ [14] or $PtSe_2$.[15] In this regard, while 2D semiconductors are constrained by a lower f_T than graphene (due to the superior carrier mobility and saturation velocity of the latter), they are not limited by the gapless band-structure that impacts the current saturation in GFETs leading to a reduced voltage and power gain.[6] Indeed, GFETs have behaved rather poor in terms of f_{max},[6] limiting the highest operating frequency of power amplifiers. It is in this field where more research is required to shed light on the potential of MoS_2 and other TMDs to develop improved RF applications.[16]

In this arena, with the 2D RF technology readiness in its early infancy, the computational tools able to support and rationalize the experimental activities are more essential than ever so as to: (i) interpret the experimental measurements; (ii) gain understanding to improve the capabilities of the devices; (iii) assess their performance and benchmark them against conventional technologies; (iv) explore new device designs; and (v) foresee the RF limits of novel technologies.

In this context, this work presents a multi-scale scheme[17] that combines numerical simulations with a small-signal model to analyze the RF performance of 2DM-based FETs. The fully detailed behavior of the device in the static operation regime obtained from the numerical simulator is combined with a small-signal model specifically developed for 2DM-based FETs.[18] Thus, we are able to

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extend the analysis from a device to a circuit level. To this purpose, we first introduce the theoretical basis of the calculations. Then, the multi-scale method is validated against the dc and high-frequency measurements of MoS_2 transistors reported in (ref. 7). Finally, f_T and f_{max} are evaluated for different gate lengths to analyze the RF potential performance of MoS_2 transistors, and then the main conclusions of the work are outlined.

2 Methods

The multi-scale approach proposed in this work combines (i) the numerical self-consistent solution of the coupled Poisson and continuity equations, including interface traps, carrier velocity saturation and short-channel effects; and (ii) the small-signal compact model that allows for the analysis of multiple interconnected devices in arbitrary designs, and their linear response to complex dynamical inputs.

With the purpose of tightening the approach to the state-of-the-art, and make realistic prospects for that technology, the studied architecture can be taken from an experimental setup of a particular 2DM-based device. Then, a self-consistent numerical simulation in the static regime is carried out, providing detailed information of the main electrostatic and transport physical magnitudes governing the transistor response, including the intrinsic device and the parasitic elements involved to contact it. Next, the intrinsic magnitudes can be extracted and fed into the small-signal model, so to have a distilled description of the device physics. The extrinsic and parasitic elements are thus isolated, and can be later reintroduced in the small-signal model, becoming external, technology-dependent parameters to the core model. That approach enables to project the RF performance of the devices and materials regardless the current technology constraints and provides a flexible and at the same time robust description. The overall picture of the proposed procedure is shown in Fig. 1. The stages are described in more detail hereunder.

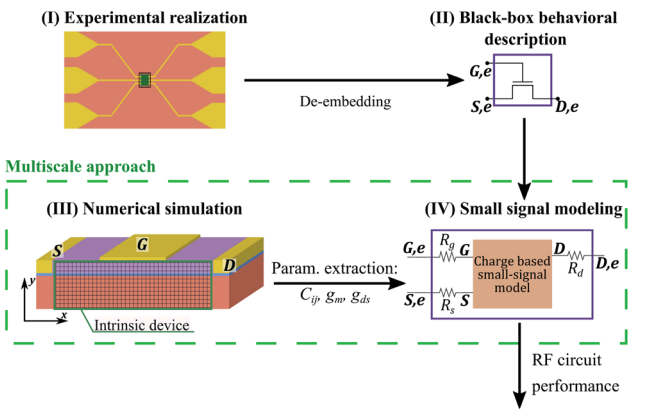

Fig. 1 The multi-scale approach consists on combining a small-signal equivalent circuit and a numerical simulator to describe the behavior of a 2DM-based FETs. The small-signal elements are extracted from the numerical solver and fed into the small-signal equivalent circuit. Importantly, the metal-2DM contact resistances as well as the gate resistance are also included.

2.1 Self-consistent numerical simulator (device level)

2.1.1 Static operation: electrostatics and carrier transport. First, the self-consistent solution of the Poisson and continuity equations is obtained for a given material and device architecture, assuming a drift-diffusion transport regime, which constitutes an accurate description for the state-of-the-art device dimensions. The electrostatic potential, the carrier density profiles, the quasi-Fermi levels for electron and holes, mapped as a function of the spatial position, and the drain-to-source current (I_{DS}) are obtained, for every combination of terminal biases.

The impact of non-idealities is also included in the simulations. In particular, three remarkable effects are considered: interface traps, electric field dependent mobility and access and contact resistances. The impact of the gate electric field on the mobility might be also of relevance as it has been studied in (ref. 19 and 20) but requires a detailed analysis of the scattering processes in MoS_2. For the former, an arbitrary energetic profile for either donors or acceptors traps can be defined to evaluate the surface charge density associated with a certain interface as a function of the electrostatic potential and Fermi level (see S4 at ESI†). As for the mobility, we consider the electric field induced degradation (see S5 at ESI†), following the expression proposed in (ref. 21).

When analyzing a device, the numerical modeling described above is applied to the complete structure, as depicted in Fig. 1, which comprises channel plus access regions and contact resistances. This enables a full self-consistent solution of the electrostatic and transport dependencies in the device. Then, the contact resistances, that are bias independent, are removed with the aim of simulating the intrinsic device and extract its small-signal parameters as explained in the following.

2.1.2 Dynamic operation: terminal charges and intrinsic capacitance scheme. To compute the dynamic operation of the device, the charge associated with each terminal is evaluated as a function of the different biases in order to subsequently determine their intrinsic capacitances.[22] In particular, the charges associated with the gate, drain and source terminals are calculated following the Ward–Dutton charge partition scheme, which ensures the charge conservation[23] (see S7–S9 at ESI†).

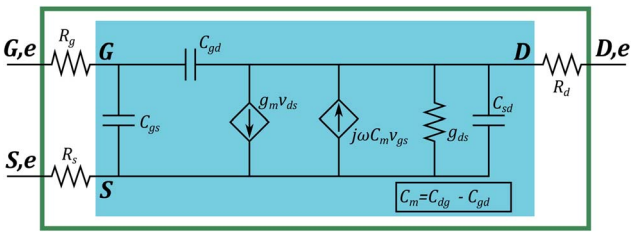

Fig. 2 Small-signal equivalent circuit suited to 2DM-based FETs.[24] The equivalent circuit of the intrinsic device is framed in blue. The small-signal elements are: $g_m = \partial I_{DS}/\partial V_{gs}$ transconductance; $g_{DS} = \partial I_{DS}/\partial V_{DS}$ output conductance; and C_{gs}, C_{gd}, C_{sd}, and C_{dg} intrinsic capacitances. R_g is the gate resistance and R_d and R_s account for the contact resistances of the drain and source, respectively. They connect the intrinsic (noted G, D and S) and extrinsic (G,e, D,e and S,e) gate, drain and source terminals.

Then, we compute the reference-independent dynamic description of a three-terminal device by calculating the intrinsic capacitances, C_{ij}, as the charge derivative at terminal i with respect to a varying voltage applied to terminal j, assuming that the bias at any other terminal remains constant:

$$C_{ij} = \begin{cases} \dfrac{\partial Q_i}{\partial V_j} & i = j \\ -\dfrac{\partial Q_i}{\partial V_j} & i \neq j \end{cases}, \quad i,\ j = g,\ d,\ s \qquad (1)$$

where the subscripts g, d and s stand for gate, drain and source, respectively.[18]

2.2 Small-signal model (circuit level)

The small-signal equivalent circuit of a 2DM-based FET is shown in Fig. 2.[24] It allows to treat the current and charge variations due to a time-varying input signal in terms of linear circuit elements, *i.e.* conductance, and capacitance elements (see ESI†). Two main features must be highlighted: (i) the metal contact resistances are included, an aspect of utmost importance when dealing with low dimensional FETs[25] and (ii) the small-signal model guarantees charge conservation and takes into account non-reciprocal capacitances. The latter is not considered in Meyer[26] and Meyer-like capacitance models making them inaccurate when trying to predict the RF performance of GFETs, where the impact of transcapacitances is critical. Indeed, the analysis of the intrinsic capacitances of a MoS_2 FET addressed in (ref. 18) shows that reciprocity between C_{gd} and C_{dg} cannot be assumed for all transistor operation regions. Such an equivalent circuit combined with our detailed self-consistent physics-based simulator allows the accurate electrical simulation of 2DM-based FETs for linear RF applications.[27]

Considering the equivalent circuit shown in Fig. 2 as a two-port network connected in a common-source configuration allows the assessment of two main figures of merit for RF devices: the cut-off frequency, f_T, and the maximum oscillation frequency, f_{max}, evaluated from the current and power gain, respectively.

3 Results and discussion

Before projecting the potential performance of MoS_2 FETs for RF applications, the multi-scale scheme is validated against the experimental data reported in (ref. 7). The device is a monolayer MoS_2 FET with 30 nm-thick top gate oxide (HfO_2) and a 270 nm-thick substrate (SiO_2). The total length of the device is L_{ch} = 340 nm, with a 240 nm-long channel plus two access regions 50 nm-long each. The measured contact resistance and electron mobility are 2 kΩ μm and 85 $cm^2\ V^{-1}\ s^{-1}$, respectively.

With the intention of emulating the effect of the contact resistances (R_C) in the numerical simulations, two doped regions are added at both edges of the semiconductor layer and its doping is modified to adjust $R_C = R_s = R_d$ to the reported experimental value (2 kΩ μm). Interface traps are a relevant magnitude in MoS_2 devices, as it is discussed in (ref. 28 and 29),

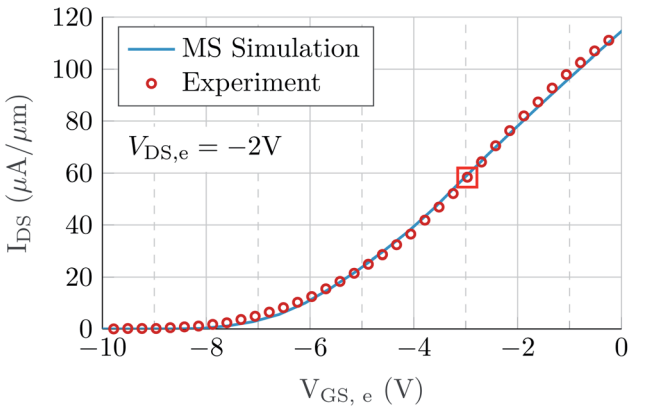

Fig. 3 Experimental data of a MoS_2 FET reported in (ref. 7) (symbols) and results from the numerical solver (line). The operating point for RF experimental measurements is indicated by a square.

although more effort is still required to achieve a deeper and more comprehensive understanding. However, as the detailed distribution of interface traps is not the main goal of this work, we have considered a constant energetic profile in both interfaces of the channel that provides the best agreement with the experimental data.[30] In particular, we set two energetic profiles: (i) at the top gate insulator interface, a constant energetic profile of donors traps with $D_{it} = 10^{12}$ cm^{-2} eV^{-1} is considered from mid-gap up to 0.57 eV towards the conduction band edge; and (ii) at the substrate interface, a constant energetic profile also of donor traps from midgap to the conduction band edge (*i.e.*

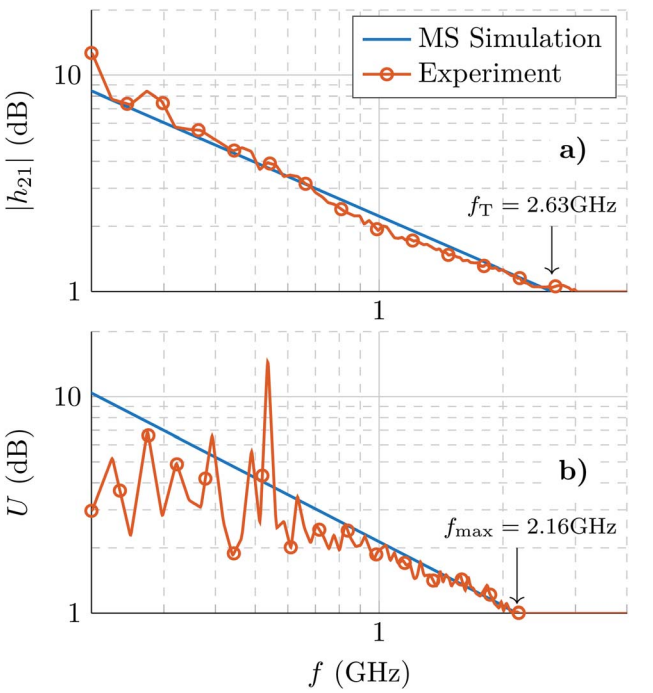

Fig. 4 (a) Current gain h_{21} and (b) Mason's unilateral gain U calculated using the multi-scale (MS) approach (blue lines) and compared against the experimental values extracted from (ref. 7) (red lines with symbols). The arrows indicate the values of f_T and f_{max}.

Table 1 Small-signal parameters extracted from the self-consistent numerical simulator

Parameter	Value	Parameter	Value
g_m	0.0828 mS μm^{-1}	g_{DS}	0.5047 mS μm^{-1}
C_{gd}	0.280 fF μm^{-1}	C_{dg}	0.442 fF μm^{-1}
C_{sd}	−0.071 fF μm^{-1}	C_{gs}	0.604 fF μm^{-1}

0.9 eV above midgap) is considered with $D_{it} = 2.5 \times 10^{11}$ cm^{-2} eV^{-1}. The channel is undoped with electron mobility $\mu = 85$ cm^2 V^{-1} s^{-1}, saturation velocity $v_{sat} = 2.8 \times 10^6$ cm s^{-1}, electron effective mass $m^* = 0.61$ m$_0$ and bandgap width $E_g = 1.8$ eV. The experimental data and the simulation results are depicted in Fig. 3, showing a very good agreement with the bias point employed in the RF experimental characterization, $V_{GS,e} = -3$ V and $V_{DS,e} = 2$ V, marked by a square. Remarkably, at this bias point the resistance associated with the access regions (as computed from the self-consistent simulations), have comparable values to R_C, reaching $R_{s,acc} = 3.3$ kΩ μm and $R_{d,acc} = 3.1$ kΩ μm at the source and drain ends, respectively and being rather bias dependent. This point highlights the strong impact that these gate-underlapped areas can produce on the RF performance of the device.[31]

Using these results, we can assess the proposed approach by confronting the RF figures of merit resulting from it with those experimentally characterized and reported in (ref. 7). To this purpose, the values of the small-signal parameters of the device are first extracted following the procedure previously described and fed into the small-signal model (Table 1).

The current gain (h_{21}) and the Mason's unilateral gain (U) obtained from the multi-scale scheme, *i.e.* combining the small-signal-model and numerical-solver analysis, are depicted in Fig. 4 along with the experimental data,[7] demonstrating an excellent correspondence and holding the soundness of the theoretical procedure. f_T and f_{max}, obtained from the numerical calculations, marked within the figures, are also shown in very close agreement with the reported measurements: $f_T = 2.63$ GHz and $f_{max} = 2.16$ GHz.

Once the multi-scale approach is validated, we exemplify its utility by proceeding with a projective analysis of the potential of MoS_2 FETs for RF applications; in particular extracting f_T and f_{max} for devices with channel lengths ranging from 10 μm down to 50 nm. In order to focus on the material intrinsic capabilities and to reduce the role of extrinsic resistive elements in the predicted behavior, the 2D-FET is improved by reducing the access regions length to 5 nm and setting contact resistances to 100 Ω μm, which is the desirable value for 2DMs to compete on the RF arena[25] and not so far from the minimum value achieved experimentally, 240 Ω μm,[32] and well above the theoretical limit of 30 Ω μm.[33]

Fig. 5 shows f_T as a function of the gate length, L_g. Each marker of the solid curves corresponds to the result achieved from the application of the multi-scale procedure to a device with a particular L_g under a given V_{DS} and considering the V_{GS} bias that causes the maximum transconductance. Along with these results, we show the physical limit represented by $v_{sat}/2\pi L_g$, *i.e.* the inverse of the minimum transit time of charge carriers in the channel, that also serves as a guide for the eyes of the $1/L_g$ scaling; and the $1/L_g^2$ trend that conventionally commands the performance in longer channels. We also show, for the sake of comparison, the results for different experimental devices based on graphene, MoS_2 and III–V compounds taken from the literature (solid and hollow symbols).[6,9,12,34–41]

According to Fig. 5, a change in the scaling trend of MoS_2 f_T, from $1/L_g^2$ for long channels to $1/L_g$ for short channels can be expected. This can be explained due to the f_T rough dependence on $\sim g_m/2\pi(C_{gs} + C_{gd})$. For long channels, g_m is proportional to $1/L_g$, and $(C_{gs} + C_{gd})$ to L_g, resulting in a trend $\sim 1/L_g^2$; while for short channels g_m saturates and f_T scales only with the capacitive response, to $1/L_g$. The transition from $1/L_g^2$ to $1/L_g$ is observed in MoS_2 still for long channels, *i.e.* $L_g \approx 1$ μm due to g_m early saturation.[6] The v_{sat} impact is also revealed in the dependence of f_T on V_{DS}: when the channel length is scaled, the performance is barely improved with V_{DS}, as it approaches the physical limit, *i.e.*, the carrier drift velocity cannot increase any further with the electric field. The values predicted are in good agreement with experimental state-of-the-art RF measurements of MoS_2 devices, demonstrating the prediction capability of the presented tool, that can be exploited to study any candidate in the 2DM realm. The experimental results shown for graphene and III–V compounds contextualize the progresses already achieved by MoS_2 electronics and the limitations associated to its lower saturation velocity.

Concerning f_{max}, Fig. 6 plots it as a function of L_g for different V_{DS} biases, together with the $1/L_g$ and $1/\sqrt{L_g}$ lines used as a guide for the eyes, and the experimental results from different technologies. For long channel devices, f_{max} varies with $1/L_g$ as f_{max} depends roughly on $\sim \sqrt{f_T/(8\pi R_g C_{gd})}$ considering that the gate resistance R_g si proportional to $1/L_g$.[42] For short channel devices, $L_g < 500$ nm, the trend changes from

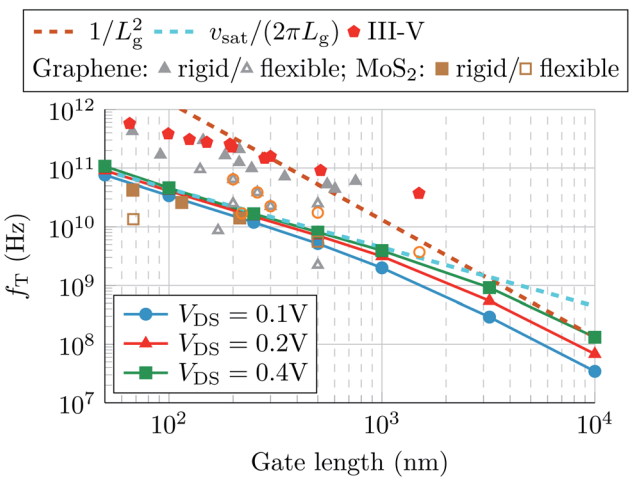

Fig. 5 Cut-off frequency f_T as a function of the gate length for different drain biases (solid lines with markers). The $1/L_g^2$ trend and the physical limit (that also serves as a guideline for the $1/L_g$ scaling) are also depicted (dashed lines). Solid and hollow markers correspond to experimental works.[6,9,12,34–41]

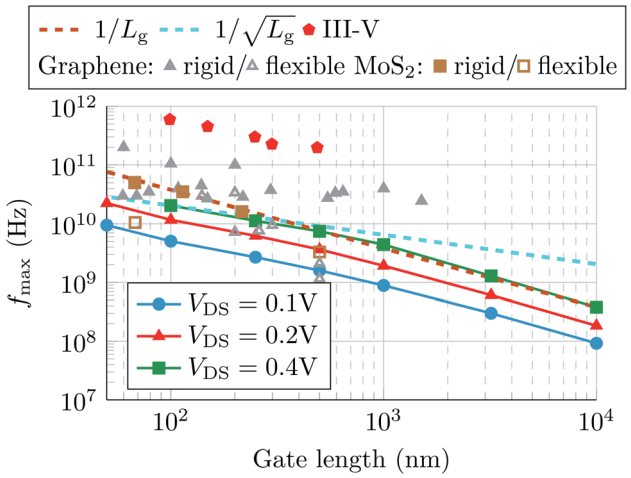

Fig. 6 Maximum oscillation frequency f_{max} as a function of the gate length for different drain biases (solid lines with markers). The $1/L_g$ and $1/\sqrt{L_g}$ trends are indicated by dashed lines. Solid and hollow markers correspond to experimental works.[6,9,12,34–41]

$1/L_g$ to $1/\sqrt{L_g}$, showing a small over-increment at the limit of the diffusive regime, as it has also been predicted for GFETs in (ref. 43). Although the experimental values correspond to diverse technologies and measured under different operating bias points, the measurements show good agreement with our predictions. More importantly, MoS_2 FETs demonstrate to be competitive or even to overcome graphene devices performance for the smaller channel lengths, thanks to their larger output conductance, postulating MoS_2 as a worthy 2D alternative for RF power circuits, being nevertheless still far from consolidated III–V architectures.

4 Conclusion

We reported a multi-scale approach that combines small-signal and numerical simulations in order to describe in detail the behavior of 2DM-based devices for RF applications. Both levels of abstraction are precisely combined, so the main features included in the Poisson-drift-diffusion system are extended to circuit level simulations. The proposed scheme was validated against experimental data, showing an excellent agreement with dc and RF measurements. The multi-scale simulation tool was then employed to project the impact of channel length scaling on the RF performance of a MoS_2 based FET with improved extrinsic behavior by considering a reduction in the contact resistance and shorter gate under-lapped access regions, so to understand and assess the intrinsic limits of the 2DMs. The resulting f_T *vs.* L_g curves show a change in their trend from $1/L_g^2$ to $1/L_g$ and a saturated behavior with respect to V_{DS} for low L_g, due to the constraining saturation velocity. When comparing the results with those achieved in experimental devices, the reduction of the access regions and contact resistances implies an increase of almost 10-fold in f_T with respect to the experimental sample.[7,10] On the other hand, the f_{max} *vs.* L_g curves present a scaling-trend varying from $1/L_g$ to $1/\sqrt{L_g}$, that is impacted by the up-scaling of the gate resistance. An improvement of the RF performance of MoS_2-based devices could be achieved by enhancing the crystal transport properties, *e.g.*, higher mobility and saturation velocity. Hence, the multi-level approach presented here constitutes a versatile platform for evaluating the impact of scaling on the RF performance of any 2D material based FET. In addition to channel scaling, the capabilities of this approach can be extended to asses the impact of surface defects and even mechanical strain in devices fabricated on flexible substrates. Furthermore, it enables the design and assessment of sophisticated RF circuits based on such devices.

Conflicts of interest

Authors do not have conflicts of interest to declare.

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