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# Comparison of diverse resistive switching characteristics and demonstration of transitions among them in Al-incorporated HfO<sub>2</sub>-based resistive switching memory for neuromorphic applications†

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Diverse resistive switching behaviors are observed in the Pt/HfAlO<sub>x</sub>/TiN memory device depending on the compliance current, the sweep voltage amplitude, and the bias polarity. We extensively compare three types of resistive switching characteristics in a Pt/HfAlO<sub>x</sub>/TiN device in terms of endurance, ON/OFF ratio, linear conductance update, and read margin in a cross-point array structure for synaptic device applications. The bipolar resistive switching under positive set and negative reset shows better linear synaptic weight updates due to gradual switching than the bipolar resistive switching at the opposite polarity. The complementary resistive switching shows a higher read margin due to the current suppression at a low voltage regime. In addition, the potentiation and the depression can be adjusted at the same voltage polarity for a hardware neuromorphic system. Finally, we demonstrate the transition between bipolar resistive switching and complementary resistive switching, which could provide flexibility for different applications.

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## Introduction

Compared to traditional non-volatile memories<sup>1</sup> such as NAND Flash, resistive switching memory (RRAM) is considered to be more promising in terms of its low power consumption<sup>2</sup> and fast switching speed.<sup>3</sup> It is also quite competitive in terms of scalability and multi-level cells (MLC).<sup>4</sup> RRAM shows different types of resistive switching from various insulating mediums such as metal oxide,<sup>5</sup> semiconductor materials, organic materials, and 2D materials.<sup>6</sup> The switching behaviors are mainly classified into progressive switching and abrupt switching during set and reset. Progressive switching is particularly suitable for MLC implementation in non-volatile memory applications.<sup>7</sup> Multi-conductance-states in an RRAM device are also extensively utilized as electronic synapses in neuromorphic systems,<sup>8</sup> which have the potential to replace von Neumann computing in the near future. Neuromorphic engineering emulates a neuro-biological architecture to implement an energy-efficient computing system with parallel data processing. Non-volatile memory devices such as Flash memory<sup>9</sup> and

resistance-type new memories can act as biological synapses in a nervous system by storing and change the weight for a long time.<sup>10</sup> Among them, RRAM-based artificial electronic synapses have shown many attractive benefits in neuromorphic computing,<sup>11</sup> *i.e.*, a simple structure, low energy consumption,<sup>12</sup> multi-level storage,<sup>13</sup> and good CMOS compatibility<sup>14</sup> with high-density integration.<sup>14</sup>

The resistive switching is largely divided into three categories. Unipolar resistive switching (URS) occurs in the same polarity in which the reset process uses Joule heating with high current. Bipolar resistive switching (BRS) occurs in different polarities, which is dominantly driven by electric field. The reset is completed after set process in the same polarity for complementary resistive switching (CRS).<sup>13</sup>

Among the many resistive switching materials, HfO<sub>2</sub> is a well-proven material with excellent reproducibility and repeatability, and it has been studied for a long time for non-volatile storage memory applications as well as for high-*k* gate dielectrics in CMOS.<sup>15,16</sup> However, the defect controlled switching-based RRAM devices including metal oxides cannot avoid the variation of switching parameters because of the stochastic nature.<sup>17</sup>

Several approaches have been applied to further improve the non-volatile memory properties of HfO<sub>2</sub> RRAM. The dopant of another material such as Al into an HfO<sub>2</sub> layer or the bilayer Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> structure can enhance the uniformity of set and reset switching by stabilizing the conductive filament.<sup>18–21</sup> The

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use of  $\text{Al}_2\text{O}_3$ ,<sup>19</sup> which has a larger band gap than  $\text{HfO}_2$ , can lead to improved resistive switching properties, such as low power consumption and nonlinear  $I$ - $V$ .<sup>19</sup> Furthermore, synaptic characteristics have been reported in several  $\text{HfO}_2$ -based RRAM devices.<sup>7,21</sup>

In this work, we characterize the various resistive switching behaviors of an Al-doped  $\text{HfO}_2$  ( $\text{HfAlO}_x$ )-based RRAM device for neuromorphic computing. The switching behaviors are classified into three types by controlling the compliance current (CC) and the voltage polarity. A single device that can have various resistive switching characteristics determined by the operating conditions is advantageous in the sense that it can be flexibly applied to various applications. Two bipolar resistive switching at positive set and negative set and a complementary resistive switching are evaluated in terms of the ON/OFF ratio, endurance cycle, read margin, and the nonlinearity and variation of potentiation and depression for synaptic device application in a hardware based-neuromorphic system. In addition, we experimentally demonstrate the transition between BRS and CRS.

## Experimental section

The Pt/ $\text{HfAlO}_x$ /TiN device was fabricated as follows. A 100 nm-thick TiN was deposited by DC sputtering on a  $\text{SiO}_2/\text{Si}$  wafer. A 7 nm-thick high- $k$   $\text{HfAlO}_x$  film was then accurately deposited by atomic layer deposition (ALD). The  $\text{HfO}_2$  layer reacted with TEMAHf and  $\text{H}_2\text{O}$ . One cycle is composed of TEMAHf (0.5 s)-pulse (35 s)- $\text{H}_2\text{O}$  (0.3 s)-pulse (35 s) for ALD  $\text{HfO}_2$  layer. The  $\text{Al}_2\text{O}_3$  reacted with TEMAH and  $\text{H}_2\text{O}$ . One cycle is composed of TMA (0.2 s)-pulse (15 s)- $\text{H}_2\text{O}$  (0.2 s)-pulse (15 s) for ALD  $\text{Al}_2\text{O}_3$  layer. For the  $\text{HfAlO}_x$  film, one cycle of  $\text{HfO}_2$  and then five cycles of  $\text{Al}_2\text{O}_3$  were alternately deposited for a total of 15 times. Next, a 100 nm thick Pt top electrode was deposited by an e-beam evaporator and patterned by a shadow mask containing circular patterns with a diameter of 100  $\mu\text{m}$ . All the electrical properties, including the DC and transient characteristics, were used with a Keithley 4200-SCS semiconductor parameter analyzer and in pulse mode using a 4225-PMU ultrafast module. All measurements were performed at room temperature and ambient atmosphere. The bias was applied on the Pt top electrode while the TiN bottom electrode was grounded.

## Results and discussion

Fig. 1(a) shows the structure of the Pt/ $\text{HfAlO}_x$ /TiN device. The device stack is well confirmed by the high-resolution transmission electron microscope (HRTEM) image shown in Fig. 1(b). Further, each element (Pt, Hf, Al, O, Ti, and N) is well scanned by energy dispersive X-ray spectroscopy (EDS) analysis, as illustrated in Fig. 1(c).

First, DC bias sweeps are applied to the device to characterize its typical  $I$ - $V$  curves for electrical analysis, as shown in Fig. 2(a). The initial forming-free behavior on pristine cell and high resistance state (HRS) are found. After applying the CC of 700  $\mu\text{A}$ , the Pt/ $\text{HfAlO}_x$ /TiN device shows stable BRS up to 200 cycles

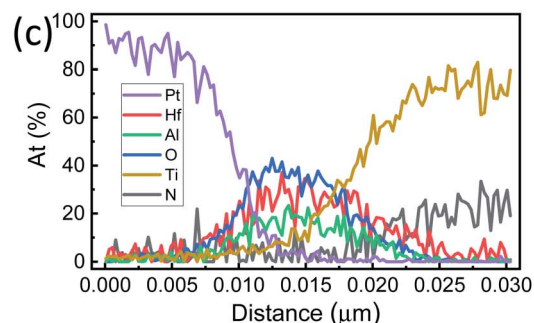
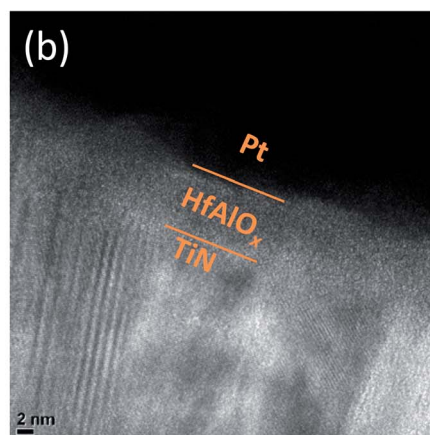
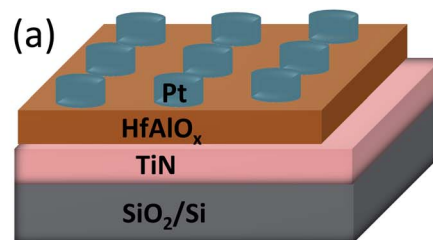


Fig. 1 Device configuration of Pt/ $\text{HfAlO}_x$ /TiN device: (a) schematic of the device stack, (b) HRTEM image, (c) EDS line scan.

with an ON/OFF ratio of about 10 at 0.5 V. The device switches from HRS to low resistance state (LRS) at about  $-1.5$  V for the set process. The device starts to return to HRS with positive sweep for reset. Note that this switching (negative set and positive reset) is classified as type 1 (BRS1) in this work. The multi-level states in the RRAM cell can increase the memory density at the same cell size, which is useful for storage memory

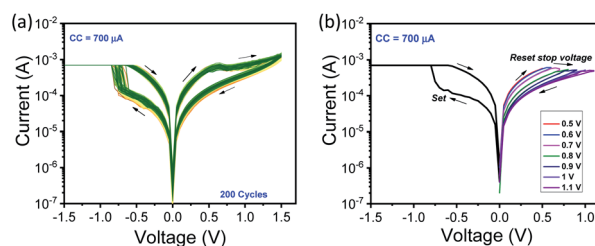


Fig. 2 (a)  $I$ - $V$  characteristics of the Pt/ $\text{HfAlO}_x$ /TiN device by negative set and positive reset (type 1, BRS1). (b) Multilevel  $I$ - $V$  curves by reset stop voltage from 0.5 V to 1.1 V.



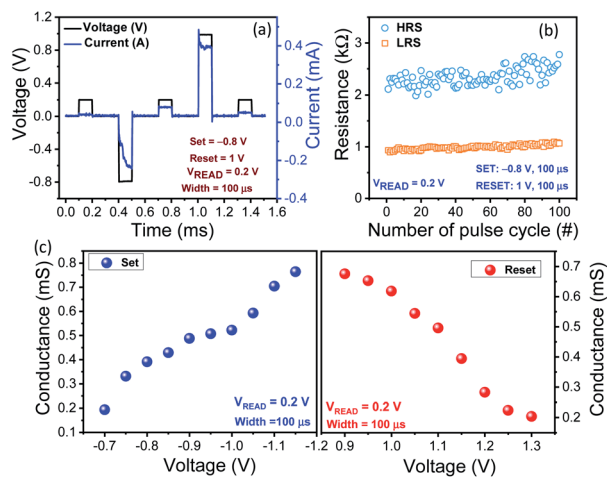


Fig. 3 Pulse responses of the Pt/HfAlO<sub>x</sub>/TiN device in type 1. (a) Set and reset switching in pulse mode, (b) endurance cycle in pulse mode, (c) MLC with difference conductance levels driven by pulse response.

applications.<sup>22</sup> Moreover, MLC improves the computing system performance in hardware neuromorphic systems.<sup>23</sup> Fig. 2(b) shows the multi-level switching by controlling reset voltage switching. The set process occurs in an abrupt manner, and it is relatively difficult to control the set voltage for MLC.<sup>24</sup> Conversely, after the set process, the current gradually decreases by a continuous reset process while positively increasing the step voltage of 0.1 V. HRS and LRS follow Schottky emission and ohmic conduction, respectively, as reported in the previous literature<sup>25,26</sup> (see Fig. S1, ESI†).

For more practical memory switching operation, pulse measurements are conducted on the Pt/HfAlO<sub>x</sub>/TiN device. Fig. 3(a) shows the set and reset transient switching driven by voltage pulse input. The low current at the initial state is monitored by read pulse (0.2 V, 100 μs), and the current increases by the same read voltage after the set pulse (-0.8 V, 100 μs) is applied. Similarly, the current decreases are confirmed by the same read pulse after reset pulse (1 V, 100 μs). The endurance is conducted by up to 100 cycles for transitions between two states (ON: about 1 kΩ, OFF: 2 kΩ–2.8 kΩ) by applying the pulse scheme displayed in Fig. 3(a), as shown in Fig. 3(b). The ON/OFF ratio can be increased by using higher voltage amplitude. The multi-level conductance values are obtained by varying the voltage amplitudes (-0.7 V to -1.15 V) with an identical pulse width of 100 μs for the set process, and by varying the voltage amplitudes (0.9 V–1.3 V) for the reset process.

Next, we emulate important biological synapse functions, such as long-term potentiation (LTP), long-term depression (LTD), and paired pulse facilitation (PPF), in a Pt/HfAlO<sub>x</sub>/TiN device, an artificial electronic device.<sup>27</sup> Fig. 4(a) shows a schematic of a biological synapse, a pre-synaptic neuron, and a post-synaptic neuron. The synapse acting as neuronal junction or bridge controls the electrical or chemical signal between two neurons.<sup>28</sup> Synapses regulate connection strength and are involved in learning and memory in the human brain. Similarly,

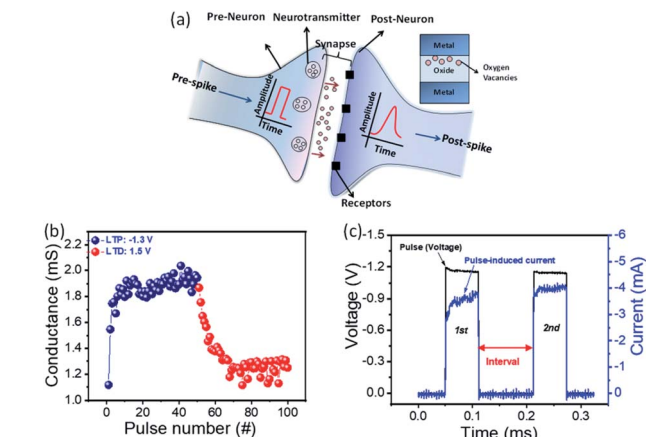


Fig. 4 Synaptic characteristics of the Pt/HfAlO<sub>x</sub>/TiN device in type 1. (a) Schematic of the biological synapse between pre-neuron and post-neuron, (b) change in the conductance of 100 consecutive identical pulse responses for LTP and LTD, (c) PPF function emulated by artificial electron device.

the metal-insulator-metal (MIM) capacitance structure can facilitate weight (conductance) adjustment through external pulse inputs.<sup>29</sup> LTP and LTD are key features for adjusting the neuronal synaptic plasticity.<sup>30</sup> Fig. 4(b) shows the LTP and LTD curve driven by each of the identical 50 pulses. Fifty consecutive conductance values are measured at a  $V_{\text{READ}}$  of 0.2 V after potentiating the set pulse (-1.3 V, 100 μs). For LTD, depressing reset pulses (1.5 V, 100 μs) and a  $V_{\text{READ}}$  of 0.2 V are used. The conductance values are tuned from 1.116 mS to 2.028 mS. In the LTP, the conductance is significantly changed at the beginning of the pulse and a large variation is observed. The variation of LTP and LTD is due to the stochastic behaviors from resistive switching using the movement of oxygen vacancies. Especially, the potentiation (set process) has large variation due to the abrupt change in filamentary type.<sup>17</sup>

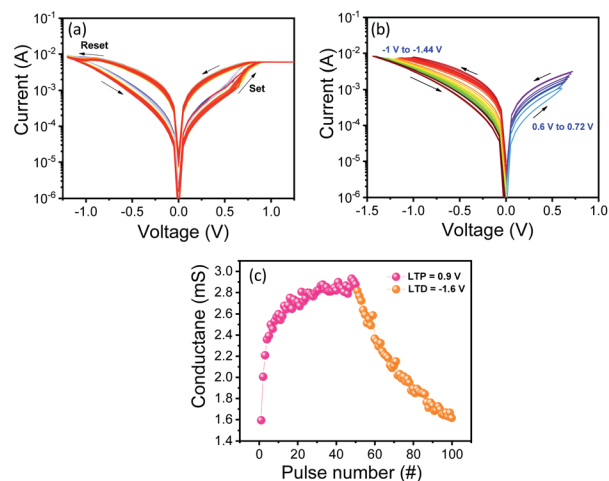


Fig. 5 (a) BRS  $I$ - $V$  characteristics of the Pt/HfAlO<sub>x</sub>/TiN device by positive-set and negative set (type 2, BRS2), (b) MLC characteristics by controlling set (positive bias) and reset (negative bias) stop voltages, (c) LTP and LTD curve by identical pulses (LTP: 0.9 V and LTD: -1.6 V).



The LTP curve is consistent with the abrupt set process of the  $I$ - $V$  curve shown in Fig. 2(a). There are large variations in the LTP and LTD curves. For example, the conductance in some points decreases with the set pulse and increases with the reset pulse. Next, we emulate PPF, which is associated with short-term plasticity.<sup>31</sup> The second current is higher than the first one when two identical paired pulses (voltage:  $-1.3$  V, width:  $100$   $\mu$ s) are applied on the artificial synaptic device (Pt/HfAlO<sub>x</sub>/TiN device). This enhancement, which is also known as facilitation in the nervous system, occurs because the interval time is shorter than the recovery time and the device has a non-volatile property.<sup>32</sup>

Resistive switching also occurs in the Pt/HfAlO<sub>x</sub>/TiN device at the positive set and negative reset process, which is defined as type 2 (BRS2). Fig. 5(a) shows the typical type 2 BRS characteristics. The more gradual switching is observed for set switching, so we can control the set stop voltage ( $0.6$  V to  $0.72$  V) as well as the reset stop voltage ( $-1$  V to  $-1.44$  V) to obtain different current levels, as shown in Fig. 5(b). In addition, LTP and LTD are obtained in a similar manner for type 1. Here, 50 consecutive increases in conductance for LTP ( $0.9$  V,  $100$   $\mu$ s) and 50 decreases in conductance for LTD ( $-1.6$  V,  $100$   $\mu$ s) are controlled to confirm the synaptic plasticity of the artificial electronic synapse.<sup>33</sup> The conductance values are varied from  $1.589$  mS to  $2.966$  mS with substantially lower fluctuation than that used in type 1.

To evaluate the CC effect on resistive switching behaviours, a high CC of  $2$  mA is applied on a pristine cell by DC voltage sweep in a negative regime. The device shows an extraordinary CRS.<sup>34</sup> The repeatable CRS up to 50 consecutive cycles is obtained; here, the set occurs first, then the reset occurs at a larger voltage in the same polarity at both positive and negative regimes. Unlike conventional BRS, the CRS has the advantage of suppressing leakage current when applying a half-bias scheme in a cross-point structure, because the current is suppressed at a low voltage regime before the set process.<sup>35</sup> Moreover, to emulate the synaptic behaviour in the CRS curve, we design the applied voltage with different amplitudes at the same polarity. The conductance levels for the LTP and LTD curve are well controlled by 50 identical pulse responses (LTP:  $0.9$  V and  $100$   $\mu$ s, LTD:  $0.9$  V and  $100$   $\mu$ s) in a manner similar to those used for type 1 (BRS1) and type 2 (BRS2). The conductance range can be controllable from  $0.745$  mS to  $1.382$  mS by this pulse condition. In addition, CRS is observed in pulse train mode (see Fig. S2,

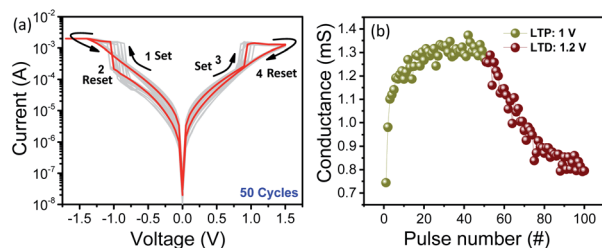


Fig. 6 (a) CRS  $I$ - $V$  curves of the Pt/HfAlO<sub>x</sub>/TiN device in type 3 (CRS), (b) LTP and LTD curve by identical pulse responses in same polarity (LTP:  $1$  V and LTD:  $1.2$  V).

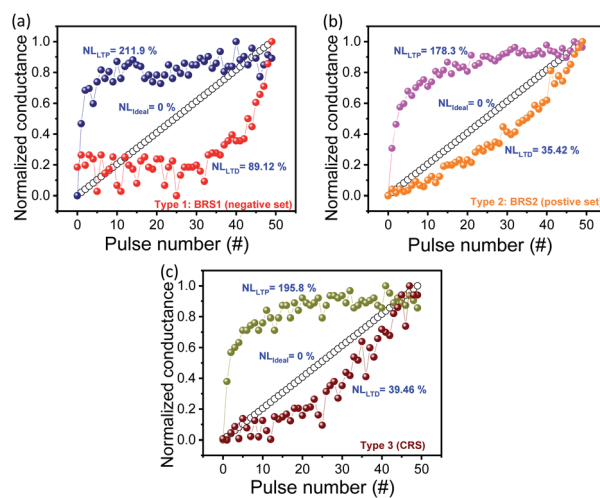


Fig. 7 Normalized conductance of (a) type 1, (b) type 2, and (c) type 3 to extract the NL.

ESI<sup>†</sup>). It should be noted that the conductance can only be increased and decreased by the magnitude of the voltage at the same polarity; this has the advantage of simplifying the peripheral circuit driving the synaptic device (Fig. 6).<sup>36</sup>

The linear weight update of the synaptic device is important for implementing high learning accuracy in a hardware neuromorphic system.<sup>37,38</sup> To evaluate the conductance update for three types (BRS1, BRS2, and CRS) in the LTP and LTD curves shown in Fig. 7(a)-(c), respectively, the nonlinearity (NL) is defined in the following equation:

$$NL = \text{average} \left( \left| \frac{G - G_{\text{LINEAR}}}{G} \right| \times 100 \right) \quad (1)$$

Here,  $G$  and  $G_{\text{LINEAR}}$  are the measurement conductance value and the conductance with ideal weight update, respectively. Type 1 shows the highest NL value because of the abrupt transition for the set process. Type 3 shows a nearly similar NL, but the variation of weight update is higher than that of type 2.

For the high-density integration of the storage memory device, the sneak current issue in the cross-point array structure can be mitigated by CRS.<sup>39</sup> The sneak current flows when a partial voltage is applied to adjacent cells of the target cell shown in Fig. 8(a). If all adjacent cells have LRS, the sneak current path leakage problem could be severe. To demonstrate

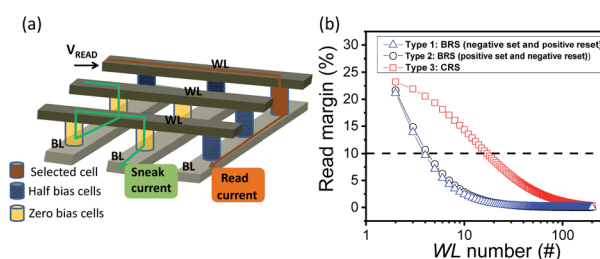


Fig. 8 (a) Sneak current in cross-point structure, (b) read margin as a function of the number of WL for three types of switching.



Table 1 Comparison of three types of  $I$ - $V$  characteristics at different current compliance

	Type 1 (BRS1)	Type 2 (BRS2)	Type 3 (CRS)
ON/OFF ratio	>10	<10	<10
Endurance cycles	200	100	50
Number of word lines at read margin (10%)	4	3	17
LTP/LTD NL (%)	211.9/89.12	178.3/35.42	195.8/39.46
LTP/LTD weight update error (%)	44.9/40.8	38.78/24.48	40.8/44.89

a better read margin in CRS, a half-bias scheme is employed in the cross-point array structure.<sup>40</sup> The worst case read margin<sup>41</sup> is calculated as a function of the word line (WL) or bit line (BL) number for the three types of switching displayed in Fig. 8(b). CRS (type 3) shows the highest read margin among them because the current is suppressed at a low voltage regime. However, a CRS curve operating at a lower current as well as an additional selector element will be connected to each memory cell to ensure a larger array size.<sup>40</sup> Table 1 compares the ON/OFF ratio, the endurance cycle, the linearity, the weight update error rate of potentiation and depression, and the read margin for the three types of switching.

The Pt/HfAlO<sub>x</sub>/TiN device shows good stability as well as multilevel and tunable switching based on different measurement conditions such as CC,<sup>42</sup> bias polarity, and voltage sweep range,<sup>43</sup> which are explained in the flow chart presented in the inset in Fig. 9. LRS current is well controlled by CC (see Fig. S3, ESI<sup>†</sup>). By increasing CC from 700  $\mu$ A to 2 mA, the BRS1 (200 cycles) behavior turns to CRS (50 cycles), as shown in Fig. 9. We can then select type 1 or type 2 from CRS depending on the CC. The  $I$ - $V$  curves (type 2, positive set and negative reset) are similar to the interface-type when a smaller voltage stop is used at positive bias. Interface-type switching is well known for its poor retention,<sup>44</sup> and we confirmed the current decay by short-term memory effect in pulse train (see Fig. S4, ESI<sup>†</sup>). There is no specific CC because the switching occurs before the effective current change. Fifty endurance cycles are observed in this switching mode, as shown in Fig. 9. Further, when a higher CC of 4 mA is newly applied at type 3 (CRS) at CC of 2 mA, the

switching mode returns to type 1 (BRS1). The tendency for the LRS current to gradually increase is observed for the conversion to be completed, and 450 DC cycles of endurance are conducted after the stabilization (see Fig. S5, ESI<sup>†</sup>). The CC dependent switching tendency suggests that low CC (700  $\mu$ A) can limit the reset process after the set process for CRS and high CC (4 mA). The possible conduction filament evolution model for the transition from BRS to CRS can be explained by the schematics based of previous literature about metal oxide-based RRAM devices (see Fig. S6, ESI<sup>†</sup>).<sup>45–49</sup>

## Conclusion

We characterize three types of resistive switching behaviors in a Pt/HfAlO<sub>x</sub>/TiN device for neuromorphic application. Type 1 (BRS1 under negative set and positive reset) shows the best endurance and ON/OFF margin. Type 2 (BRS2 under positive set and negative reset) shows the weight update with the best linear manner and the lowest variation by identical pulses. Type 3 (CRS, the reset after the set process in the same polarity) is advantageous in the sense that it has the highest read margin in a cross-point array structure due to the nonlinear  $I$ - $V$  characteristics. Moreover, with the same polarity, the increase and the decrease of the conductance can be controlled by the magnitude of the pulse. Finally, the transitions between BRS and CRS are verified by controlling the operation polarity and the CC. Various resistive switching characteristics according to the operation switching mode in one device can be flexibly applied to various applications including neuromorphic system.

## Conflicts of interest

There are no conflicts to declare.

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## Notes and references

- 1 Y. Chen, G.-Y. Jung, D. A. A. Ohlberg, X. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart and R. S. Williams, *Nanotechnology*, 2003, **14**, 462–468.

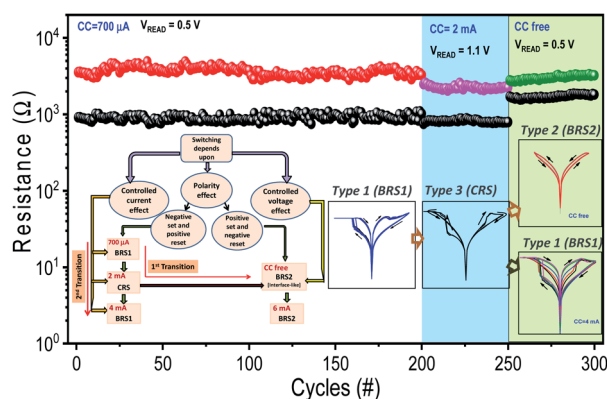


Fig. 9 Continuous endurance cycle for three switching types (BRS1 → CRS → BRS2) and flow chart and  $I$ - $V$  curves for the transition among different switching types.



- 2 M. D. Pickett and R. William, *Nanotechnology*, 2012, **23**, 215202.
- 3 B. Gao, X. Shimeng, N. Liu, B. Liu and B. Wang, *IEEE Int. Electron Devices Meet.*, 2008, 1–4.
- 4 F. Pan, S. Gao, C. Chen, C. Song and F. Zeng, *Mater. Sci. Eng., R*, 2014, **83**, 1–59.
- 5 D. Ielmini and H. S. P. Wong, *Nat. Electron.*, 2018, **1**, 333–343.
- 6 W. Bai, R. Huang, Y. Cai, Y. Tang, X. Zhang and Y. Wang, *IEEE Electron Device Lett.*, 2013, **34**, 223–225.
- 7 Y. Wang, Q. Liu, S. Long, W. Wang, Q. Wang, *et al.*, *Nanotechnology*, 2009, **21**, 045202.
- 8 S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder and W. Lu, *Nano Lett.*, 2010, **10**, 1297–1301.
- 9 T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, *et al.*, *Science*, 2009, **326**, 1516–1519.
- 10 S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, *et al.*, *IEEE Trans. Electron Devices*, 2011, **58**, 2729–2737.
- 11 Q. Wan, M. T. Sharbati, J. R. Erickson, Y. Du and F. Xiong, *Adv. Mater. Technol.*, 2019, **4**, 1900037.
- 12 V. Milo, C. Zambelli, P. Olivo, E. Pérez, M. K. Mahadevaiah, O. G. Ossorio, Ch. Wenger and D. Ielmini, *APL Mater.*, 2019, **7**, 081120.
- 13 F. Pan, S. Gao, C. Chen, C. Song and F. Zeng, *Mater. Sci. Eng., R*, 2014, **83**, 1–59.
- 14 C. D. Wright, P. Hosseini and J. A. V. Diosdado, *Adv. Funct. Mater.*, 2013, **23**, 2248–2254.
- 15 A. Wedig, M. Luebben, D. Cho, M. Moors, K. Skaja and I. Valov, *Nat. Nanotechnol.*, 2016, **11**, 67–74.
- 16 Y. X. Zhou, Y. Li, Y. T. Su, Z. R. Wang, L. Y. Shih, T. C. Chang, K. C. Chang, S. B. Long, S. M. Sze and X. S. Miao, *Nanoscale*, 2017, **9**, 6649–6657.
- 17 R. Degraeve, A. Fantini, N. Raghavan, L. Goux, S. Clima, B. Govoreanu, A. Belmonte, D. Linten and M. Jurczak, *Microelectron. Eng.*, 2015, **147**, 171–175.
- 18 S. Yu, B. Gao, H. Dai, B. Sun, L. Liu, X. Liu, R. Han, J. Kang and B. Yu, *Electrochem. Solid-State Lett.*, 2010, **13**, 36.
- 19 X. Di Huang, Y. Li, H. Y. Li, Y. F. Lu, K. H. Xue and X. S. Miao, *Appl. Phys. Lett.*, 2020, **116**, 173504.
- 20 M. Akbari, M. K. Kim, D. Kim and J. S. Lee, *RSC Adv.*, 2017, **7**, 16704–16708.
- 21 B. Gao, B. Chen, F. Zhang, L. Liu and Yu. Bin, *IEEE Trans. Electron Devices*, 2013, **60**, 1379–1383.
- 22 S. La Barbera, A. F. Vincent, D. Vuillaume, D. Querlioz and F. Alibert, *Sci. Rep.*, 2016, **6**, 1–11.
- 23 G. Wang, S. Long, Z. Yu, M. Zhang, Y. Li, D. Xu, H. Lv, Q. Liu, X. Yan, M. Wang, X. Xu, H. Liu, B. Yang and M. Liu, *Nanoscale Res. Lett.*, 2015, **10**, 1–7.
- 24 C.-Y. Lin, C.-Y. Wu, C.-Y. Wu, C. Hu and T.-Y. Tseng, *J. Electrochem. Soc.*, 2007, **154**, G189.
- 25 U. Celano, Y. Yin Chen, D. J. Wouters, G. Groeseneken, M. Jurczak and W. Vandervorst, *Appl. Phys. Lett.*, 2013, **102**, 121602.
- 26 J. K. Lee, S. Jung, J. Park, S. W. Chung, J. Sung Roh, S. J. Hong, I. Hwan Cho, H. I. Kwon, C. Hyeong Park, B. G. Park and J. H. Lee, *Appl. Phys. Lett.*, 2012, **101**, 103506.
- 27 S. G. Hu, Y. Liu, T. P. Chen, Z. Liu, Q. Yu, L. J. Deng, Y. Yin and S. Hosaka, *Appl. Phys. Lett.*, 2013, **102**, 183510.
- 28 B. Granseth, B. Odermatt, S. J. J. Royle and L. Lagnado, *Neuron*, 2006, **51**, 773–786.
- 29 R. Yang, H. Huang and X. Guo, *Adv. Electron. Mater.*, 2019, **5**, 1900287.
- 30 G. G. Turrigiano and S. B. Nelson, *Nat. Rev. Neurosci.*, 2004, **5**, 97–107.
- 31 P. P. Atluri and W. G. Regehr, *J. Neurosci.*, 1996, **16**, 5661–5671.
- 32 S. A. Baccus, *Proc. Natl. Acad. Sci. U. S. A.*, 1998, **95**, 8345–8350.
- 33 R. Guo, Y. Zhou, L. Wu, Z. Wang, Z. Lim, X. Yan, W. Lin, H. Wang, H. Y. Yoong, S. Chen, Ariando, T. Venkatesan, J. Wang, G. M. Chow, A. Gruverman, X. Miao, Y. Zhu and J. Chen, *ACS Appl. Mater. Interfaces*, 2018, **10**, 12862–12869.
- 34 Y. T. Tseng, T. M. Tsai, T. C. Chang, C. C. Shih, K. C. Chang, R. Zhang, K. H. Chen, J. H. Chen, Y. C. Li, C. Y. Lin, Y. C. Hung, Y. E. Syu, J. C. Zheng and S. M. Sze, *Appl. Phys. Lett.*, 2015, **106**, 213505.
- 35 T. Breuer, A. Siemon, E. Linn, S. Menzel and R. Vikas, *Nanotechnology*, 2015, **26**, 415202.
- 36 S. Yu, *Proc. IEEE*, 2018, **106**, 260–285.
- 37 G. Indiveri, E. Chicca and R. Douglas, *IEEE Trans. Neural Network.*, 2006, **17**, 211–221.
- 38 G.-Q. Bi and M.-M. Poo, *J. Neurosci.*, 1998, **24**, 10464–10472.
- 39 G. Khurana, N. Kumar, M. Chhowalla, J. F. Scott and R. S. Katiyar, *Sci. Rep.*, 2019, **9**, 1–10.
- 40 J. J. Huang, Y. M. Tseng, C. W. Hsu and T. H. Hou, *IEEE Electron Device Lett.*, 2011, **32**, 1427–1429.
- 41 J. Zhou, K. H. Kim and W. Lu, *IEEE Trans. Electron Devices*, 2014, **61**, 1369–1376.
- 42 J. T. Qiu, S. Samanta, M. Dutta, S. Ginnaram and S. Maikap, *Langmuir*, 2019, **35**, 3897–3906.
- 43 Y. Lu, J. H. Lee and I. W. Chen, *Nanoscale*, 2017, **9**, 12690–12697.
- 44 F. Pan, C. Chen, Z. S. Wang, Y. C. Yang, J. Yang and F. Zeng, *Prog. Nat. Sci.: Mater. Int.*, 2010, **20**, 1–15.
- 45 S. Chandrasekaran, F. M. Simanjuntak, R. Saminathan, D. Panda and T.-Y. Tseng, *Nanotechnology*, 2019, **30**, 445205.
- 46 D. Panda, A. Dhar and T.-Y. Tseng, *IEEE Trans. Nanotechnol.*, 2012, **11**, 51–55.
- 47 D. Panda and T.-Y. Tseng, *Thin Solid Films*, 2013, **531**, 1–20.
- 48 D. Panda and T.-Y. Tseng, *J. Mater. Sci.*, 2013, **48**, 6849–6877.
- 49 D. Panda, C.-Y. Huang and T.-Y. Tseng, *Appl. Phys. Lett.*, 2012, **100**, 112901.

