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Resistance state evolution under constant electric stress on a MoS₂ non-volatile resistive switching device†

Xiaohan Wu, [iD] Ruijing Ge, Yifu Huang, [iD] Deji Akinwande and Jack C. Lee

MoS₂ has been reported to exhibit a resistive switching phenomenon in a vertical metal–insulator–metal (MIM) structure and has attracted much attention due to its ultra-thin active layer thickness. Here, the resistance evolutions in the high resistance state (HRS) and low resistance state (LRS) are investigated under constant voltage stress (CVS) or constant current stress (CCS) on MoS₂ resistive switching devices. Interestingly, compared with bulk transition metal oxides (TMO), MoS₂ exhibits an opposite characteristic in the fresh or pre-RESET device in the "HRS" wherein the resistance will increase to an even higher resistance after applying CVS, a unique phenomenon only accessible in 2D-based resistive switching devices. It is inferred that instead of in the highest resistance state, the fresh or pre-RESET devices are in an intermediate state with a small amount of Au embedded in the MoS₂ film. Inspired by the capability of both bipolar and unipolar operation, positive and negative CVS measurements are performed and show similar characteristics. In addition, it is observed that the resistance state transition is faster when using higher electric stress. Numerical simulations have been performed to study the temperature effect with small-area integration capability. These results can be explained by a modified conductive-bridge-like model based on Au migration, uncovering the switching mechanisms in the ultrathin 2D materials and inspiring future studies in this area.

1 Introduction

In the last few years, various two-dimensional (2D) materials have been reported to exhibit non-volatile resistive switching (NVRS) behavior including functionalized graphene oxide, degraded black phosphorus, double-layer MoS₂, single- or multi-layer hexagonal boron nitride (h-BN), *etc.*[1–6] These devices, in the simple structure of metal–insulator–metal (MIM), are based on the resistive switching effect in the active layer, where the resistance can be repeatably switched between a high resistance state (HRS) and a low resistance state (LRS) and sustained without any power supply.[7–11] Compared with the transition metal oxide (TMO)-based resistive random access memory (RRAM), the 2D-based NVRS devices have drawn much attention due to the atomically thin active layer thickness, the complex switching mechanisms involving interaction of defects and ions at the sharp interfaces, and the potential applications in flexible memory fabrics and neuromorphic computing.[12–15] In 2018, the "atomristors" based on monolayer or few-layer transition metal dichalcogenides (TMDs), was first demonstrated in vertical MIM configuration and show stable NVRS behavior with

high ON/OFF ratio, fast switching speed and forming-free characteristics.[16–19]

Constant electric stress has been used in RRAM devices with bulk metal oxides as active layers to study transition time, reliability and switching mechanisms.[20–24] In this article, we performed constant voltage stress (CVS) and constant current stress (CCS) on MoS₂-based NVRS devices. It has been found that for fresh devices or working devices that RESET to HRS, the resistance would increase to an even higher resistance state by applying CVS at low voltages, instead of decreasing to LRS in conventional metal-oxide memory devices. To the best of our knowledge, this unique phenomenon has only been reported for the 2D-based NVRS devices, indicating a distinct switching mechanism due to the ultrathin active layer thickness. While with CVS at higher voltage (>SET voltage), the devices will be switched to LRS. This observation implies that the initial state or the "HRS" obtained by voltage sweeping is not the highest resistance state, but an intermediate state. Both positive and negative CVS were applied on the pre-RESET devices, showing similar resistance increasing behavior, which is consistent with the co-existence of bipolar and unipolar modes in MoS₂ atomristors. On the other hand, by using CCS on the devices at HRS, the resistance will be switched to a LRS. The different behaviors under current and voltage stress suggest that SET process is triggered by electric field, while RESET process is dominated by Joule heating. In addition, we performed CVS and CCS on

Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758, USA. E-mail: leejc@austin.utexas.edu; deji@ece.utexas.edu

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working devices at LRS to switch them to HRS. It is also observed that with higher electric stress, the resistance state transition time will be shorter. To study the Joule heating effect during RESET process, we have performed numerical simulations and demonstrated significant temperature reduction using diamond substrate, enabling small-area device integration. The electric stress test results provide evidence for the switching mechanisms in MoS_2 atomristors which can be explained by a modified conductive-bridge-like model with Au ion migration to interpret the conductive path evolution.

2   Device fabrication and characterization

The CVD-grown continuous 3–5 layers MoS_2 films on SiO_2/Si substrate were purchased from SixCarbon Technology. Bottom electrodes (BE) were patterned by electron beam lithography and deposited with a 2 nm Cr/100 nm Au metal stack by electron beam evaporation on a commercial diamond substrate. The MoS_2 layer was transferred onto the target substrate with BE using a polydimethylsiloxane (PDMS) stamp transfer method.[16] The PDMS stamp was adhered to the MoS_2 film and then the sample was soaked into diluted water. The MoS_2–PDMS film was separated from the hydrophilic SiO_2/Si substrate and brought into contact with the target diamond substrate. The

PDMS was subsequently peeled off, leaving the continuous MoS_2 film ($\sim 2 \times 2$ mm^2) on the target substrate with BE on it. The crossbar devices were finished by the patterning and deposition of top electrodes (TE) using the same method as BE. Au was used as both BE and TE to avoid metal oxide formation. The fabricated devices were measured on a Cascade probe station with an Agilent 4156 semiconductor analyzer under ambient conditions. Raman spectroscopy was performed to evaluate the MoS_2 film by a Renishaw inVia system using a 532 nm wavelength source.

3   Results and discussions

The schematic and optical image of fabricated crossbar device are shown in Fig. 1a and b respectively. The vertical MIM device structure consists of a 3–5 layers MoS_2 film and two gold electrodes. The device area (typically 0.5×0.5 μm^2 in this paper) is defined as the overlapped region between TE and BE. Compared with SiO_2/Si substrate with a low thermal conductivity for SiO_2 (1.4 W m^{-1} K^{-1}), diamond substrate is used in the MoS_2-based memory devices with a high thermal conductivity of ~ 1000 W m^{-1} K^{-1} that can dissipate the excessive heat through the substrate more effectively. This prevents the narrow metal electrode lines from Joule heating and thus enables the fabrication of small-area crossbar devices. Raman spectroscopy was
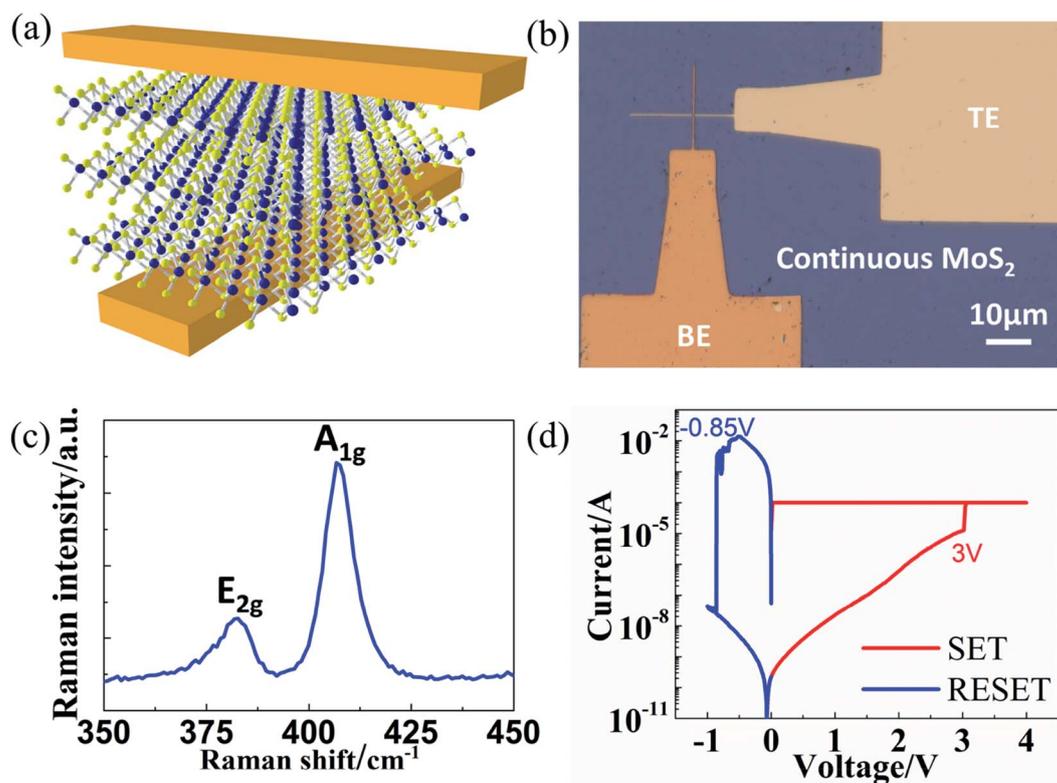

Fig. 1   Device characterization and basic switching curve. (a) The schematic of crossbar device with few-layer MoS_2 as the active layer. (b) The optical image of fabricated crossbar device with continuous MoS_2 layer sandwiched between Au electrodes on diamond substrate. The area of this device is 0.5×0.5 μm^2. (c) Raman spectrum of CVD-grown 3–5 layers MoS_2 film. (d) A representative I–V curve of MoS_2 resistive switching device. The SET and RESET voltage are 3 V and −0.85 V respectively.

performed and displayed in Fig. 1c, showing high quality of the crystalline 2D layered material.[25]

Fig. 1d shows a representative bipolar I–V switching curve of a crossbar MoS_2 NVRS device. At first, the as-fabricated devices are generally at HRS. By applying a positive voltage bias, the current suddenly increases to the compliance, indicating a transition from HRS to LRS ("SET" process). The reverse transition ("RESET" process) is realized by applying a negative voltage sweep (bipolar mode) or a positive voltage sweep (unipolar mode), which are both accessible for MoS_2 NVRS devices.[16] The critical voltages that trigger the resistive switching behavior are called SET and RESET voltage. Note that a high RESET current is commonly observed in both traditional bulk oxide-based and emerging 2D-based NVRS devices, which produces Joule heating in the switching layer that is responsible for the RESET process.[2,7,26–28] In addition to voltage sweeping, other operation methods like current sweeping, pulse operation and constant electric stress including CVS and CCS as discussed below, can be used to study the switching characteristics and investigate the underlying mechanisms.

Fig. 2 shows the resistance evolution under CVS measured on the devices at HRS. The working devices that exhibit stable
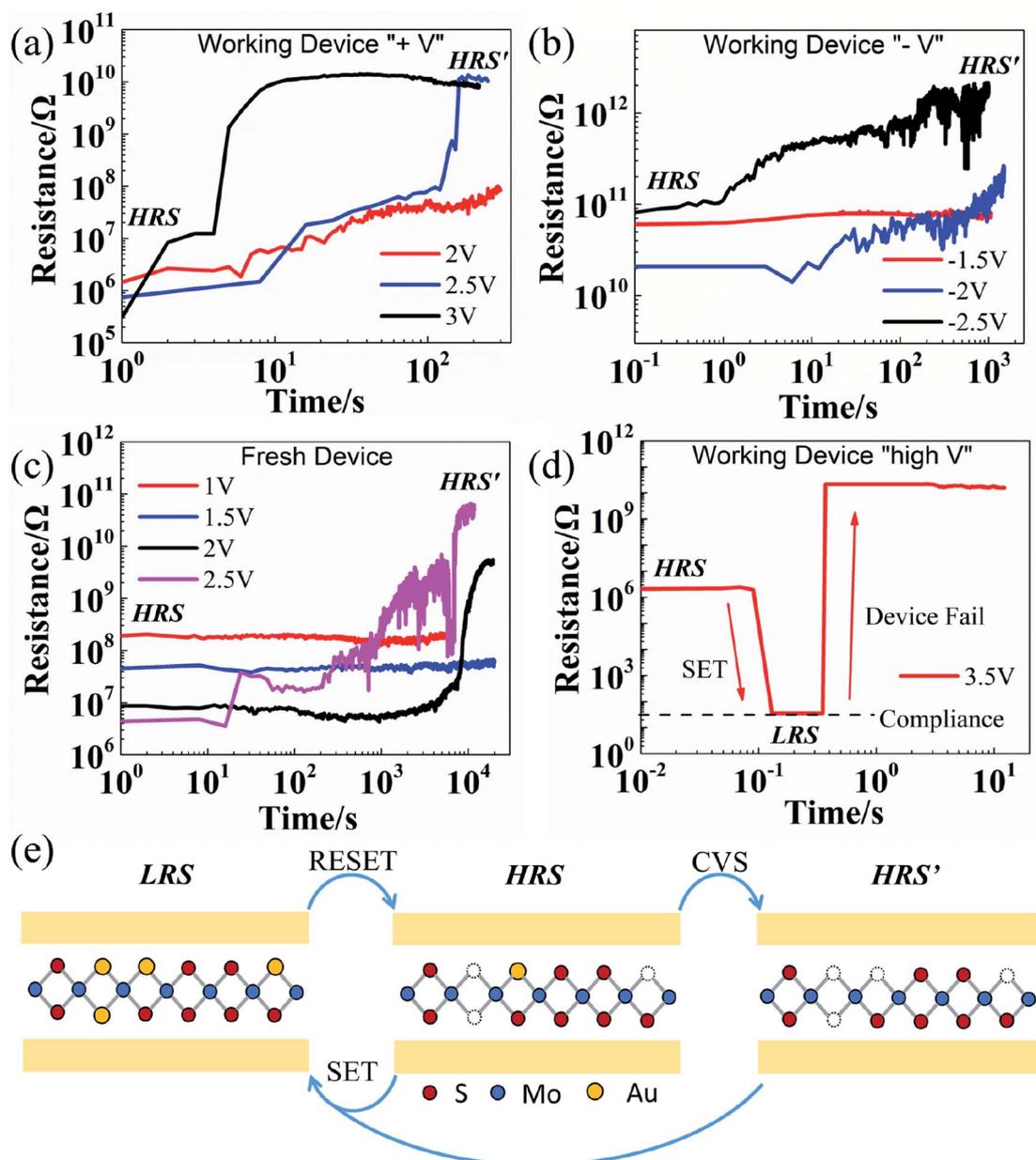

Fig. 2 Resistance evolution under CVS for devices at HRS. The resistance of working devices at HRS (pre-RESET devices) measured during (a) positive voltage stress and (b) negative voltage stress. (c) The resistance of fresh (as-fabricated) devices at HRS measured during CVS. The resistance states change from HRS to a higher resistance state (labelled as HRS') for the cases of (a)–(c). (d) The resistance of working devices at HRS measured during a high voltage stress (>V_{SET}). The resistance state changes from HRS to LRS and then fails due to high power. (e) Illustration of the resistance states for MoS_2 NVRS devices by voltage-sweep SET/RESET and low-voltage CVS.
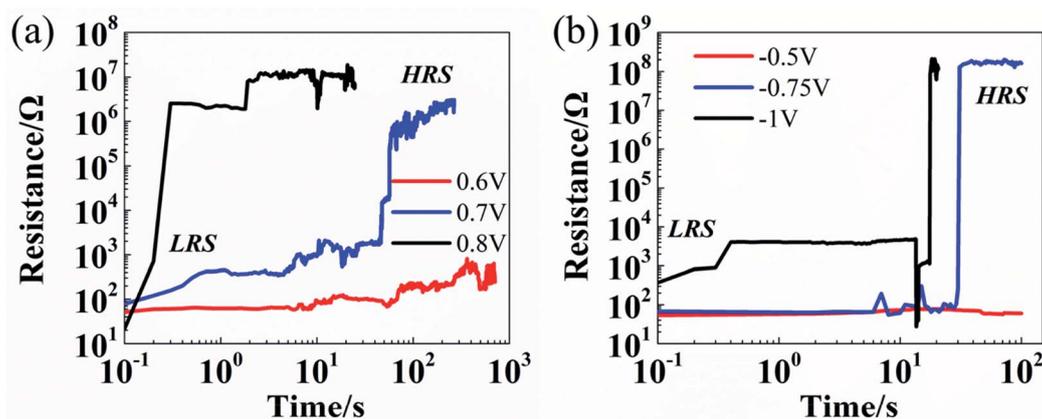
Fig. 3 Resistance evolution under CVS for devices at LRS. The resistance of working devices at LRS (pre-SET devices) measured during (a) positive voltage stress and (b) negative voltage stress. The resistance states change from LRS to HRS for the cases of (a) and (b).

switching characteristics are tested for several DC cycles and RESET to HRS before stress measurement. Subsequently, relatively low constant voltage bias ($<V_{SET}$) is applied on the devices as shown in Fig. 2a with positive CVS and Fig. 2b with negative CVS. It is observed that the resistance changes from HRS to an even higher resistance state (labelled as HRS′). This is opposite to the observation in the devices using bulk metal oxides as active layer, where the resistance is switched from HRS to LRS under CVS.[22,24] The READ I–V curves before and after CVS in Fig. S1† clearly show the transition from HRS to HRS′ and demonstrate that this resistance state transition can be sustained without external stress. Similar behavior is observed with both positive and negative CVS, which can be associated with the co-existence of unipolar and bipolar modes in MoS_2 NVRS devices. In addition, CVS test is performed on the fresh (as-fabricated) devices, showing similar HRS to HRS′ transition (see Fig. 2c). This phenomenon indicates that for both fresh devices and pre-RESET working devices, the commonly called "HRS" is not the highest resistance, but an intermediate state that can still be switched to a higher resistance state (HRS′). On the other hand, if the voltage stress is higher than the SET voltage (see Fig. 2d), the device will switch to LRS and then fail due to high power.

A previously proposed conductive-bridge-like model with the assistance of metal atom/ion migration is used to explain the NVRS phenomenon in MoS_2 atomristors.[4,17] The CVS test results provide more insights to the model with the resistance states illustrated in Fig. 2e. In MoS_2 film, sulfur vacancies commonly exist and play an important role in resistive switching.[29,30] The SET process is driven by the migration of Au ions into the sulfur vacancies, which changes the MoS_2 film from semiconducting to metallic at the localized defect-rich regions. This atomic-level conductive-bridge-like model is supported by our recent finding that the Au atoms moving in and out from the vacancy site was directly observed by scanning tunnelling microscopy (STM), which results in NVRS behavior tested by electrical measurements using STM tip as the top electrode.[31] The existence of HRS′ indicates that, a small amount of metal atoms may be embedded in the MoS_2 film at HRS, which are possibly induced

by deposition process for fresh devices or incomplete voltage-sweep RESET for working devices. Experimental evidence in supporting this proposed mechanism can be found in previous reports which suggest that metal atoms could diffuse into the defects in 2D TMD films during the evaporation deposition process of top electrodes as shown in cross-sectional TEM images.[32,33] These embedded metal atoms/ions are negligible in bulk metal oxides, but are important in the atomically thin MoS_2 sheets.[7,34,35] With a relatively low voltage stress, these metal atoms tend to move out of the vacancies due to the accumulated Joule heating effect, resulting in a transition to the higher resistance state (HRS′). By applying a high voltage stress ($>V_{SET}$), the sulfur vacancies would be substituted by more metal ions from the electrodes. This is similar to the SET process supported by ab initio simulation and STM measurements that one or multiple conductive links are formed.[4,17,31] It is worth noting that the devices at HRS′ after CVS can still SET to LRS by voltage sweeping (see Fig. S2 in ESI†). It can be inferred from the CVS analysis that the SET process is dominated by electric field (voltage) since a voltage bias beyond the critical voltage is needed to trigger the resistance switching effect. The unique resistance evolution phenomenon under CVS treatment suggests a distinct property for 2D materials. For traditional bulk materials, the resistance state is typically determined by the characteristics of the conductive filament and the "gap" region between the electrode and filament tip.[7,28] While for 2D materials, the resistance state can be modulated by the inter-action between atoms/ions from electrodes and interfacial vacancies, which in turn enabling atomic-level resistance control with advanced defect engineering for crystalline 2D materials.

The resistance evolution under CVS measured on the devices at LRS is shown in Fig. 3. It is observed that the resistance states can be switched from LRS to HRS with either positive bias (Fig. 3a) or negative bias (Fig. 3b). The READ I–V curves before and after CVS are included in Fig. S3.† As shown in Fig. 3b as an example, with relatively low stress at −0.5 V, the device tends to remain at LRS. However, by applying higher voltage stress (at −0.75 V and −1 V), the device can be switched to HRS in a short
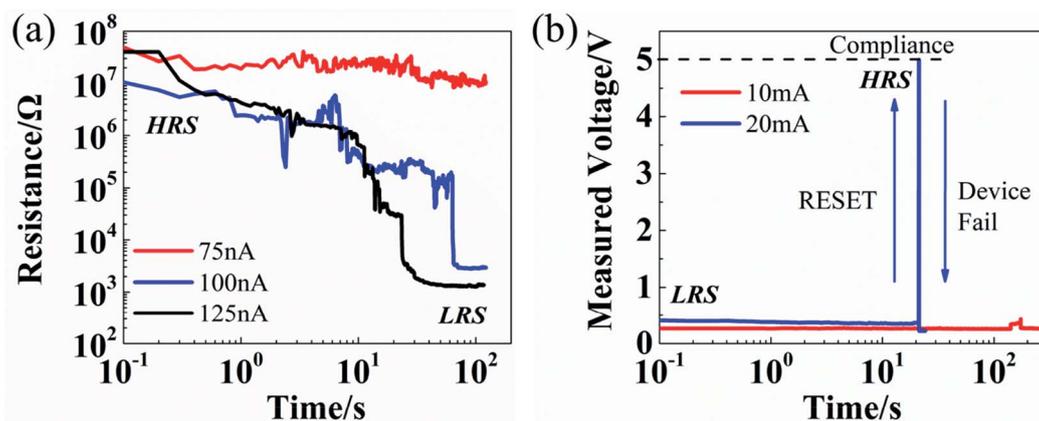
Fig. 4 Resistance evolution under CCS for devices at HRS and LRS. (a) The resistance of devices at HRS measured during CCS. The resistance states change from HRS to LRS. (b) The voltage of devices at LRS measured during CCS. Resistance state changes from LRS to HRS with 20 mA CCS and then fails due to high power.

time. This RESET-like behavior can be explained by the Joule heating induced by the high current (typically ∼10 mA) that dissolves the conductive path into metal ions, which then migrate back to the electrodes by reduction. Our previous experimental observation of co-existence of both bipolar and unipolar switching in MoS$_2$-based devices provides additional evidence supporting this theory.[7,28]

CCS tests are performed on MoS$_2$ NVRS devices and exhibit similar characteristics compared with traditional metal oxide-based devices.[21–23] In Fig. 4a, CCS is applied on the devices at HRS, resulting in a resistance decrease from HRS to LRS, which can be attributed to the additional defects introduced into the MoS$_2$ thin film under the low current stress. With relatively low current stress at 75 nA, the device stays at the initial HRS. While
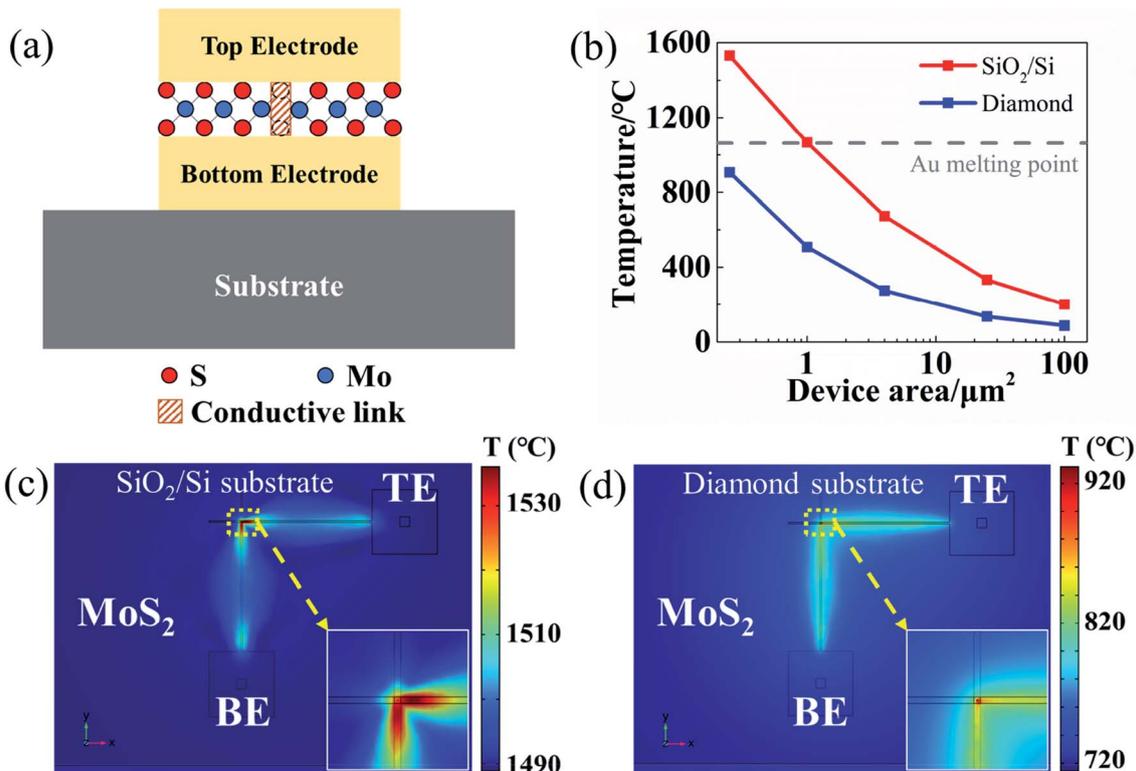

Fig. 5 Numerical simulation results of temperature distribution. (a) Schematic of cross-sectional MIM structure of MoS$_2$ NVRS device at LRS on SiO$_2$/Si or diamond substrate. (b) Calculated peak temperature with different device areas on SiO$_2$/Si and diamond substrate. The temperature distribution of MoS$_2$ crossbar device on (c) SiO$_2$/Si and (d) diamond substrate. The temperature induced by Joule heating effect reduces significantly for device on diamond substrate due to its high thermal conductivity.

with higher stress (100 nA and 125 nA), the HRS-to-LRS transition can be observed shortly. Note that the current density here (up to 5×10^5 A m^{-2}) through the device is within the common range for NVRS devices at HRS.[2,26,27,36,37] The READ I–V curves before and after CCS can be seen in Fig. S4,† showing the resistance transition from HRS to LRS can be maintained without external stress. For the devices at LRS (Fig. 4b), a transition from LRS to HRS happens under high CCS and then the device fails due to the high power. It is also observed that, the LRS-to-HRS transition, as shown in Fig. 3a, b and 4b, is a fast process with sudden resistance increase, which is similar to the sharp RESET behavior in voltage sweeping that caused by the conductive path rupture due to Joule heating. For all the electric stress tests, different stress amplitudes have been used, showing a common trend that higher electric stress results in shorter transition time.

To further study the Joule heating effect, numerical simulation has been performed to calculate the temperature distribution on MoS$_2$-based devices during the RESET process. The electrical current and heat transfer in solids modules in COMSOL Multiphysics® are utilized to compute the Joule heat induced by electric current. In this model, a vertical metal–insulator–metal (MIM) structure is established on a SiO$_2$/Si or diamond substrate (Fig. 5a). Crossbar device configuration is used with Au as TE/BE and continuous MoS$_2$ film as the active layer. At LRS, a metallic cylinder with a radius of 50 nm is modelled as the conductive link. A voltage sweeping (0–2 V) is applied on TE while BE and substrate are grounded. Fig. 5b shows the peak temperature with different device area (from 0.5 $\times$ 0.5 μm^2 to from 10 $\times$ 10 μm^2). As the device area shrinks, the peak temperature increases. This is to be expected as the resistance of the metal line increases. This trend is consistent with the experimental observation that for devices below 1×1 μm^2 on SiO$_2$/Si substrate, the metal lines could actually be burned (or blown out) due to the high temperature induced by Joule heating effect. While by using diamond substrate with a high thermal conductivity, the peak temperature of a 0.5 $\times$ 0.5 μm^2 device can be significantly reduced from 1558 °C on SiO$_2$/Si substrate to 906 °C on diamond substrate, below Au melting point at 1064 °C. The calculated temperature distribution in Fig. 5c shows that the peak temperature region spreads to metal lines for the device on SiO$_2$/Si substrate, resulting in the line burning phenomenon. As shown in Fig. 5d, benefiting from the high thermal conductivity of diamond substrate, the peak temperature region is confined within the device area. These simulations results, correlated with experimental data, demonstrate a significant temperature reduction during RESET process by using a diamond substrate, which prevents metal lines from burning and enables small-area device integration. Our simulation and experimental results provide additional insights into the failure analysis and mechanism studies due to Joule heating effect.

4 Conclusion

In summary, we performed CVS and CCS tests on MoS$_2$-based 2D memory devices. The resistance evolution results disclose an additional resistance state which can be achieved by low CVS treatment on the devices at HRS. A modified conductive-bridge-like model based on metal atom/ion migration is proposed to explain the stress effects. Our results provide additional insights into resistance states transition, device reliability and applications of 2D atomristors.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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