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Interfacial synthesis of a large-area coordination polymer membrane for rewritable nonvolatile memory devices†

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The facile synthesis of large-area coordination polymer membranes with controlled nanoscale thicknesses is critical towards their applications in information storage electronics. Here, we have reported a facile and substrate-independent interfacial synthesis method for preparing a large-area two-dimensional (2D) coordination polymer membrane at the air–liquid interface. The prepared high-quality 2D membrane could be transferred onto an indium tin oxide (ITO) substrate to construct a nonvolatile memory device, which showed reversible switching with a high ON/OFF current ratio of 10^3, good stability and a long retention time. Our discovery of resistive switching with nonvolatile bistability based on the substrate-independent growth of the 2D coordination polymer membrane holds significant promise for the development of solution-processable nonvolatile memory devices with a miniaturized device size.

The exponential growth of communication for information and the miniaturization of electronic devices have caused an urgent demand for the design and preparation of new memory materials and devices.[1–4] Organic/polymer memory devices have attracted considerable attention as promising alternatives to the conventional inorganic semiconductor-based memory devices.[5] They have distinguished themselves as potential candidates for flexible and high-density data storage due to their low cost, structural tenability, mechanical strength, flexibility, and ease of processing.[6–16] Nonetheless, the intrinsically weak intermolecular interactions between organic molecules result in low thermal stability and poor long-term environmental stability, which hinder their potential applications.[17–19]

As an important class of organic materials, coordination polymers demonstrate attractive switching properties and exhibit promising applications in the data storage field.[20–22] Compared with polymers that have pure organic skeletons, coordination polymers comprising metal and organic ligands offer a potential alternative due to their facile preparation and high thermal stability, combining the advantages of both polymers and metal complexes. Particularly, by the flexible design of metal and organic constituents as well as by modifying the functional groups in the coordination complexes, the properties of memory devices based on the resultant

coordination polymers can be fine-tuned.[15] For instance, ternary resistive random access memory devices have been fabricated from one-dimensional conjugated coordination polymer chains coordinated with Co ions,[23] which exhibit excellent thermal and long-term stability benefiting from their strong intermolecular interactions. Moreover, the successful growth of high-quality metal–organic framework (MOF) membranes on flexible gold-coated polyethylene terephthalate (PET) substrates has been achieved by liquid phase epitaxy for practical wearable information storage applications; moreover, a uniform and reproducible resistive switching effect has been observed.[24]

Besides molecular design, the formation of the thin films of active materials is crucial for the memory performance and coordination polymers downsized to nanoscale membranes with controllable electrical conductivity are promising for high-density data storage with a miniaturized device size. To date, vacuum-deposited, spin-coated or inkjet-printed films of the as-synthesized memory materials have been reported for memory applications.[25] Unfortunately, severe problems such as easy cracking, unsatisfactory uniformity and thickness uncontrollability usually accompany the above-mentioned elaborate membrane deposition approaches, seriously limiting the memory performance. To address these issues, the growth and preparation of high-quality memory material membranes through facile chemical synthesis has been an urgent demand. Currently, liquid phase epitaxy or a layer-by-layer (LbL) approach is commonly used to grow high-quality coordination polymer membranes on organically functionalized surfaces for memory devices.[26] Memory devices based on LbL approach-processed coordination polymer membranes have been

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reported to show excellent switching performance with a high ON/OFF current ratio and multilevel storage. Though the LbL approach offers unique opportunities, the substrate-dependent characteristics of the LbL thin-film preparation scheme seriously limit the applications of coordination polymers in memory devices. Despite the above-mentioned advances, coordination polymer membranes with an appropriate molecular design concomitant with a good film preparation approach are still urgently needed to obtain high-performance memory devices.

In this work, we have presented a facile and substrate-independent interfacial synthesis method for the preparation of a continuous and large-area coordination polymer membrane with nanoscale thickness at the air–liquid interface. The high-quality two-dimensional (2D) membrane can be transferred onto an indium tin oxide (ITO) substrate as the active layer to construct a nonvolatile memory device. The sandwiched device shows excellent rewritable nonvolatile memory performance with a low operational voltage, a large ON/OFF ratio, good stability and a long retention time.

Through a mild coordination reaction between a cobalt salt and the ligand 1,2,4,5-benzenetetramine tetrahydrochloride, a large-scale d–π conjugated coordination polymer membrane at the air–liquid interface can be prepared (Fig. 1). The resulting brown membrane demonstrates great substrate independence and can be transferred on to any substrate by dipping the support in the reaction solution and then lifting the membrane, making it practically applicable in diverse fields. The scanning electron microscopy (SEM) characterizations of the as-prepared membrane transferred onto the SiO$_2$/Si substrate indicated a large-scale and continuous distribution of the membrane with a uniform thickness of ~300 nm.

The structure of the as-prepared brown membrane was characterized by powder X-ray diffraction (PXRD) utilizing two individual scattering geometries, namely, out-of-plane scattering geometry and in-plane geometry. The PXRD profile
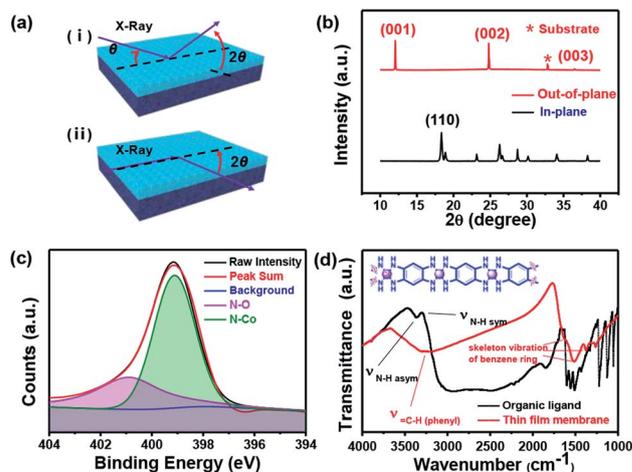
Fig. 2 (a) The orientation of the films for (i) out-of-plane XRD scan and (ii) in-plane XRD scan. (b) PXRD profiles of out-of-plane XRD and in-plane XRD of the polymer membrane. (c) N 1s core level spectra of the membrane. (d) FT-IR spectra of the membrane and the ligand; the inset is the structure of the polymer membrane.

obtained using grazing-incidence XRD is presented in Fig. 2a. Different diffraction patterns were observed under these two XRD scattering geometries, suggesting an orientation-dependent characteristic of the prepared membrane (Fig. 2b).[27] X-ray photoelectron spectroscopy (XPS) of the as-prepared membrane was conducted (Fig. 2c and S1†). The strong peak at 399.1 eV suggests a strong coordination between Co(II) and the ligand. The quantification of the elements present in the coordination polymer membrane based on XPS analysis demonstrated a 3.53 : 1 atomic ratio of N : Co (Table S1†), which was close to the theoretical stoichiometric ratio (4 : 1) for the membrane structure, as shown in the inset of Fig. 2d; this further confirmed the strong coordination between one Co cation and two benzenetetramine groups of the organic ligand.[28] In addition, the characteristic N–H stretching mode of –NH$_2$ disappeared in the IR spectra after the reaction,[29] whereas the phenyl-related vibration remained, further indicating that the coordination reaction occurred (Fig. 2d). On the basis of facile preparation, substrate independence, highly oriented structure and d–π conjugation construction facilitating carrier transportation, the synthesized 2D coordination polymer membranes are expected to possess potential applications in electronic devices.

With the use of the synthesized coordination polymer membrane as the active material layer, a typical memory device with the Al/polymer membrane/ITO sandwich structure was fabricated by directly transferring the as-prepared membrane with a thickness of 300 nm from the air–liquid interface onto the ITO substrate, followed by the thermal evaporation of the top Al electrodes (inset of Fig. 3a). The as-fabricated device exhibited progressively increasing injection currents as the initial voltage was swept from 0 to −5 V (ITO as the reference level, Sweep 1), and a sharp increase from 10^{-5} A to 10^{-2} A was observed at a switching threshold voltage of −1 V (Fig. 3c), indicating the device transition from a high-resistance state
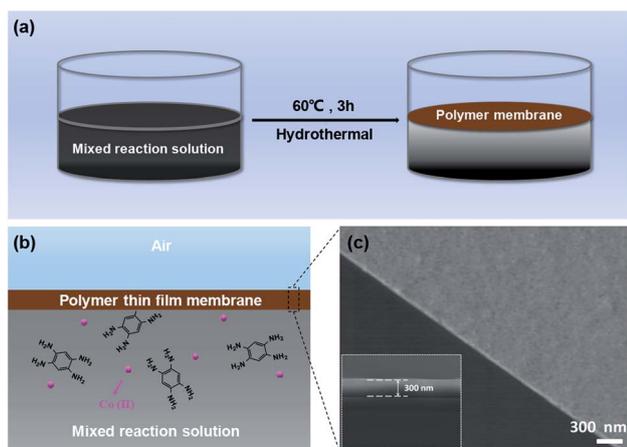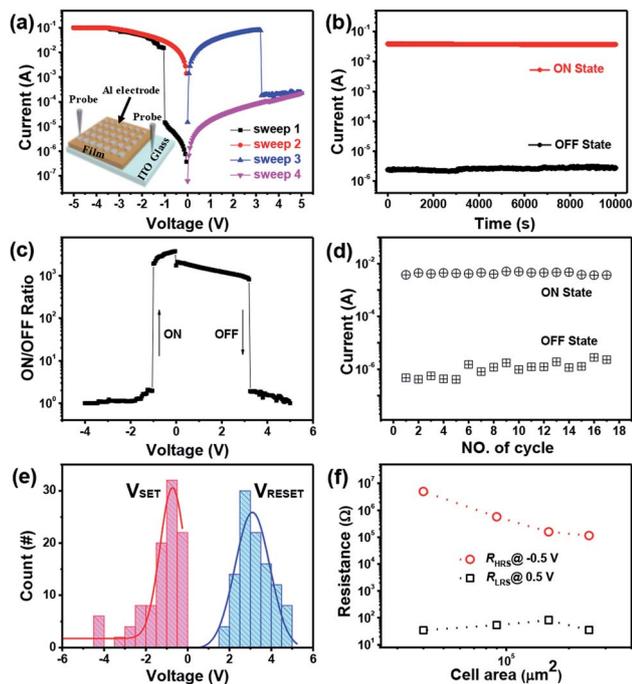

Fig. 1 (a) Illustration of the polymer membrane formation process at the interface. (b) Schematic of the polymer membrane at the air–liquid interface. (c) SEM images of the as-prepared membrane with a thickness of 300 nm.

Fig. 3 (a) *I–V* curves of the Al/polymer membrane/ITO memory device. Inset: schematic of the device structure. (b) Retention ability test of the device at a reading voltage of −0.5 V in the HRS and LRS states. (c) The ON/OFF ratio of the device under different applied voltages. (d) Currents of the device in the ON and OFF states. (e) Statistic histograms of SET/RESET voltages. (f) The cell area dependence of resistances in HRS and LRS.

(OFF state) to a low-resistance state (ON state). This electrical transition from OFF to ON states represents the "writing" process of the memory device. Significantly, the abrupt increase in the current level with a high current ratio of 10^3 contributed to a minimal misreading error for the memory device and a small switching threshold voltage of −1 V was desirable for low-power memory applications. The device maintained the ON state with high stability in the subsequent voltage sweep (Sweep 2). When the voltage was swept from 0 to 5 V (Sweep 3), an abrupt decrease in the current was observed at the threshold voltage of about 3 V and the transition from the ON state to OFF state was equivalent to the "erasing" process. Furthermore, the device maintained the OFF state with high stability in the subsequent voltage sweep (Sweep 4). The current–voltage curve sweeps revealed an integrated write-read-erase-read switching process of this memory cell, suggesting a typical nonvolatile bistable FLASH-type memory device.

Moreover, the long-term stability of the coordination polymer memory device was evaluated from the retention time tests in both the ON and OFF states (Fig. 3b). Under a constant voltage stress of 0.5 V, the OFF state current remained stable but with some slight variations. When a bias of −0.5 V was applied, the device exhibited a stable current of about 0.04 A (ON state) for up to 10 000 s and no significant decrease was observed. A high ON/OFF current ratio of 10^3 was maintained and the precise control of both ON and OFF states promised a quite low

misreading rate of the memory device. To evaluate the reliability of memory devices, their cycling endurance was investigated. Fig. 3d shows that the OFF state currents remain between 4×10^{-7} and 3×10^{-6} A and the ON state currents range from 3×10^{-3} to 6×10^{-3} A. According to the statistical current distribution (measured at −0.5 V), no significant difference was observed in the ON/OFF state currents, indicating the good stability of the device. Compared with the endurance of previously reported devices,[30,31] the endurance of our memory device is relatively short, which can be attributed to the fact that the top aluminum electrode is easily oxidized in an ambient environment without effective device packaging. It is expected that the device stability can be further improved if effective packaging is carried out or measurements are obtained in a vacuum system.

The uniformity in the distribution of switching voltages was evaluated by measuring 100 randomly selected device cells. Fig. 3e shows that the V_{SET} values of most device cells are distributed in the range from 0 to −2 V and more than 50% devices exhibit a switching threshold voltage from 0 to −1 V. The average values of V_{SET} and V_{RESET} were −0.89 V and 3.09 V (the standard deviations were 0.26 (V_{SET}) and 0.41(V_{RESET})), respectively, which coincided well with the measured results of the as-fabricated FLASH memory device. Notably, the difference between V_{SET} and V_{RESET} was large enough to ensure a low misreading rate and promise reliability when a readout was made.

Moreover, the dependence of the device resistance on the cell area was systematically studied based on a series of controlling tests to explore the underlying switching mechanism in the as-fabricated memory cell (Fig. 3f). When the applied voltage was in the range from 1 to −0.5 V, the memory cell was in a high resistance state (HRS) and the resistance (RHRS) was inversely proportional to the cell area due to the homogeneous current flowing through the memory cell.[32] In contrast, for the low-resistance state (LRS) from 0 to 0.5 V, RLRS was independent of the cell area, suggesting that the LRS was dominated by the localized conducting path.

To investigate the resistance mechanism of the 2D coordination polymer membrane-based memory device, log *I*–log *V* plots were studied to analyze the carrier transport mechanism of the OFF and ON states (Fig. 4a and b). The fitting results reveal that the *I–V* curve of the flash memory device in the OFF state consists of two distinct linear regions, corresponding to the ohmic conduction mechanism and trap-limited space charge limited conduction (TL-SCLC) mechanism,[33–39] whereas the device in the ON state only obeys the ohmic conduction mechanism. The corresponding resistive switching phenomenon was further studied by exploring the transportation mechanism of charge carriers *via* physical models (Fig. 4c–f). When a bias voltage was applied to the Al electrode and the scanning voltage was low, the density of the injected charge carriers was lower than that of the free carriers generated by thermal excitation in the film, which contributed to most of the charge transportation. The corresponding *I–V* curve shows linear behavior governed by ohmic conduction, resulting in a high resistance state (Fig. 4c). With the increase in the applied bias voltage, space charges appeared and
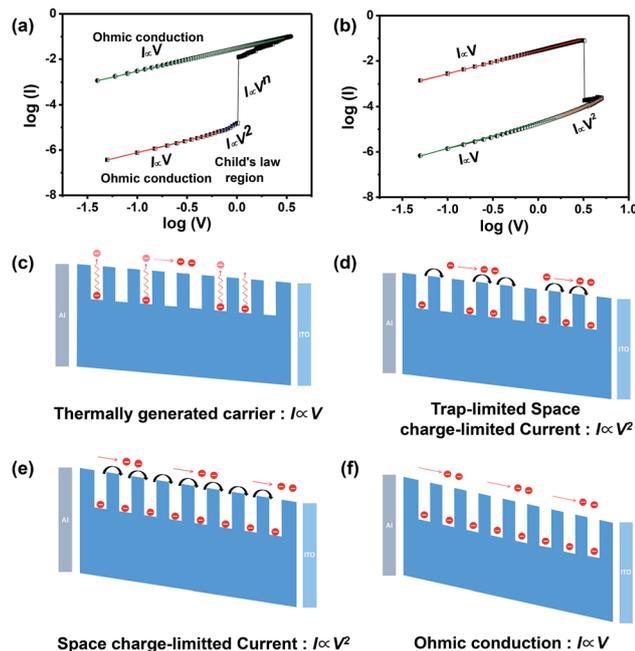
Fig. 4 (a) Fitted $I–V$ curves of the memory device at the SET process. (b) Fitted $I–V$ curves of the memory device at the RESET process. (c–f) Transportation mechanisms of charge carriers from low conductive state to intermediate conductive state and further to high conductive state.

some traps in the dielectric layer were occupied by the injected free carriers, leading to SCLC with limited trap filling dominating the carrier transport process, and the charge transport mechanism was dominated by TL-SCLC (Fig. 4d). With increasing carriers injected, the carrier transport changed from a trap-limited stage to a trap-free stage. When all the traps were filled, the injected carriers could move freely in the dielectric layer, which corresponded to trap-free SCLC conduction, indicating that the device underwent a transition from HRS to LRS. When the device changed to a low resistance state, the charge transfer still followed the ohmic conduction mechanism (Fig. 4f). The RESET process where the device changed from LRS to HRS (Fig. 4b) showed an $I \propto V$ relationship in the low resistance state, indicating that ohmic conduction dominated the charge transport process. As the device transfer to HRS, the trap center releases charges from a fully filled state to an unfilled state which shows a $I \propto V^2$ relationship. Then the state is continuously dominated by ohmic conduction. The device exhibited typical non-volatile flash characteristics, affording new ways to achieve 2D coordination polymer membrane-based memory devices *via* interfacial nanostructure engineering.

Conclusions

In summary, we have successfully prepared a large-area and continuous 2D coordination polymer membrane by a facile interfacial synthesis method. Importantly, the as-prepared high-quality 2D membrane can be transferred onto any substrate, demonstrating great substrate independence.

Moreover, a sandwich-structured memory device was fabricated with the prepared polymer membrane as the active material; the device exhibited excellent rewritable nonvolatile memory performance with a low operational voltage, high ON/OFF ratio and good stability, making coordination polymer membranes promising candidates for the development of solution-processable nonvolatile memory devices with a miniaturized device size.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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