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## Device performance limits and negative capacitance of monolayer GeSe and GeTe tunneling field effect transistors†

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Exploring the device performance limits is meaningful for guiding practical device fabrication. We propose archetype tunneling field effect transistors (TFETs) with negative capacitance (NC) and use the rigorous *ab initio* quantum transport simulation to explore the device performance limits of the TFETs based on monolayer (ML) GeSe and GeTe along with their NC counterparts. With the ferroelectric dielectric acting as a negative capacitance material, the device performances of both the ML GeSe and GeTe NCTFETs outperform their TFET counterparts, particularly for the on-state current ( $I_{on}$ ).  $I_{on}$  of the optimal ML GeSe and GeTe TFETs fulfills the demands of the International Technology Roadmap for Semiconductors (ITRS 2015 version) for low power (LP) and high performance (HP) devices, at the "6/5" node range, while with the aid of 80 nm and 50 nm thickness of ferroelectric  $\text{SrBi}_2\text{Nb}_2\text{O}_9$ , both their NC counterparts extend the fulfillments at the "4/3" node range.

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### Introduction

The successful fabrication of sub-10 nm conventional field effect transistors (FETs) based on 2D  $\text{MoS}_2$ , Si nanowires<sup>1</sup> and carbon nanotubes<sup>2</sup> encourages continuing research including but not limited to conventional FETs with new materials; figuring out the ideal device performance limits is a vital guide for the real device fabrication. Relative to the conventional FET, tunneling FET (TFET) and negative capacitance FET (NCFET) offer two new mechanisms to create a deeper subthreshold slope (SS) than the Boltzmann limit of  $60 \text{ mV dec}^{-1}$ . The lowest reported SS is only  $3.9 \text{ mV dec}^{-1}$  in the vertical Ge– $\text{MoS}_2$  TFET at room temperature,<sup>3</sup> and the minimum SS is reported for the  $\text{MoS}_2$  NCFET with ferroelectric hafnium zirconium oxide (HZO) with the value of  $6.07 \text{ mV dec}^{-1}$ .<sup>4</sup> The combination of the two mechanisms, *i.e.*, NCTFET would give a better device performance than TFET or NCFET. Lee *et al.*<sup>5</sup> found that the gate capacitance of Ge/Si NCTFET is 6–9% higher than that of its TFET counterpart. Liu *et al.*<sup>6</sup> found that double-gate Si TFET having an ultrathin body with a negative capacitance can avoid

hysteresis and reduce the SS. To some extent, the device performance of NCTFET would represent the performance limit of a new-mechanism device.

ML GeSe and GeTe are emerging semiconductors with puckered honeycomb networks such as black phosphorene (BP). The syntheses of ML GeSe<sup>7</sup> and ML GeTe<sup>8</sup> by mechanical exfoliation have been demonstrated. In contrast to the instability of BP and low carrier mobility of the transition-metal dichalcogenides (TMDs),<sup>9–12</sup> ML GeSe and GeTe possess both air-stability<sup>13,14</sup> and high carrier mobility,<sup>15–17</sup> which are beneficial for the realization of practical equipment. Moreover, ML GeSe and GeTe have moderate band gaps<sup>13,15,18–20</sup> and anisotropic electronic properties,<sup>13,15,21</sup> which are very attractive merits for a competitive channel of TFET with a planar homogeneous p-i-n architecture. However, the performance limits of ML GeSe and GeTe based new-mechanistic devices are not known. Due to their superior stability and dramatic electronic properties, it is of vital scientific significance to explore the device performance limits of the ML GeSe and GeTe TFETs and NCTFETs.

In this study, we explore the device performance limits of the ML GeSe and GeTe TFETs, when their physical gate length is  $L_g = 10 \text{ nm}$  with various doping concentrations and supply voltages by the rigorous *ab initio* quantum transport simulation. For the optimal ML GeTe TFETs, the values of  $I_{on}$  (HP) are even more extensive than those of the optimal ML GeSe TFETs and exceed the ITRS demands for HP devices until  $V_{dd}$  is less than 0.65 V. Moreover, the optimal ML GeSe TFETs still surpass the ITRS demands for the LP logic devices at a  $V_{dd}$  of 0.65 V. Furthermore, we choose four different ferroelectric dielectrics

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to construct a prototype negative capacitance TFET (NCTFET) to improve the performance of the logic devices. We found that the performance of the optimal ML GeSe and GeTe NCTFETs can increase dramatically and exceed the ITRS demands for both LP and HP logic devices at a lower  $V_{dd}$  of 0.55 V. In addition, lower delay time ( $\tau$ ) and power dissipations (PDP) can be obtained in all the ML GeSe and GeTe TFETs, which are much smaller than those of the ITRS requirements.

## Models and computational methods

With the optimal ML GeSe and GeTe structures (see Fig. 1(a)), a double-gated (DG) TFET model with a planar p-i-n architecture is built, as shown in Fig. 2(a), that is, the source region is doped with p-type, the gate region is intrinsic, and the drain region is doped with n-type. The transport mechanism of the carriers is band-to-band tunneling (BTBT) in this p-i-n

architecture. The tunneling barrier is formed in the intrinsic region, which can be tuned to switch on and off through the gate voltage. We set the length of the gate region ( $L_g$ ) to 10 nm and the thickness of the  $\text{SO}_2$  dielectric layer to 0.56 nm. Various p-n-type source/drain doping concentrations ( $N_S/N_D$ ) are taken to optimize the device leakage currents ( $I_{\text{leak}}$ ) and on-state currents ( $I_{\text{on}}$ ). We study the device performances of the selected ML GeSe and GeTe TFETs with optimal  $N_S/N_D$  under a series of the supply voltage ( $V_{dd}$ ) of 0.4–0.74 V with regards to the ITRS 2015 version. Here,  $V_{dd}$  is the chosen gate voltage drop, which equals to the source-drain voltage, and the value of  $V_{dd}$  with regards to the year target of the ITRS 2015 version, *i.e.*,  $V_{dd}$  of 0.74, 0.65, 0.55, 0.45, and 0.4 V refers to the technical node range of “11/10”, “6/5”, “4/3”, “3/2.5”, and “2/1.5”, respectively.

The electronic property and geometric structures of the ML GeSe and GeTe are investigated using density functional theory (DFT), and the device performances of the ML GeSe and GeTe

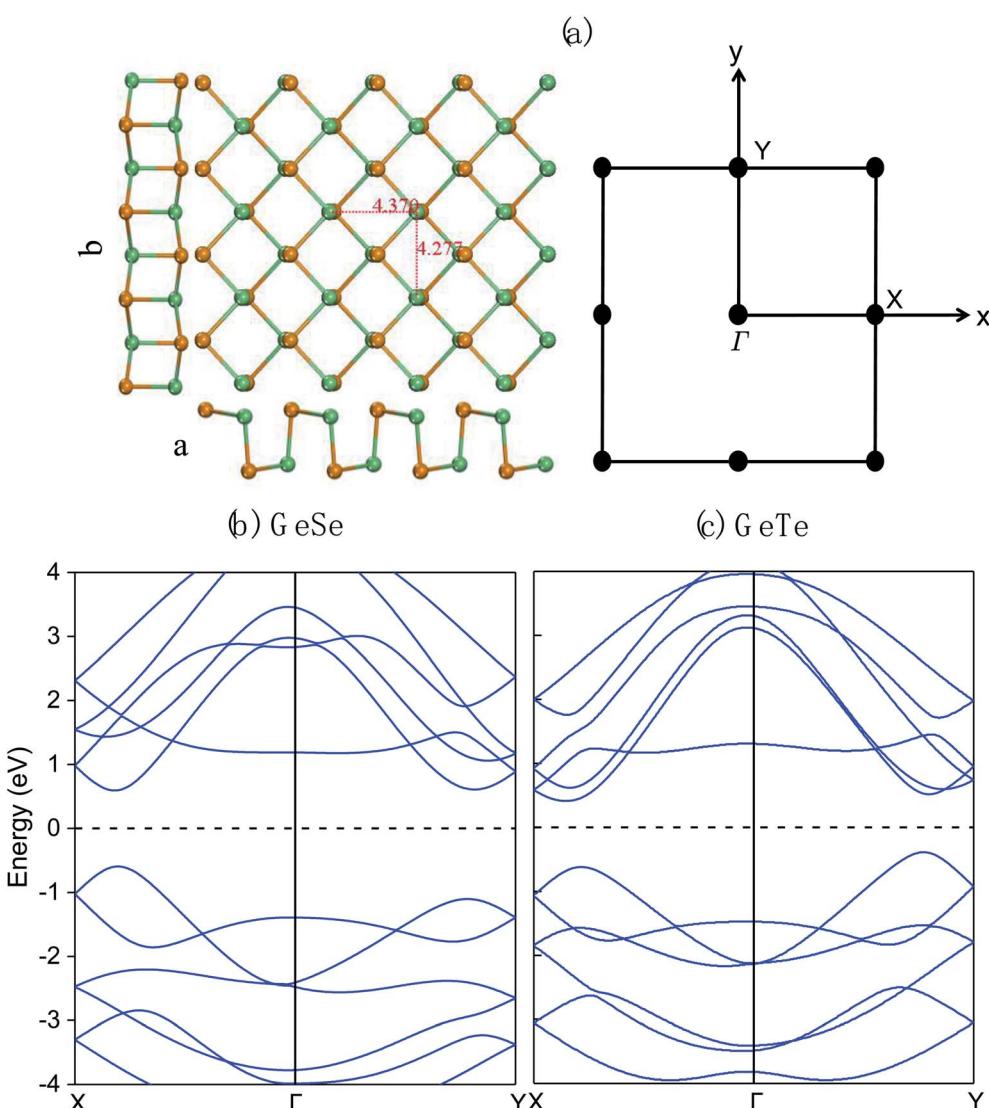


Fig. 1 (a) Top and side views of ML GeTe. (b and c) Band structure of the ML GeSe and GeTe. Green ball: Ge atom; brown ball: Te atom.  $\Gamma$ –Y and  $\Gamma$ –X represent the zigzag and armchair directions, respectively.



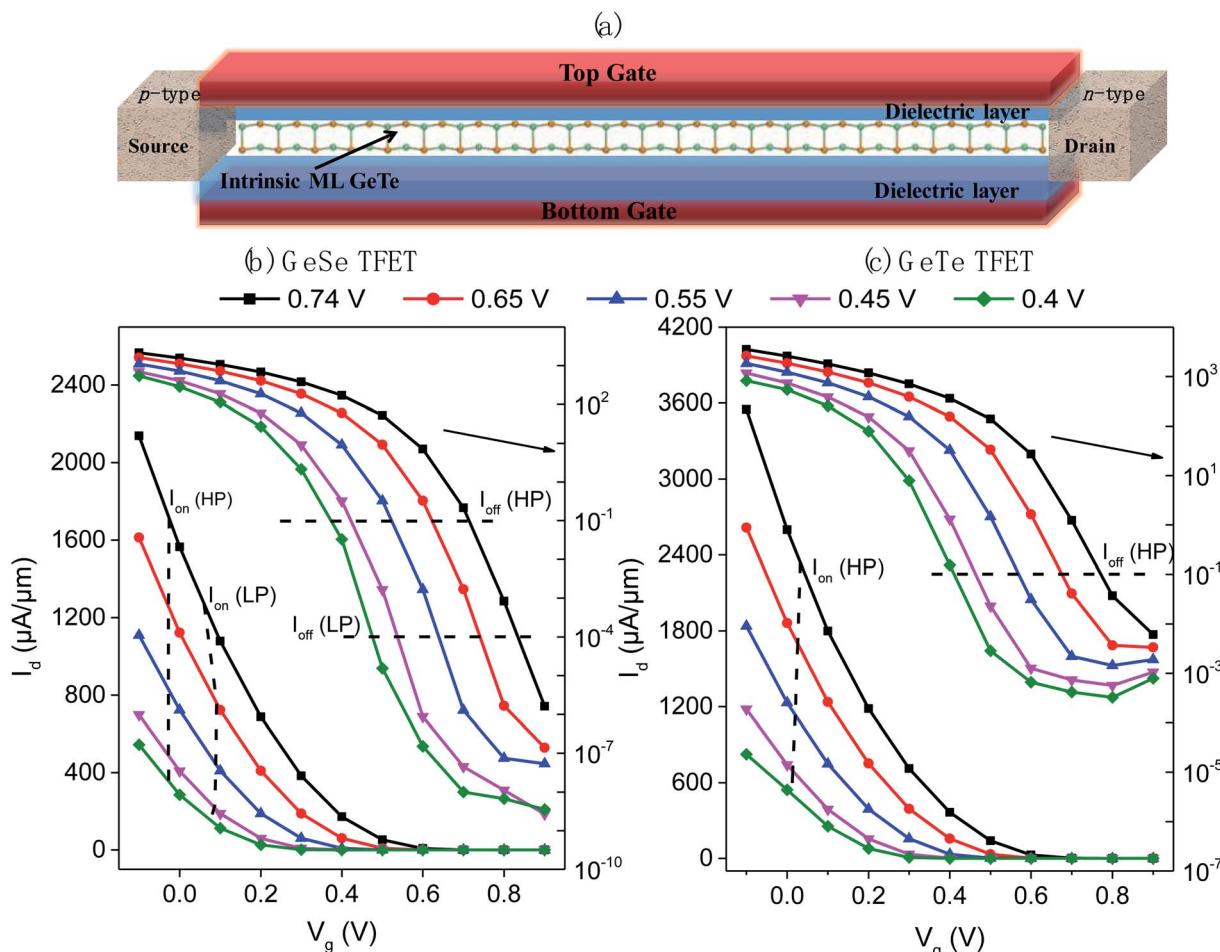


Fig. 2 (a) Device model of the ML GeTe TFET. Transfer characteristics of the ML GeSe (b) and GeTe (c) TFETs with  $L_g = 10$  nm at  $V_{dd}$  of 0.4–0.74 V. The ITRS requirements for HP and LP devices (2015 version) are given for comparison.  $N_S/N_D = 0.1/5 \times 10^{13} \text{ cm}^{-2}$  for each TFETs.

TFETs are calculated using the non-equilibrium Green's function (NEGF) method based on the DFT, the so-called DFT + NEGF approach. Both the methods are executed in the package of Atomistix Tool Kit (2017 version).<sup>22–24</sup> The generalized gradient approximation of Perdew–Burke–Ernzerhof (GGA-PBE) was chosen as the exchange-correlation function.<sup>25</sup> The pseudopotential is 'SG15' norm-conserving pseudopotential, and the basis set is 'Medium'. The density mesh cut-off energy and electron temperature are set as 100 Ha and 300 K, respectively. The Monkhorst–Pack  $k$ -point sampling<sup>26</sup> is  $31 \times 31 \times 1$  for 2D crystal calculation and  $1 \times 31 \times 151$   $k$ -points for device simulation. The convergence criteria are  $10^{-3}$  eV Å<sup>-1</sup> and  $10^{-5}$  eV for the maximum force and energy, respectively. The convergence criteria are  $10^{-3}$  eV Å<sup>-1</sup> and  $10^{-5}$  eV for the maximum force and energy, respectively.

After self-consistent, we calculate the transmission coefficient  $T(E, k_y)$  using the equation as follows:

$$T(E, k_y) = \text{Tr}[G^r \Gamma_S(E, k_y) G^a \Gamma_D(E, k_y)]$$

Here,  $G^{r/a}$  is the retarded/advanced Green's function and  $\Gamma_{S/D}(E, k_y) = i(\sum_{S/D}^r(E, k_y) - \sum_{S/D}^a(E, k_y))$  is the line width function

expressed in terms of the electrode self-energies  $\sum_{S/D}^{r/a}(E)$  for the Source and Drain. Then, the average of  $T(E, k_y)$  over 61  $k_y$ -points in the Brillouin zone can be used to obtain the transmission spectrum  $T(E)$ . The current  $I(V_{DS}, V_g)$  can be calculated according to the Landauer–Büttiker formula<sup>27</sup> at a given gate voltage  $V_g$  and bias voltage  $V_{DS}$  by integrating the  $T(E)$ :

$$I(V_{DS}, V_g) = \frac{2e}{h} \int_{-\infty}^{+\infty} \{ T(E, V_{DS}, V_g) [f_S(E - \mu_S) - f_D(E - \mu_D)] \} dE$$

where  $f_{S/D}$  is the Fermi–Dirac distribution function, and  $\mu_S/\mu_D$  is the electrochemical potential for the Source/Drain. By self-consistently solving the Poisson equations, the gate effect can be realized.

We choose four different ferroelectric capacitors (*i.e.*, BaTiO<sub>3</sub>, Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> (HZO), PZT, and SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub>) to construct a negative capacitance TFET (NCTFET) for the ML GeSe and GeTe channels at the  $V_{dd}$  of 0.55 V. With the combination of the Silvaco Atlas commercial simulator and the Landau–Khalatnikov (L–K) theory of ferroelectrics, we can calculate the voltage drop  $V_{NC}$  across the ferroelectric film.<sup>28,29</sup>

$$V_{NC} = 2\alpha t_{Fe}Q + 4\beta t_{Fe}Q^3 + 6\gamma t_{Fe}Q^5$$

where  $t_{Fe}$  is the thickness of the ferroelectric dielectrics,  $\alpha$ ,  $\beta$ , and  $\gamma$  are the Landau coefficients of the ferroelectric film, and  $Q$  is the electrical charge on the channel, which we get from the Mulliken population based on DFT. We take the four series of  $\alpha$ ,  $\beta$ , and  $\gamma$  from ref. 30–33 with the values of  $-1 \times 10^7$ ,  $-8.9 \times 10^8$ , and  $4.5 \times 10^{10}$  for BaTiO<sub>3</sub>,  $-1.35 \times 10^8$ ,  $3.05 \times 10^8$ , and  $-2.11 \times 10^7$  for PZT,  $-1.911 \times 10^8$ ,  $5.898 \times 10^9$ , and 0 for HZO and  $-1 \times 10^7$ ,  $-8.9 \times 10^8$ , and  $4.5 \times 10^{10}$  for SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub>, respectively. We can then obtain the enhanced effect of gate control on the channel material of the NCTFET, that is, with a chosen zero drain current  $I_d$  point like the leakage current, a smaller gate voltage drop ( $V_g$  subtracts  $V_{NC}$ ) is obtained for the same  $I_d$ . This also means a higher  $I_d$  for the same gate voltage drop. With a point by point calculated new gate voltage ( $V_g - V_{NC}$ ) from the above  $V_{NC}$  equation, we get a new transfer characteristic for the NCTFET.

## Results and discussion

### Geometric and electronic properties

ML GeSe and GeTe have puckered honeycomb networks with orthorhombic crystal structures similar to that of BP. The side and top views of the relaxed puckered atomic configuration of the ML GeTe in the armchair and zigzag directions are shown in Fig. 1(a). The band structures of ML GeSe and GeTe are given in Fig. 1(b) and (c). ML GeSe is a direct gap semiconductor, while ML GeTe is a semiconductor with an indirect bandgap. ML GeSe and GeTe show anisotropic electronic behaviors as the band dispersions along the zigzag ( $T$ – $Y$ ) and armchair ( $T$ – $X$ ) directions are asymmetric. We summarize the optimized lattice parameters, bandgap values, and effective masses in Table 1, with available published results given for comparison. The lattice lengths  $a/b$  are 4.27/3.99 Å and 4.37/4.28 Å, for ML GeSe and GeTe, respectively. The value of the bandgap is 1.18 eV for ML GeSe, while the direct/indirect bandgap value of ML GeTe is 0.91/0.80 eV, respectively. The electron/hole effective masses are 0.13/–0.14 and 0.10/–0.12  $m_0$  for ML GeSe and GeTe along the zigzag direction, respectively, which are lighter than those of 0.22/–0.29 and 0.23/–0.17  $m_0$  along the armchair direction. Our calculated lattice lengths, gaps, and electron/hole effective masses are in good agreement with the former calculated and published results for the GeSe and GeTe, as shown in Table 1.<sup>14,15</sup>

**Table 1** The optimized lattice lengths, band gaps, and effective masses of the ML GeTe and ML GeTe compared with those from previous works of literature.<sup>14,15</sup> The direct (indirect) band gap is also given in the parenthesis

	$a$ (Å)	$b$ (Å)	$E_g$ (eV)	$m_e^a$ ( $m_0$ )	$m_h^a$ ( $m_0$ )	$m_e^z$ ( $m_0$ )	$m_h^z$ ( $m_0$ )
GeSe	4.27	3.99	1.18	0.22	0.29	0.13	0.14
Ref. 14	4.26	3.99	1.11	0.23	0.33	0.14	0.16
GeTe	4.37	4.28	0.91 (0.80)	0.23	0.17	0.10	0.12
Ref. 15	4.40	4.24	0.91 (0.88)	0.28	0.23	0.07	0.1

### Optimal doping concentration

The effect of asymmetric  $N_S/N_D$  is tested at first. From a former study on ML GeSe TFET,<sup>34</sup> we find an enhanced p-type character in the device with a lower  $N_S$  (e.g.,  $N_S/N_D = 1/5 \times 10^{13}$  cm<sup>–2</sup>), while an enhanced n-type character is obtained with an opposite ratio of  $N_S/N_D = 5/1 \times 10^{13}$  cm<sup>–2</sup>. In this study, we fix  $N_D$  to  $5 \times 10^{13}$  cm<sup>–2</sup>, and set  $N_S$  to  $1 \times 10^{13}$ ,  $0.5 \times 10^{13}$  and  $0.1 \times 10^{13}$  cm<sup>–2</sup>, respectively. For the ML GeSe and GeTe TFETs with  $L_g = 10$  nm, the p-type transfer characteristics along the zigzag direction are presented in Fig. S1(a) and (b) in the ESI.†  $I_{leak}$  values of the ML GeSe TFETs are  $8.4 \times 10^{-4}$ ,  $6.8 \times 10^{-5}$ , and  $1.6 \times 10^{-6}$   $\mu\text{A } \mu\text{m}^{-2}$  for  $N_S/N_D$  of  $1/5 \times 10^{13}$ ,  $0.5/5 \times 10^{13}$ , and  $0.1/5 \times 10^{13}$  cm<sup>–2</sup>, respectively, which are more than three orders of magnitude smaller than those of the ML GeTe TFETs ( $1.41$ ,  $0.3$ , and  $6.08 \times 10^{-3}$   $\mu\text{A } \mu\text{m}^{-2}$ ) at the same  $N_S/N_D$ .

The off-current  $I_{off}$  (HP)/ $I_{off}$  (LP) is taken as  $0.1 \times 10^{-4}$   $\mu\text{A } \mu\text{m}^{-2}$  from the ITRS demands (2015 version), and the corresponding  $V_g$  is marked as  $V_{goff}$  (HP)/ $V_{goff}$  (LP). For  $V_{dd} = 0.74$  V,  $I_{on}$  (HP) is then obtained at  $V_{gon}$  (HP) =  $V_{goff}$  (HP) – 0.74 V. The value of  $I_{on}$  (HP) of the ML GeSe TFETs increases from 1654, 1664, to 1715  $\mu\text{A } \mu\text{m}^{-2}$  as  $N_S$  decreases from  $1 \times 10^{13}$ ,  $0.5 \times 10^{13}$  to  $0.1 \times 10^{13}$  cm<sup>–2</sup>, respectively, with all exceeding the ITRS requirement of  $1287 \mu\text{A } \mu\text{m}^{-2}$  for HP devices at similar  $V_{dd}$  of 0.75 V.  $I_{on}$  (HP) of 2342  $\mu\text{A } \mu\text{m}^{-2}$  of the ML GeTe TFET is much larger than those of the ML GeSe TFETs.  $I_{leak}$  values of the ML GeSe TFETs meet  $I_{off}$  (LP) at  $N_S = 0.5 \times 10^{13}$  and  $0.1 \times 10^{13}$  cm<sup>–2</sup>, and the corresponding  $I_{on}$  (LP) are 759 and 1272  $\mu\text{A } \mu\text{m}^{-2}$ , which exceed the ITRS requirement of  $629 \mu\text{A } \mu\text{m}^{-2}$  for the LP devices. In total, the optimal doping concentration is  $N_S/N_D = 0.1/5 \times 10^{13}$  cm<sup>–2</sup> for both the GeSe and GeTe TFETs with regards to  $I_{leak}$  and  $I_{on}$ .

### Device performance

Herein, we explore the device performance limits of the ML GeSe and GeTe TFETs under the optimal doping concentration of  $N_S/N_D = 0.1/5 \times 10^{13}$  cm<sup>–2</sup> with regards to the ITRS demands of HP and LP devices. We plot the enhanced p-type transfer characteristics of the ML GeSe and GeTe TFETs with  $L_g = 10$  nm with different supply voltages ( $V_{dd} = 0.4$ –0.74 V) in Fig. 2(b) and (c) and  $I_{on}$  vs.  $I_{off}$  (HP/LP) in Fig. 3(a). With the decrease in the supply voltages from 0.65 to 0.4 V, the  $I_{on}$  (HP) values of ML GeSe TFETs decrease from 1200 to 355  $\mu\text{A } \mu\text{m}^{-2}$ , which do not reach the requirements of ITRS (2015 version) for HP devices (see Table 2). Notably,  $I_{on}$  (LP) of the ML GeSe TFET is 759  $\mu\text{A } \mu\text{m}^{-2}$  ( $V_{dd} = 0.65$  V), which is 1.2 times of the requirement of  $629 \mu\text{A } \mu\text{m}^{-2}$  of the ITRS (2015 version) for LP devices.  $I_{on}$  (HP) of the ML GeTe TFET is 1699  $\mu\text{A } \mu\text{m}^{-2}$  at  $V_{dd}$  of 0.65 V, which prominently exceeds the requirement (*i.e.*,  $1476 \mu\text{A } \mu\text{m}^{-2}$ ) of ITRS (2015 version) for the HP device. However, as  $V_{dd}$  decreases to less than 0.65 V, the optimal ML GeTe TFETs can still possess high  $I_{on}$  (HP) of 512–1135  $\mu\text{A } \mu\text{m}^{-2}$ , and  $I_{on}$  (LP) of the optimal ML GeSe TFETs is 156–444  $\mu\text{A } \mu\text{m}^{-2}$ , which all cannot exceed the ITRS (2015 version) demands for the HP and LP devices, respectively.

The device dynamic performance metrics are defined by the delay time ( $\tau = \frac{Q_{on} - Q_{off}}{WI_{on}}$ ) and power dissipation



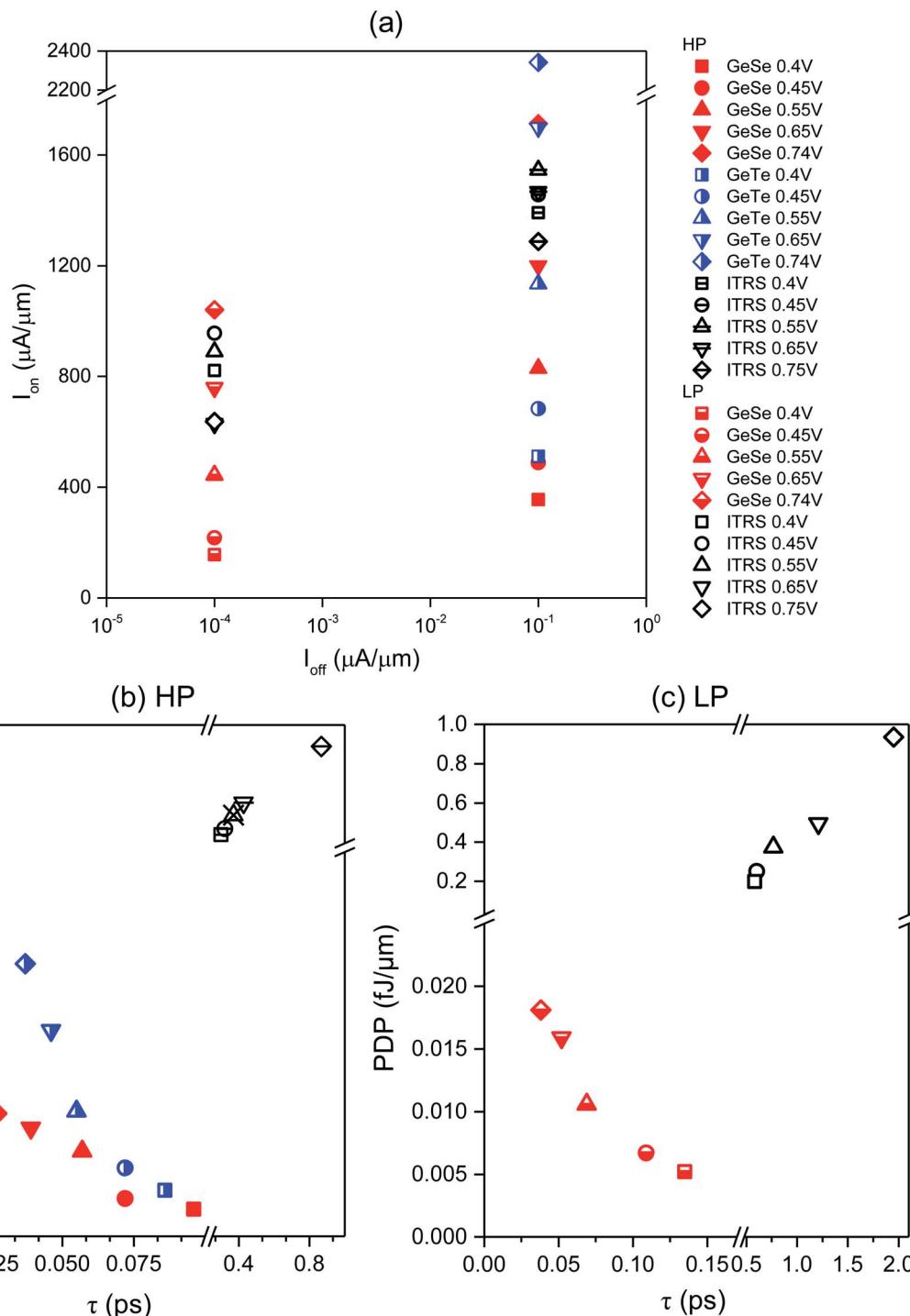


Fig. 3 (a)  $I_{on}$  vs.  $I_{off}$  and (b) and (c) delay time ( $\tau$ ) vs. power dissipation (PDP) of the ML GeSe and GeTe TFETs ( $V_{dd} = 0.4$ – $0.74$  V) against those of the ITRS requirements for HP and LP devices (2015 version).

$\left( PDP = \frac{(Q_{on} - Q_{off})V_{dd}}{W} \right)$ . In the formula,  $Q_{on/off}$  is the overall charge in the gate region for the on-/off-states, and  $W$  is the channel width.  $\tau$  vs. PDP of the optimal ML GeSe and GeTe TFETs with  $L_g = 10$  nm at  $V_{dd} = 0.4$ – $0.74$  V benchmarked with those of the ITRS requirements (2015 version) for the HP and LP

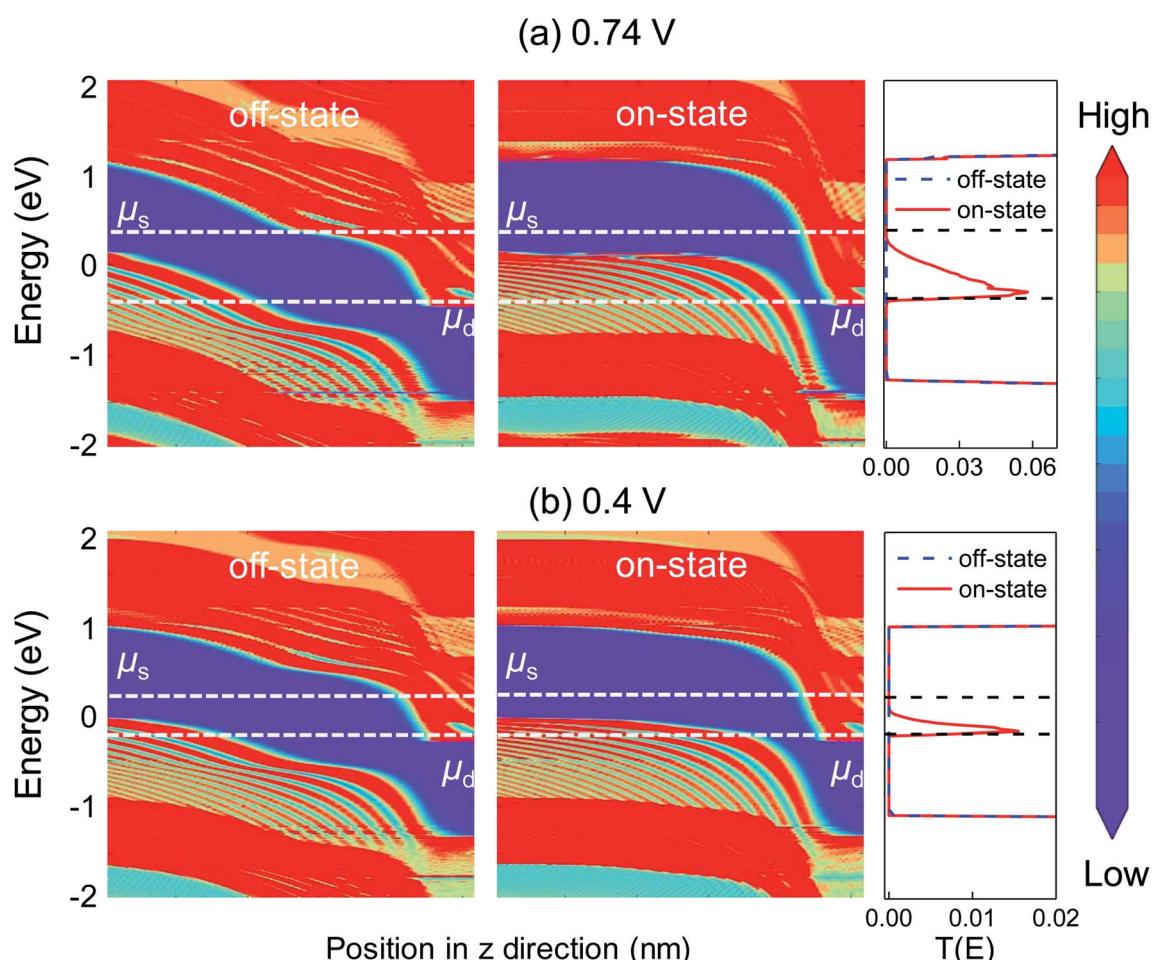
devices, as shown in Fig. 3(b) and (c). We can see that the values of  $I_{on}$  and  $\tau$  descend when the  $V_{dd}$  decreases from 0.74 to 0.4 V, while PDP values improve. A smaller  $\tau$  indicates a faster switching speed, and a smaller PDP marks lower energy consumption. Thus, the left corner is favorable with respect to both fast switching speed and little energy consumption. For HP applications, the values of  $\tau$  of ML GeSe and GeTe TFETs

**Table 2** Device performances of the ML GeSe and GeTe TFETs along the zigzag for HP and LP applications at the  $V_{dd}$  of 0.4–0.74 V. Here,  $L_g = 10$  nm, EOT = 0.56 nm,  $N_s/N_D = 0.1/5 \times 10^{13} \text{ cm}^{-2}$ , and  $I_{off} = 0.1/1 \times 10^{-4} \mu\text{A} \mu\text{m}^{-1}$  for HP/LP application.  $I_{on}$ : on-state current; SS: subthreshold swing;  $\tau$ : delay time; and PDP: power dissipation

	$V_{dd}$ (V)	SS (mV dec $^{-1}$ )	$I_{on}$ (HP) ( $\mu\text{A} \mu\text{m}^{-1}$ )	$\tau$ (HP) (ps)	PDP (HP) (fJ $\mu\text{m}^{-1}$ )	$I_{on}$ (LP) ( $\mu\text{A} \mu\text{m}^{-1}$ )	$\tau$ (LP) (ps)	PDP (LP) (fJ $\mu\text{m}^{-1}$ )
GeSe	0.74	39	1715	0.027	0.021	1272	0.034	0.020
	0.65	38	1200	0.039	0.019	759	0.052	0.016
	0.55	37	829	0.057	0.016	444	0.069	0.011
	0.45	36	489	0.072	0.010	217	0.109	0.007
	0.4	37	355	0.096	0.009	156	0.135	0.005
GeTe	0.74	70	2342	0.037	0.041	—	—	—
	0.65	69	1699	0.046	0.032	—	—	—
	0.55	66	1135	0.055	0.021	—	—	—
	0.45	63	683	0.072	0.014	—	—	—
	0.4	58	512	0.086	0.011	—	—	—

range from 0.027–0.096 ps and 0.037–0.086 ps, respectively, and the values of PDP of ML GeSe and GeTe TFETs range from 0.009–0.021 fJ  $\mu\text{m}^{-1}$  and 0.011–0.041 fJ  $\mu\text{m}^{-1}$ , respectively. They are both smaller than one-tenth and one-twentieth of the ITRS HP requirements of 0.299–0.868 ps and 0.166–0.838 fJ  $\mu\text{m}^{-1}$ ,

respectively. For LP applications, the values of  $\tau$  and PDP of ML GeSe TFETs are 0.034–0.135 ps and 0.005–0.020 fJ  $\mu\text{m}^{-1}$ , which are smaller than one-twentieth and one-fortieth of the ITRS LP requirements of 0.604–1.95 ps and 0.198–0.934 fJ  $\mu\text{m}^{-1}$ , respectively.



**Fig. 4** Local device density of states (LDDOS) and transport spectra of the ML GeTe TFET with a physical gate length of  $L_g = 10$  nm for HP application with  $N_s/N_D = 0.1/5 \times 10^{13} \text{ cm}^{-2}$  at the  $V_{dd}$  of 0.74 V (a) and 0.4 V (b).



**Table 3** Different ferroelectric dielectric device performances of the ML GeSe (LP) and GeTe (HP) NCTFETs with  $L_g = 10$  nm at the  $V_{dd}$  of 0.55 V.  $t_{FE}$ : the thickness of ferroelectric dielectric;  $I_{on}$ : on-state current;  $\tau$ : delay time; and PDP: power dissipation

	Ferroelectric dielectrics	$\alpha$	$\beta$	$\gamma$	$t_{FE}$ (nm)	$I_{on}$ ( $\mu\text{A } \mu\text{m}^{-2}$ )	$\tau$ (ps)	PDP ( $\text{fJ } \mu\text{m}^{-2}$ )	
GeSe	SrBi <sub>2</sub> Nb <sub>2</sub> O <sub>9</sub>	$-3.74 \times 10^8$	$-9.4 \times 10^7$	$1.18 \times 10^9$	80	892	0.036	0.010	
	HZO	$-1.99 \times 10^8$	$5.898 \times 10^9$	0	160	908	0.033	0.010	
	PZT	$-1.35 \times 10^8$	$3.05 \times 10^8$	$-2.11 \times 10^7$	230	920	0.033	0.010	
	BaTiO <sub>3</sub>	$-1 \times 10^7$	$-8.9 \times 10^8$	$4.5 \times 10^{10}$	3000	895	0.033	0.010	
ITRS <sup>35</sup>	LP				—	890	0.766	0.375	
	GeTe	SrBi <sub>2</sub> Nb <sub>2</sub> O <sub>9</sub>	$-3.74 \times 10^8$	$-9.4 \times 10^7$	$1.18 \times 10^9$	50	1822	0.033	0.021
	HZO	$-1.99 \times 10^8$	$5.898 \times 10^9$	0	90	1661	0.036	0.021	
	PZT	$-1.35 \times 10^8$	$3.05 \times 10^8$	$-2.11 \times 10^7$	120	1569	0.038	0.021	
ITRS <sup>35</sup>	BaTiO <sub>3</sub>	$-1 \times 10^7$	$-8.9 \times 10^8$	$4.5 \times 10^{10}$	1600	1559	0.039	0.021	
	HP				—	1546	0.370	0.315	

The sub-threshold swing (SS) is defined as the linear relationship of  $V_g$  and  $\lg I_D$  in the sub-threshold region, which is expressed as  $\text{SS} = \frac{\partial V_g}{\partial \lg I_D}$ . SS of the ML GeSe and GeTe TFETs are 36–39 and 58–70 mV dec<sup>-1</sup> at  $V_{dd} = 0.4$ –0.74 V, respectively. SS of the ML GeSe TFETs is much smaller than that of the thermal diffusion limit of conventional FETs (of 60 mV dec<sup>-1</sup>).

The local device density of states (LDDOS) and transmission spectra of the optimal ML GeTe TFET for the HP application under on- and off-states at the  $V_{dd}$  of 0.74 and 0.4 V are shown in Fig. 4(a) and (b), respectively. The source-to-drain BTBT mechanism can be obviously seen from LDDOS. In the bias windows, the BTBT currents are generated because of the overlap of the source valence bands and drain conduction bands. When it is on-state and off-state, the BTBT barrier width is small and large, respectively. From the transport spectra in the right panels of Fig. 4, a narrower transport spectrum with a lower peak for the on-state is found at  $V_{dd} = 0.4$  V, so that an obvious descend of the  $I_{on}$  is obtained.

## NCTFET

A prototype negative capacitance TFET (NCTFET) is proposed to make  $I_{on}$  meet the standard of ITRS at a lower  $V_{dd}$ . We list the required thicknesses of four ferroelectric materials to make  $I_{on}$  exceed the ITRS demands at  $V_{dd} = 0.55$  V in Table 3. Notably, for the ML GeTe TFET,  $I_{on}$  is 1135  $\mu\text{A } \mu\text{m}^{-2}$ , which dramatically raises to 1822  $\mu\text{A } \mu\text{m}^{-2}$  by adding 50 nm-thick SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub> ferroelectric dielectric to construct the NCTFET architecture for HP device, while 80 nm-thick SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub> is needed for the ML GeSe NCTFET to make the on-state current increase from 444  $\mu\text{A } \mu\text{m}^{-2}$  to 892  $\mu\text{A } \mu\text{m}^{-2}$  for LP devices. The required thicknesses of the HZO/PZT/BaTiO<sub>3</sub> ferroelectric dielectrics are much larger, with 160/230/2300 nm for the ML GeSe NCTFETs and 90/120/1600 nm for the ML GeTe NCTFETs to reach the ITRS requirements. It is found that the NCTFET not only improves the corresponding  $I_{on}$ , but also has positive impacts on  $\tau$ , which are shown in Table 3. The value of  $\tau$  is decreased from 0.069 to 0.036–0.033 ps for the ML GeSe TFETs, while the  $\tau$  decreased from 0.055 to 0.039–0.033 ps for the ML GeTe TFETs. For PDP, the values of the ML GeSe and GeTe NCTFETs are almost equal to those of the ML GeSe and GeTe TFETs. In all, we suggest

SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub> among the checked ferroelectric dielectrics for both the ML GeSe and GeTe NCTFETs.

## Conclusions

In summary, we use the rigorous *ab initio* quantum transport simulation to explore the device performance limits of the 10 nm-gate-long ML GeSe and GeTe TFETs. At a supply voltage of 0.65–0.74 V,  $I_{on}$  of the ML GeSe and GeTe TFETs can meet the ITRS requirements for the LP and HP applications, respectively. Moreover, with the ferroelectric dielectric, we find that adding 80 and 50 nm-thickness of SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub> can elevate the  $I_{on}$  (LP) and  $I_{on}$  (HP) of the optimal ML GeSe and GeTe TFETs by 2 and 1.6 times to exceed the ITRS demands for the LP and HP devices, respectively, at a lower  $V_{dd}$  of 0.55 V. We expect our research to encourage future experimental investigations on the ML GeSe and GeTe NCTFETs at sub-10 nm nodes.

## Conflicts of interest

There are no conflicts to declare.

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