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## A Gd-doped $\text{HfO}_2$ single film for a charge trapping memory device with a large memory window under a low voltage

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In this study, a performance-enhanced charge trapping memory device with a Pt/Gd-doped  $\text{HfO}_2/\text{SiO}_2/\text{Si}$  structure has been investigated, where Gd-doped  $\text{HfO}_2$  acts as a charge trapping and blocking layer. The device demonstrates a large memory window of 5.4 V under a  $\pm 5$  V sweeping voltage (360% of the device with pure  $\text{HfO}_2$ ), which is extremely attractive in low-power applications. In addition, the device also exhibits good retention characteristics with a 24.5% charge loss after the retention time of  $1 \times 10^5$  seconds and robust endurance performance with a 1% degradation after  $1 \times 10^4$  program/erase cycles. It is considered that the high density of defect states and the reduction in the defect energy levels induced by Gd-doping contribute to the performance improvement.

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### Introduction

Recently, charge-trapping memory (CTM) devices, such as a silicon-oxide-nitride-oxide-silicon (SONOS) structure flash memory, have attracted numerous interests for its potential for the further scale down below 15 nm node.<sup>1</sup> Compared with the conventional floating-gate (FG) devices, CTM devices hold numerous advantages of higher reliability, lower operating voltage and simpler manufacturing process.<sup>1,2</sup> However, there are still many challenges from the data retention due to the scaling of the thickness of tunnelling oxide and charge trapping oxide.<sup>3</sup> To overcome these intrinsic shortcomings, high-k materials, such as  $\text{HfO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{TiO}_x$ ,  $\text{ZnO}$  and  $\text{ZrO}_2$ , have been introduced into CTM devices to achieve better charge trapping efficiency and retention capability.<sup>4–10</sup> Moreover, an ideal coexistence of a large memory window and low operating voltage is still a great challenge. Most present CTM devices have negligible memory window while operating at lower than 6 V. For high-k materials, doping is proved to be a potential approach to achieve low-power charging-trapping memories, such as Zr-doped  $\text{BaTiO}_3$  and fluorinated  $\text{ZrO}_2$ ,<sup>11,12</sup> Gd-doped  $\text{HfO}_2$  (GHO), as one of promising high-k materials, has been proposed to have a relatively high trap density, large conduction

band offset and high dielectric constant.<sup>13</sup> Moreover, a GHO thin film also has excellent compatibility with CMOS processing. Therefore, it is expected that GHO should have good charge trapping characteristics and will be a promising candidate for the next generation flash memory. In recent years, the potential of GHO films for CTM applications has been proved,<sup>14</sup> but the charge trapping mechanisms are still not well understood.

In this study, Pt/GHO/ $\text{SiO}_2/\text{Si}$  structure (MGOS) cells were fabricated and investigated for CTM applications, where the simple thin GHO film acts as the charge trapping and blocking layer. The experimental results demonstrate that the MGOS devices hold a remarkable charge-trapping efficiency. A large memory window of 5.4 V is observed under a low operating voltage of 5 V, while the P/E speed and retention characteristic are not sacrificed. Furthermore, the charge trapping mechanism of the MGOS is discussed.

### Experiment

A 2-inch p-type (100) silicon wafer with a resistivity of  $1\text{--}10 \Omega \text{ cm}$  was cleaned by the standard RCA process, and then the native oxide on the Si wafer was removed using diluted HF (DHF) solution for 3 min. Before the high-k deposition, a tunnelling oxide layer of 2 nm was thermally grown in the  $\text{O}_3$  atmosphere at  $300^\circ\text{C}$ . Then, the GHO film was deposited *via* plasma-enhanced atomic layer deposition (PE-ALD) at  $300^\circ\text{C}$ . During this process,  $\text{Gd}(\text{TMHD})_3$ , TDMAH, and  $\text{O}_3$  were used as the precursors for Gd, Hf, and O, respectively. In the following step, Pt top electrodes with an area of  $3.8 \times 10^{-4} \text{ cm}^2$  were sputtered on the surface of the samples using a shadow mask at room temperature. Then, 300 nm Al was sputtered on the backside of the wafer as the bottom electrode. Finally, the samples were

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annealed at 300 °C for 5 min in argon atmosphere using a rapid thermal annealing (RTA) system. The electrical properties of the devices were characterized with a Keithley 4200 SCS analyzer. The cross-sectional morphology of the device was observed *via* high-resolution transmission electron microscopy (HRTEM). The defect states in the GHO films were investigated *via* photoluminescence (PL).

## Results and discussion

A schematic of the fabricated MGOS memory cells and the corresponding cross-sectional HRTEM image are shown in Fig. 1(a) and (b), respectively. As shown in Fig. 1(a), the thickness of the GHO layer is about 30 nm. Also, the SiO<sub>2</sub> layer with bright contrast is about 2 nm in thickness, which indicates a uniform interface with Si to prevent charge tunnelling back to the Si substrate. The sharp interface between GHO and SiO<sub>2</sub> is also observed, which means a less interdiffusion interface that can bring about a good device performance. In our experiments, the Gd concentration in the GHO thin film is 0.5% (determined *via* X-ray photoelectron spectroscopy), where the fabricated CTM devices present the optimum memory window.

To study the memory properties of the MGOS devices, such as memory window, retention and endurance performance, the high frequency (1 MHz) capacitance–voltage (*C*–*V*) measurements were performed at room temperature. Fig. 2(a) demonstrates the *C*–*V* curves of the as-prepared devices under various sweeping gate voltages. The counterclockwise direction of the

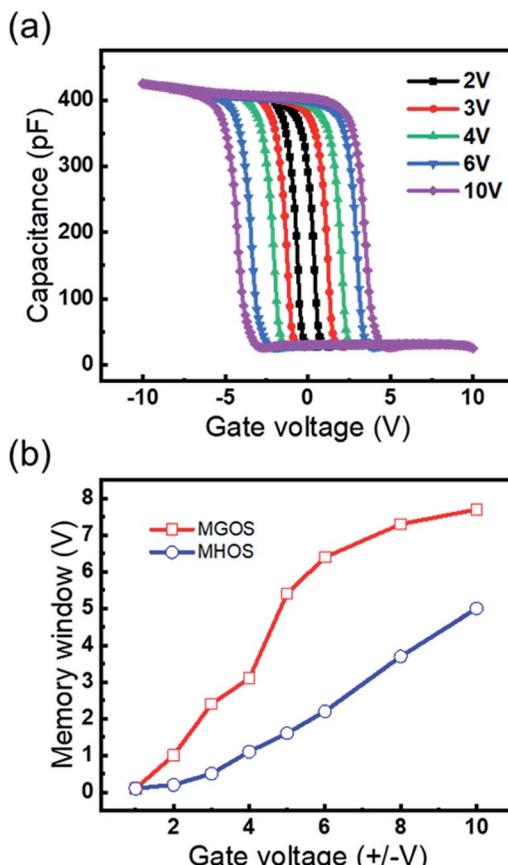


Fig. 2 (a) High frequency (1 MHz) *C*–*V* characteristics of the MGOS device with GHO film; (b) memory window versus gate voltage characteristics of the MGOS and MHOS device.

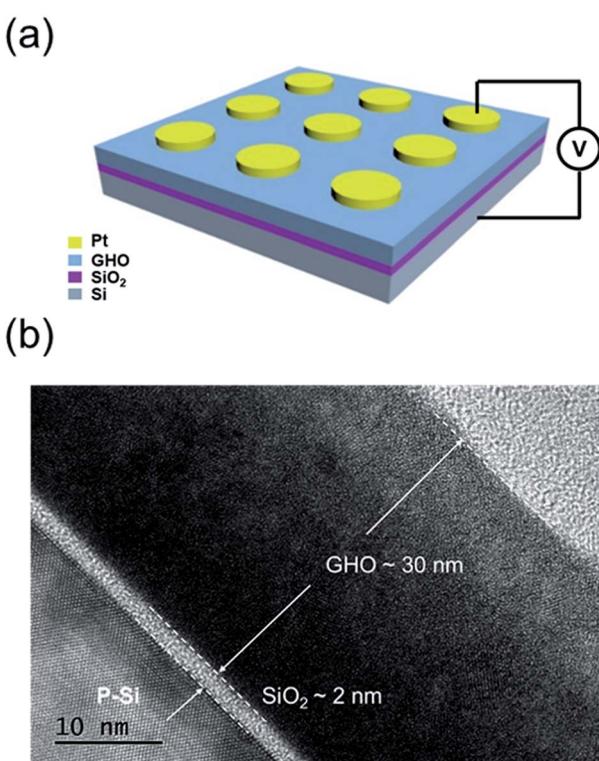


Fig. 1 (a) A schematic of the MGOS device structure and (b) the cross-sectional HRTEM image for a single Gd-doped HfO<sub>2</sub> film.

*C*–*V* hysteresis during a positive-negative-positive voltage sweep demonstrates the typical hysteresis loop direction of charge trapping. The memory window is defined as the difference in the flat-band voltages (*V*<sub>FB</sub>) between the program and erase states, which increases with the increase of the sweeping voltages. A large memory window of 5.4 V under a  $\pm 5$  V sweeping voltage occurred, indicating an excellent charge trapping effect under a low operating voltage. When the sweeping voltage is further increased above 6 V, the memory window shows a saturation tendency and reaches the maximum value of 7.7 V under 10 V. The density of trapped charges per unit area (*N*<sub>t</sub>) can be approximately estimated by the following equation:<sup>15</sup>

$$N_t = \frac{C_{ox} V_{FB}}{qA}, \quad (1)$$

where *C*<sub>ox</sub> represents the capacitance in the accumulation region; in this case, *C*<sub>ox</sub> = 425 pF. *A* is the effective area of the Pt electrode; in this case, *A* =  $3.8 \times 10^{-4}$  cm<sup>2</sup>. *q* is the charge of an electron. According to this equation, the trapped charge density in the MGOS device is about  $5.4 \times 10^{13}$  cm<sup>-2</sup>, 700% of it in the MHOS device,<sup>19</sup> which shows that the GHO film deposited by PE-ALD can offer a high density of charge traps. To further understand the CTM behavior of the GHO film, a control sample with a Pt/HfO<sub>2</sub>/SiO<sub>2</sub>/Si (MHOS) structure, where pure



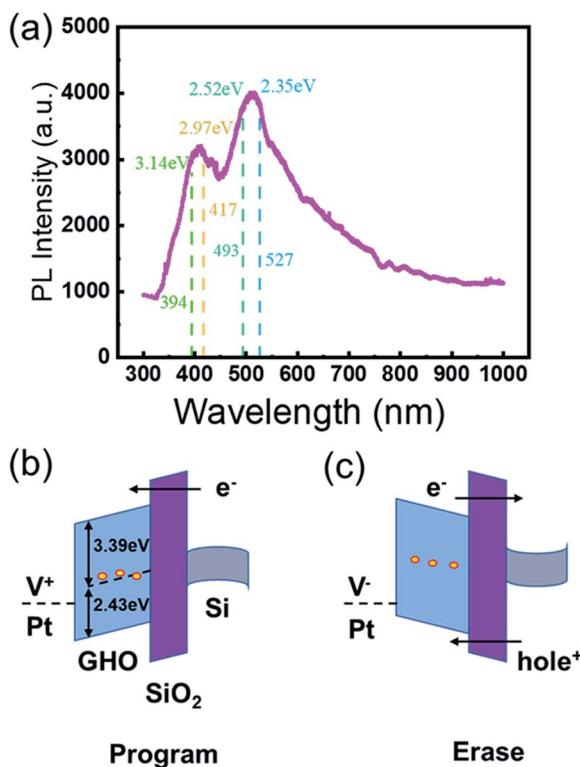


Fig. 3 (a) Photoluminescence spectra of GHO films; (b) a schematic of the energy levels of the defect states and the programming process of the MGOS device; and (c) a schematic of the erasing process of the MGOS device.

$\text{HfO}_2$  acts as a charge trapping layer is also investigated. Fig. 2(b) shows the memory window *versus* gate voltage characteristics of the MGOS and MHOS devices. Clearly, the memory window of the MGOS sample is 260% larger than that of the MHOS sample under an operating voltage of 5 V. The results show that Gd doping can induce a significant performance improvement under a low operating voltage. Alternatively, the charge tunnelling barrier is reduced. Even if the gate voltage is below 2 V, an effective charge trapping process still exists.

In the conventional tri-layer CTM devices, the quantum well is proposed to be responsible for the charge trapping effects, which usually formed by the different band offsets of the blocking layer, charge trapping layer and tunnelling layer.<sup>16,17</sup> However, such a quantum well is not in this MGOS device as there is no blocking layer. Thus, the quantum well is not the origin of the excellent charge trapping effect. It has been reported that some intrinsic defects exist in the  $\text{HfO}_2$  films, such as oxygen vacancies and interstitial oxygen atoms, which induce defect energy levels.<sup>18</sup> The high charge trapping efficiency is attributed to these defect energy levels.<sup>19</sup> In this study, the charge trapping capability has a remarkable improvement as a result of the doping of Gd.

In order to prove the above viewpoint, the position of majority charge traps in this MGOS device was estimated with the calculation of charge trap centroid. The charge trap centroid

( $X_{\text{cent}}$ ) can be calculated by the so-called constant current stress (CCS) method<sup>20</sup> with the following equation:

$$X_{\text{cent}} = \frac{t_{\text{stack}}}{\left[ 1 - \Delta V_g^- / \Delta V_g^+ \right]}, \quad (2)$$

where  $X_{\text{cent}}$  is the distance measured from the Pt/GHO layer interface,  $t_{\text{stack}}$  is the thickness of GHO/ $\text{SiO}_2$ ,  $\Delta V_g^-$  and  $\Delta V_g^+$  are the maximum negative and positive gate voltage shift under constant current stress, respectively. The calculated  $X_{\text{cent}}$  is 15.8 nm, which illustrates that the charge traps are mainly located in the GHO layer instead of the interface between GHO and  $\text{SiO}_2$ .

To further investigate the defect states of the GHO film, photoluminescence (PL) characterization was carried out. As shown in Fig. 3(a), the photoluminescence spectra under a 325 nm excitation wavelength shows clear PL peaks at 2.35–2.52 eV and 2.97–3.14 eV for the GHO film. Considering that the band gap of the GHO film is around 5.82 eV,<sup>13</sup> we believe that the PL peaks at 2.35–2.52 eV and 2.97–3.14 eV cannot originate from the band-to-band recombination. Instead, it is most probably due to the recombination from defect states induced by  $\text{V}_0$  to valence band ( $E_V$ ) or donor defect states to acceptor states, which indicates the existence of the high concentration defects in the GHO films.

According to the theoretical simulations on defect energy levels, the defect states mainly occupy the donor levels rather than the acceptor levels in the GHO film.<sup>18</sup> Therefore, the strongest PL peak at 2.43 eV shown in Fig. 3(a) is assigned to the recombination processes from the donor states at 2.43 eV above  $E_V$  to the  $E_V$  of the GHO film. It can be assumed that the electrons are first excited to the defect states of 2.43 eV above  $E_V$ , and then recombine with the holes in the valence band with luminance. In conclusion, we put forward that the dominant defects are situated at 2.43 eV above the valence band. The energy level positions of the defect states are schematically shown in Fig. 3(b), where the band gaps of  $\text{SiO}_2$  and GHO are 9 eV and 5.82 eV, respectively. The charge trapping and escaping processes are schematically plotted in Fig. 3(b) and (c). Therefore, the efficient charge trapping processes in the MGOS device can be explained by the charge transfer between the defect states and the silicon substrate. It is ascertained that the dominant defect energy levels are located at 3.0 eV above the  $E_V$  in pure  $\text{HfO}_2$  films.<sup>19</sup> By contrast, the dominant defect energy levels in GHO films are located at 2.43 eV above  $E_V$ . Therefore, we believe that the performance improvement under a low operating voltage can be ascribed to the energy level shift caused by Gd-doping.

The retention performance of the MGOS device was measured. As depicted in Fig. 4(a), the high and low capacitances are observed at a fixed read voltage of -1 V after  $\pm 5$  V/1 s programming or erasing pulse voltage. After a  $1 \times 10^5$  s retention time, the capacitance of the device exhibits negligible degradation with only 1% charge loss, which is mainly caused by the direct tunnelling from the trap sites to the Si substrate at room temperature. The excellent retention capability can be attributed to the high potential barriers provided by defect



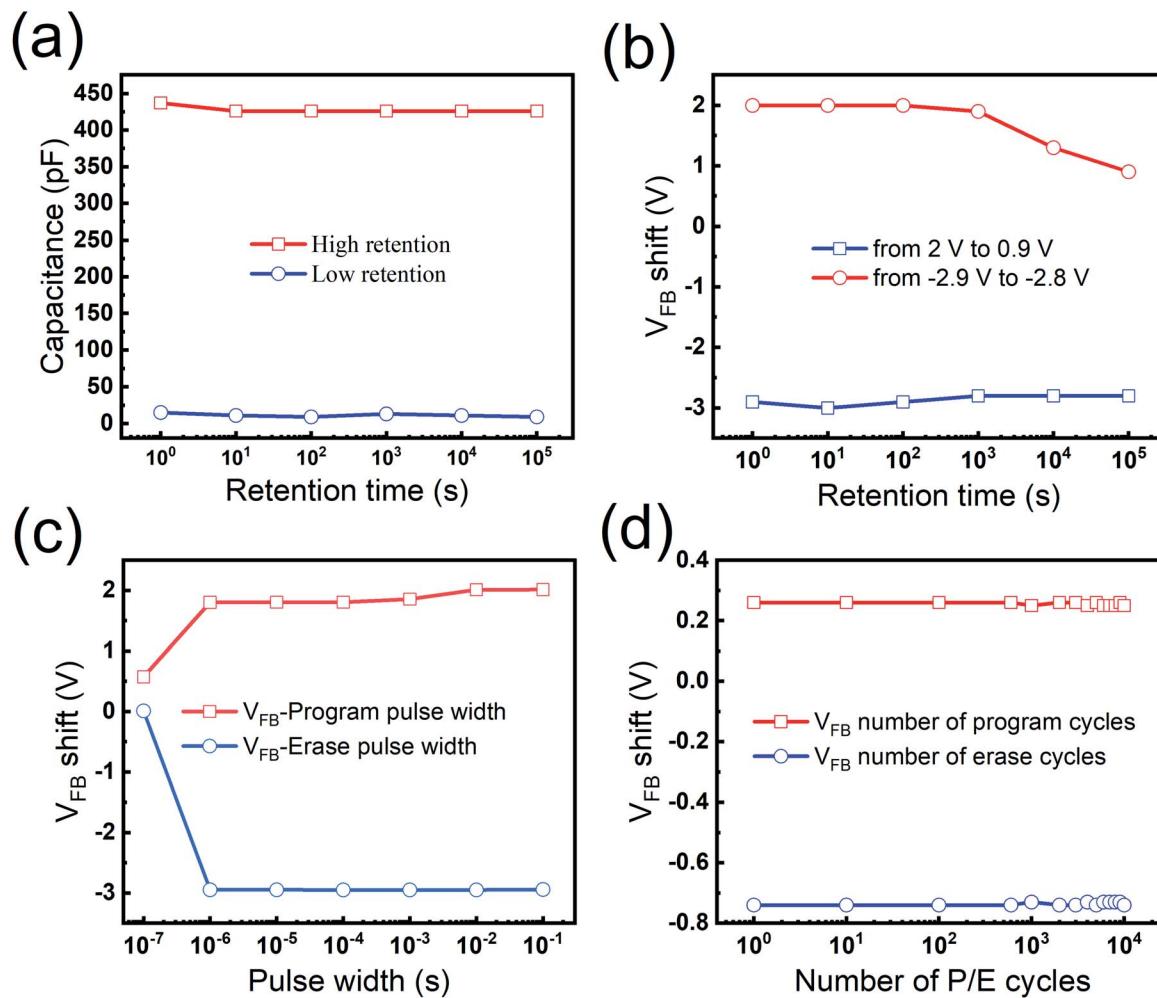


Fig. 4 (a) The high and low capacitances of the memory device based on the single GHO layer and (b) the long-term retention characteristics of the  $V_{FB}$  shift; (c) the program/erase characteristics of the MGOS device and (d) the endurance characteristic of the MGOS device at room temperature.

states in the GHO film, which restrains the trapped charges from tunnelling back to the silicon substrate. To further investigate the retention properties, the flat band voltage ( $V_{FB}$ ) retention characteristics are also investigated, which are shown in Fig. 4(b). The  $V_{FB}$  values retain the large value after  $1 \times 10^5$  s. The charge retention property of memory can be expressed as the percentage of trapped charge loss<sup>21</sup> as below:

$$\text{Charge loss (\%)} = \left( \frac{V_p - V_{100\text{ K}}}{V_p - V_0} \right) \times 100\%, \quad (3)$$

where  $V_0$  is the flat-band voltage of the fresh sample,  $V_p$  is the flat-band voltage after immediately releasing the applied voltage, and  $V_{100\text{ K}}$  is the flat-band voltage after releasing the applied voltage for the retention time of  $1 \times 10^5$  seconds.  $V_{100\text{ K}}$

Table 1 Comparison of the memory windows under low operating voltages for memory devices with various structures

Tunnelling layer	Charge trapping layer	Blocking layer	Operating voltage (V)	Memory window (V)	Total thickness (nm)	References
SiO <sub>2</sub>	Gd:HfO <sub>2</sub>	Gd:HfO <sub>2</sub>	±5	5.4	32	This work
Al <sub>2</sub> O <sub>3</sub>	HfO <sub>2</sub>	Al <sub>2</sub> O <sub>3</sub>	±6	0.8	28	2
SiO <sub>2</sub>	Zr <sub>0.5</sub> Hf <sub>0.5</sub> O <sub>2</sub>	Zr <sub>0.5</sub> Hf <sub>0.5</sub> O <sub>2</sub>	±5	2.0	52.5	6
SiO <sub>2</sub>	Ba <sub>0.6</sub> Sr <sub>0.4</sub> TiO <sub>3</sub>	Ba <sub>0.6</sub> Sr <sub>0.4</sub> TiO <sub>3</sub>	±7	1.1	27	10
SiO <sub>2</sub>	NiO	SiO <sub>2</sub>	±5	2.1	33	17
SiO <sub>2</sub>	HfO <sub>2</sub>	HfO <sub>2</sub>	±6	2.4	59	19
Al <sub>2</sub> O <sub>3</sub>	HfAlO	Al <sub>2</sub> O <sub>3</sub>	±6	4.1	23	22
Al <sub>2</sub> O <sub>3</sub>	ZnO/graphene/ZnO	Al <sub>2</sub> O <sub>3</sub>	±6	4.0	22.6	23

is extracted from the measured  $C$ - $V$  curve in a small range of applied voltage from 2 V to  $-2$  V at a time of  $1 \times 10^5$  seconds. The calculated charge loss is only 24.5%, implying a good retention performance.

To study the P/E characteristics of the MGOS device, voltage pulses of  $\pm 5$  V with various duration are applied to the samples. As shown in Fig. 4(c), the speed of the P/E process is quite fast. With the increase in the pulse width,  $V_{FB}$  increases rapidly in both program or erase operations. To reveal the endurance property, a P/E pulse voltage ( $\pm 2$  V with a pulse width of 10 ms) up to  $10^4$  cycles was applied to the MGOS device. As described in Fig. 4(d), both  $V_{FB}$  curves show negligible degradation. After  $10^4$  cycles of the P/E operation, the  $V_{FB}$  shifts are only 1% lower than their initial values. Therefore, this MGOS device demonstrates an admirable endurance performance, which is a necessary feature for future non-volatile memory devices.

## Conclusion

In summary, we have investigated the memory characteristics and mechanism of the CTM device with the MGOS structure. A comparison of the memory windows at low operating voltages is summarized in Table 1 that includes the CTM devices with various structures. It is demonstrated that the device with a Pt/GHO/SiO<sub>2</sub>/Si structure holds great advantages in low-power consumption applications. A large memory window of 5.4 V is obtained under 5 V. Furthermore, the device also provides good retention characteristics, robust endurance performance, and fast program/erase speed. The efficient charge trapping effects under a low voltage can be attributed to the defect energy levels induced by the oxygen vacancies in the GHO films. Overall, the proposed MGOS structure is a promising candidate for future CTM applications.

## Conflicts of interest

The authors declared that they have no conflicts of interest to this work.

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