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Interface chemistry modulation and dielectric optimization of TMA-passivated HfDyO$_x$/Ge gate stacks using doping concentration and thermal treatment

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In this work, the effects of different Dy-doping concentrations and annealing temperatures on the interfacial chemistry and electrical properties of TMA-passivated HfDyO$_x$/Ge gate stacks have been investigated systematically. The microstructural, optical, interfacial chemistry, and electrical characteristics of sputtering-driven HfDyO$_x$ gate dielectrics have been characterized by means of X-ray diffraction (XRD), UV-Vis transmission spectroscopy, X-ray photoelectron spectroscopy (XPS), and electrical measurements. This work reveals that the interfacial chemistry evolution takes place *via* two competing processes, including oxide growth and oxide desorption. XPS analyses have confirmed that the 10 W-deposited targeted gate dielectrics display optimized interface characteristics, which can be attributed to the suppressed unstable Ge oxides and inhibition effects on inter-diffusion at the interface. Electrical observations show that the 10 W-driven HfDyO$_x$/Ge MOS device without annealing treatment exhibits optimized electrical performance, including a larger permittivity of 22.4, a smaller flat band voltage of 0.07 V, vanishing hysteresis, a lowest oxide charge density of $\sim 10^{11}$ cm^{-2}, and a lowest leakage current density of 2.31×10^{-8} A cm^{-2}. Furthermore, the influences of doping and annealing conditions on the leakage current conduction mechanisms (CCMs) of HfDyO$_x$/Ge MOS capacitors have also been investigated systematically. All of the experimental results indicate that TMA-passivated HfDyO$_x$/Ge gate stacks with appropriate doping concentrations demonstrate potential application prospects for Ge-based MOSFET devices.

1. Introduction

During the last decade, various methods have been investigated to obtain high efficiency and low energy consumption semiconductor microelectronics devices. Conventional Si-based complementary-metal-oxide semiconductor (CMOS) have been scaled down to a fundamental limit leading to the unceasing reduction of gate oxide thickness, which contributes to extensive leakage current through ultra-thin gate dielectrics for the metal-oxide-semiconductor (MOS) devices. To overcome the scaling limits of Si-based CMOS, alternative methods using high-permittivity (high-*k*) dielectric materials have been extensively investigated to avoid a large gate leakage current and maintain capacitance density on several nanometer scales by improving the physical thickness of the gate dielectric thin films. Therefore, in view of the physical microstructure and electrical characteristics, Hf-based high-*k* insulation materials have been extensively investigated as next-generation candidates to replace conventional SiO$_2$ gate dielectrics beyond a few nanometers in technology nodes.[1–4] In addition, as potential candidates for high-*k* gate dielectrics, Hf-based dielectrics have demonstrated some advantages, such as a relatively high permittivity, suitable band gap, and a satisfactory breakdown electric field strength. However, the direct deposition of HfO$_2$ still has some disadvantages, including the low crystallization temperature and the high interface defects owing to its oxygen affinity, which prevents improvement of the interface chemistry and electrical performance.
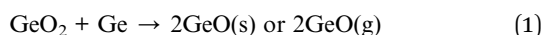
Recently, investigation of HfO$_2$ doped with rare-earth elements (La, Gd, Y, Dy, Yb) has received significant attention, which could be due to the fact that doping can reduce the oxygen vacancy and increase the dielectric constant. In the current work, a Dy-doped HfO$_2$ (HDO) gate dielectric was investigated as a high-*k* gate dielectric and displayed an improved performance, such as the comparative band offset, a suitable band gap, a small amount of hysteresis, and a reduced leakage current, which lays a solid foundation for use in high-performance and low-power semiconductor devices.

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Although the performance of the Si-based CMOS device has been significantly optimized by using high-k gate dielectrics to replace the conventional SiO_2 gate dielectric, the coulomb scattering and phonon scattering lead to a striking reduction in the channel carrier mobility, which significantly reduces the operating speed of the Si-based CMOS devices. Therefore, to further improve the device performance, candidate channel materials such as germanium (Ge) and GaAs (III–V) compound semiconductors have been studied to increase the carrier mobility in the channel region. Among the modified channel materials, Ge is a leading candidate owing to its higher intrinsic carrier mobility and lower band gap compared with the conventional Si substrate. However, the Ge-based CMOS process may produce extrinsic trapped charges and unacceptable interfacial oxidation charges owing to the existence of native oxides and the unstable Ge sub-oxides. The high density of the interface states (D_{it}) of the high-k/Ge gate stack can cause Fermi level pinning, which can adversely degrade the electrical properties of the Ge-based CMOS devices. On the one hand, the unstable Ge sub-oxides occurring on the Ge surface could be primarily attributed to the Ge diffusion or relative thermal instability and water solubility of the Ge oxide, which can be expressed using the following interface reaction:

$$GeO_2 + Ge \rightarrow 2GeO(s) \text{ or } 2GeO(g) \tag{1}$$

On the other hand, the re-diffusion of Ge into the dielectric and the inter-diffusion of the interface occur throughout all the deposition and annealing processes.[5] As a result, the diffusion leads to degradation of the interface chemistry and a destructive electrical performance, including the unignorable hysteresis and the relatively larger flat band voltage.[6,7] Therefore, for the successful implementation of Ge-based metal-oxide-semiconductor field-effect transistors (MOSFETs), surface treatment of the Ge substrate before deposition of the high-k gate dielectrics is the key to improve the quality of the Ge-based semiconductor devices. As we known, traditional surface treatment include conventional wet processes and interface passivation, such as nitridation, bromination, or plasma cleaning of the GeO_x interlayer and sulfur passivation, and so forth.[8–11] Although the above conventional interface processing can suppress the Ge diffusion and the formation of the native oxide, it also produces an unacceptably low-k dielectric layer. The low-k dielectric layer prevents the reduction in the equivalent oxide thickness (EOT) for Ge-based complementary metal-oxide-semiconductor field-effect transistors (CMOSFETs). As a result, a new interface control should be explored.

Recently, atomic layer deposition (ALD)-driven trimethyl aluminum (TMA) with a self-cleaning effect has been investigated systematically to suppress the inter-diffusion and improve the interface stability of a high-k/Ge gate stack.[12,13] Based on these reports, it can be noted that the TMA precursor cleaning can effectively remove the intrinsic oxide on the Ge surface and reduce the EOT of the high-k/Ge gate stack, thereby improving the electrical properties of the device, including the increased dielectric constant and the suppressed leakage current. In spite of the improved electrical performance, the evolution of interface chemistry dielectric properties and the leakage current mechanism of the TMA-passivated $HfDyO_x$/Ge gate stack as functions of the doping concentration and annealing temperature have not been investigated in detail. In the current work, prior to the deposition of the $HfDyO_x$ gate dielectric, Ge was subjected to a combination of S passivation and TMA precursor cleaning by exposure to $(NH_4)_2S$ solution and an ALD vacuum chamber, respectively. The Dy-doping concentration and annealing temperature dependent interfacial chemistry stability and electrical performance of the TMA-passivated $HfDyO_x$/Ge gate stacks have been studied systematically. In addition, further attention has been paid to the investigation of the leakage current conduction mechanism for $HfDyO_x$/Ge gate stacks.

2. Experimental

p-type Ge (100) wafers were dipped in acetone at 80 °C for 10 min to remove organic contamination. The Ge wafers were then washed with ethanol solution to remove superfluous acetone, followed by a mixed solution of $NH_3 \cdot H_2O : H_2O = 1 : 4$ at room temperature for 5 min to remove the surficial oxides layer, and were then processed by H_2O_2 solution ($H_2O_2 : H_2O = 1 : 5$) for 1 min to facilitate the formation of oxide layers. Then, the as-cleared Ge wafers were soaked in 20% $(NH_4)_2S$ solution at room temperature for 20 min to remove the oxides layers and passivate the surface dangling bonds. After that, it was rinsed with deionized (DI) water to remove the residual solution and blown dry with pure N_2. Finally, the as-cleaned Ge wafers were transferred quickly into the ALD vacuum chamber. Before deposition of the gate dielectrics, fifteen cycles of TMA pre-pulsing were performed on all of the Ge substrates. In this work, the TMA pulsing cycle consisted of a TMA pulse (0.02 s)/ N_2 purge (8 s) at 200 °C. During the TMA rinsing process, the chamber base pressure and temperature in the ALD process were 1.0 torr and 200 °C, respectively. After passivation, the *ex situ* $HfDyO_x$ gate dielectric layers were deposited using co-sputtering with a HfO_2 (99.995%) target and a metal Dy (99.95%) target under an Ar/O_2 (=30/5 sccm) atmosphere at room temperature. The background vacuum and the working pressure was controlled at 5.0×10^{-4} and 0.5 Pa, respectively. The radio-frequency power of the HfO_2 target was kept at 60 W. However, different amounts of Dy doping of the $HfDyO_x$ films were achieved by changing the direct-current power fixed at 5, 10 and 15 W, which were marked as S1, S2, and S3, respectively. The dielectric films deposition process was implemented using high vacuum system equipment (JGP-DZS, Chinese Academy of Sciences, Shenyang Scientific Instrument Co., Ltd). To investigate the annealing temperature-dependent interface chemistry and the electrical characteristics, $HfDyO_x$/Ge gate stacks sputtered at 10 W were thermally treated from 400 to 600 °C, which were assigned as S4, S5 and S6, respectively. To study the interfacial chemical composition of the $HfDyO_x$/Ge gate stacks, 5–6 nm $HfDyO_x$ films were deposited on the Ge substrates for all of the S1–S6 samples. *Ex situ* XPS measurements were performed with an ESCALAB 250Xi system using an Al Kα radiation source (1486.7 eV). The hemispherical analyzer was

implemented with a pass energy of 20 eV. The take-off angle and each energy step of the high-resolution XPS spectrum were set at 58° and 0.1 eV, respectively. The HfDyO$_x$ films (∼50 nm) were deposited on the cleaned quartz wafers and Ge substrates to obtain their optical band gaps (E_g) using ultraviolet-visible spectroscopy (UV-Vis, Shimadzu, UV-2550). The thickness of all of the HfDyO$_x$ films was obtained by using *ex situ* spectroscopy ellipsometry (SC630, SANCO Co, Shanghai) in air at room temperature. The measuring wavelength range and step were set at 190–900 nm and 10 nm and the incident angles were kept at 65° and 75°.

To investigate the electrical properties, Al/HfDyO$_x$/Ge/Al MOS capacitors were fabricated by sputtering the Al top and back electrode, the top electrode was obtained through a shadow mask with an area of 3.14×10^{-4} cm^2. Forming-gas (N$_2$ 96% + H$_2$ 4%) annealing (FGA) was performed at 300 °C for 4 min on the MOS capacitors to decrease the contact resistance. In addition, the capacitance *versus* voltage (C–V) and gate leakage current *versus* voltage (J–V) curves were measured by using a semiconductor parameter analyzer device (Agilent B1500A) combined with a Cascade Probe Station. A short circuit and open circuit calibration were required before the actual measurements. Here, all of the electrical characteristic measurements were recorded in a shielded darkroom at room temperature.

3. Results and discussion

3.1 Microstructure characteristics

The crystallinity of the dielectric layer is one of the most important factors to affect the surface structure and electrical properties of the high-k/Ge gate stack. At a low crystallization temperature it is easy for the HfO$_2$ to form a polycrystalline structure, including cubic, tetragonal, monoclinic and orthorhombic. Based on the previous investigation, it can be noted that sputtering-driven HfDyO$_x$ films are polycrystalline materials, and the crystallinity of the polymorph depends on the deposition technique and the annealing temperature. In this experiment, to obtain the effect of crystallinity on HfDyO$_x$ films as functions of sputtering powers and annealing temperature, HfDyO$_x$ thin films above 50 nm were deposited on the Ge substrate. The 50 nm far exceed the minimum critical thickness for the onset of crystallization.[14]

Fig. 1 shows the XRD pattern of the HfDyO$_x$ dielectric films as functions of the sputtering power and annealing temperature by matching with Dy$_2$Hf$_2$O$_7$ (JCPDS card no. 24-0360) and HfO$_2$ (JCPDS card no. 21-0904). It can be clearly noted that the diffraction peaks located at 29.6°, 34.3°, 49.4° and 58.6° correspond to the (111), (200), (220), and (311) plane of the cubic Dy$_2$Hf$_2$O$_7$, respectively. The main diffraction peaks located at 51.28° and 53.78° can be attributed to the (220) and (212) plane of HfO$_2$ with orthorhombic phases, respectively. As shown in Fig. 1, as the sputtering power of the Dy target increases from 5 to 15 W, a reduced intensity of the diffraction peaks and an increased full width at a half maximum were observed. Furthermore, as the sputtering power is increased to 15 W, it was clearly observed that all of the cubic-structured peaks
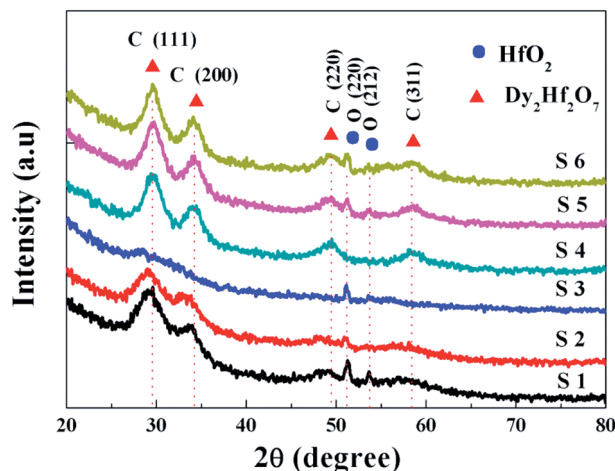

Fig. 1 XRD patterns of the HfDyO$_x$ films for samples S1–S6.

disappear. As we know, the HfDyO$_x$ gate dielectric films with a cubic phase can contribute to reducing the trap charge density, decreasing the gate leakage current and increasing the dielectric constant.[15] Therefore, it can be concluded that the appearance of the cubic phase HfDyO$_x$ will lead to a decreased dielectric constant and an increased leakage current in the S3 sample compared with the S2 sample, which is not beneficial for improving the electrical performance. The increase in disorder in the S3 sample could be due to the increased Dy doping concentration and the reduced oxygen content in the target films. Combined with the above described analysis results, 10 W-deposited HfDyO$_x$ gate dielectric thin films have been chosen and used to further explore the effect of different annealing temperatures on the interfacial chemistry and electrical characteristics of HfDyO$_x$ dielectric films. Considering the S2, S4, S5 and S6 samples, when the annealing temperature of the S2 sample was increased from 400 to 600 °C, it can be seen that the diffraction peaks shift slightly towards a higher angle, which could be due to the increased lattice constant. This can be explained by the fact that a larger ionic radius of dysprosium (91 pm) than that of hafnium (71 pm) results in the increase in the lattice constant, which will be confirmed by the following XPS measurements. In addition, with the increasing annealing temperature, the increased peaks intensities and the decreased full width at half maximum for all of the diffraction peaks have been detected, which is primarily due to the increasing interdiffusion of hafnium, dysprosium and oxygen, resulting in an enhanced order of grain arrangement.[16] Furthermore, the enhanced crystallinity will bring about a reduction in the number of trapping centers and carrier scattering events, which facilitates the formation of carrier conductive channels within the film, resulting in an increase in the gate leakage current.[17]

3.2 Interface chemical bonding states analysis

To explore the effect of the dielectric depositional conditions on the interfacial chemical bonding states, the *ex situ* XPS of the HfDyO$_x$ films were measured. All of the XPS measured data were
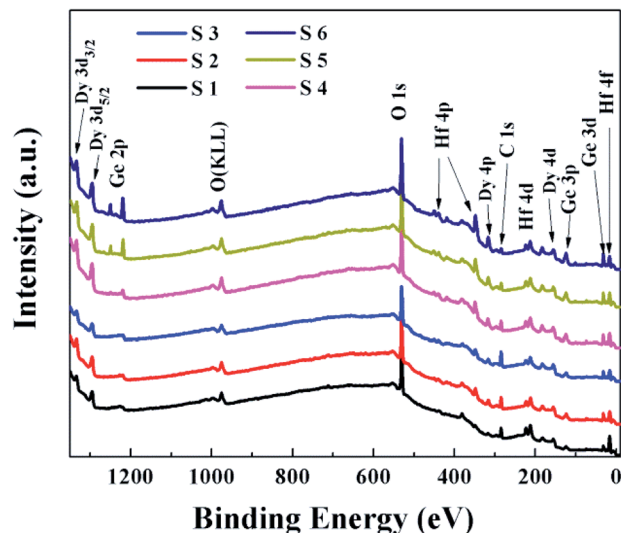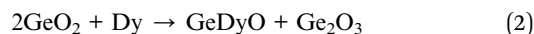
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Fig. 2 XPS survey spectra for samples S1–S6.

fitted through the Gaussian and Lorentzian functions to achieve Shirley background subtraction. Fig. 2 shows that the survey spectra of the HfDyO$_x$/Ge gate stacks, including the Ge, O, Hf, Dy and C elements, which demonstrates the successful preparation of the HfDyO$_x$ films. In addition, all of the measurement data were calibrated using the binding energy peak (284.6 eV) of C 1s. The presence of a small amount of C elements can be attributed to the contamination introduced during the measurement.

Fig. 3a and 4a show the high-resolution Ge 3d XPS spectra of all of the samples and the quantified XPS results are summarized in Table 1. Furthermore, all of the Ge 3d spectra are convoluted into three chemical components, corresponding to Ge^0, Ge–O (Ge^{1+}, Ge^{2+}, Ge^{3+} and Ge^{4+}) and germanate (Ge*), respectively. Herein, the bonding state of Ge* was found between the Ge^{3+} and

Ge^{4+} components.[18] The interfacial layer of the HfDyO$_x$/Ge gate stacks contain all of the Ge oxides (Ge^{1+}, Ge^{2+}, Ge^{3+} and Ge^{4+}). Compared to the Ge oxides (Ge^{1+} and Ge^{3+}), an increase in the content of GeO (Ge^{2+}) and GeO$_2$ (Ge^{4+}) tends to cause a sharp degradation of the device performance. Owing to the fact that Ge^{2+} and Ge^{4+} have a higher thermal instability than Ge^{1+} and Ge^{3+}. Fig. 3a displays the Ge 3d spectra for the S1, S2, and S3 samples. Compared to S1 sample, a slight reduction in the Ge sub-oxides and a slight increase in germanate were observed in the S2 sample. This indicates that the higher sputtering power of the Dy metal target could be conducive to the consumption of unstable Ge oxides on the interface. In combination with Table 1, it can be noted that the Ge^{3+} content increases and the Ge^{4+} content decreases. This could be due to the following chemical reaction:

$$2GeO_2 + Dy \rightarrow GeDyO + Ge_2O_3 \tag{2}$$

Similarly, in comparison with the S3 samples, a significant reduction in the intensity of Ge^0 and GeO$_2$ and an obvious increase in the Ge sub-oxides and germanate were observed, which could be attributed to the reason that the excessive sputtering power greatly promotes the inter-diffusion of the interface layer and the re-diffusion. Furthermore, the excessive Dy doping results in a relative decrease in the oxygen content of the interface layer, which may be conducive to the occurrence of the following reactions:

$$Ge + O \rightarrow GeO \tag{3}$$

$$Ge + GeO_2 \rightarrow 2GeO \text{ or } Ge_2O_3 \tag{4}$$

$$Hf(Dy) + GeO \rightarrow Hf(Dy)GeO \tag{5}$$

To further verify the effect of the sputtering power on the interfacial chemistry component, the high-resolution O 1s XPS
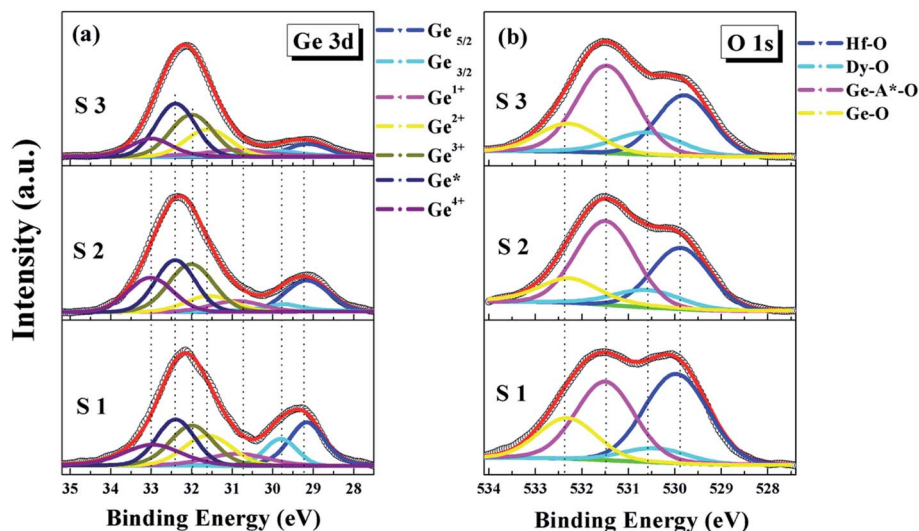

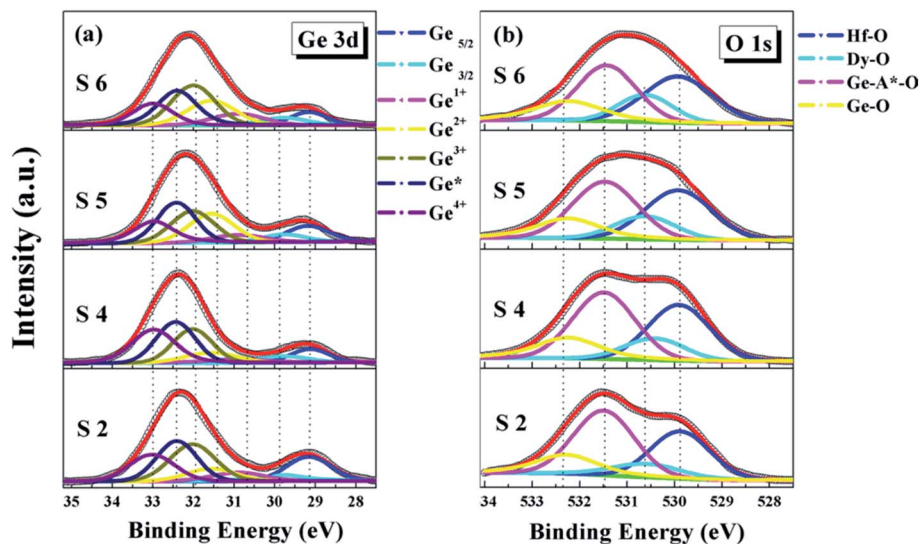Fig. 3 (a) Ge 3d and (b) O 1s XPS core-level spectra for samples S1–S3.

Fig. 4   (a) Ge 3d and (b) O 1s XPS core-level spectra for samples S2, S4, S5 and S6.

spectra for the S1–S3 samples is demonstrated in Fig. 3b and the quantified O 1s XPS results are listed in Table 2. All of the O 1s spectra have been deconvoluted into four chemical components, including Hf–O (529.88 eV), Dy–O (530.60 eV), germanate Ge–A*–O (531.49 eV) and Ge–O (532.28 eV), respectively. As demonstrated in Fig. 3b, it can be clearly observed that the intensity of Dy–O increases gradually and the intensity of Hf–O decreases with the sputtering power ranging from 5 to 15 W, indicating that the Dy concentration is increasing in the films. In agreement with the Ge 3d spectra, the increase in germanate and the reduction in the Ge–O content have also been found.

Table 1 The peak area percentages of Ge^0, Ge^{1+}, Ge^{2+}, Ge^{3+}, Ge^{4+} and germinate in the Ge 3d core-level XPS spectra for samples S1–S6

Sample	Ge^0 (%)	Ge^{1+} (%)	Ge^{2+} (%)	Ge^{3+} (%)	Ge* (%)	Ge^{4+} (%)
S1	26.8	8.0	14.5	19.1	18.3	13.3
S2	20.5	6.3	8.6	24.3	23.1	17.2
S3	17.6	5.8	16	22.1	25.3	13.2
S4	18.6	3.0	11.8	23.4	22.2	21.0
S5	15.0	6.2	16.3	25.2	22.1	15.2
S6	12.5	8.6	17.2	25.6	21.8	14.3

Table 2 The peak area percentages of all the O 1s peaks for samples S1–S6

Sample	Hf–O (%)	Dy–O (%)	Ge–A*–O (%)	Ge–O (%)
S1	38.8	5.7	37.2	18.3
S2	34.5	10.6	38.0	16.9
S3	28.0	13.3	44.3	14.4
S4	33.1	12.3	37.3	17.3
S5	32.8	13.1	37.4	16.7
S6	33.9	14.5	35.2	16.4

In order to further investigate the composition of the $HfDyO_x$ dielectric film, the high-resolution Hf 4f and Dy 3d spectra have also been obtained and are shown in Fig. 5. Owing to the spin–orbit splitting, the Hf 4f spectra are decomposed into three peaks, including a Hf-germanate and two main peaks (Hf $4f_{7/2}$ and Hf $4f_{5/2}$). The Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peak are set at 16.13 and 17.9 eV, which is in good agreement with the reported value for HfO_2.[19] Comparing S1 with the S2 and S3 samples, it is easy to determine that the composition of the Hf-germanate is gradually increasing, which is consistent with previous Ge 3d and O 1s XPS measurement results. Furthermore, the Dy 3d spectra shown in Fig. 5b consists of two peaks of Dy $3d_{5/2}$ and Dy $3d_{3/2}$, which are attributed to the spin–orbit splitting. No apparent changes in the peak position and only a slight increase in the areas of the peaks were observed, suggesting the Dy content in the $HfDyO_x$ thin films increases with the increase in sputtering power. Based on all of the XRD and XPS measurements, the conclusion can be drawn that the controlled composition and the optimized interface chemistry have been achieved in the S2 sample.

In order to further optimize the interface chemistry and improve the device performance, annealing was performed for the 10 W-driven $HfDyO_x$/Ge gate stacks from 400 to 600 °C, respectively. For the S4–S6 samples, the deposited films selected the S2 sample with a Dy sputtering power of 10 W. A comparative XPS spectra analysis of the S2, S4, S5 and S6 samples is presented in Fig. 4 and 6 and the corresponding calculated components are also displayed in Tables 1 and 2. Based on Fig. 4a, it can be noted that the intensity in Ge^0 has decreased with the increasing annealing temperature from 400 to 600 °C, implying that the higher temperature annealing facilitates the Ge re-diffusion in the high-k/Ge interface layers. In addition, comparing the S2 and S4 samples, a significant reduction in the Ge^{1+} and Ge^{3+} content and an increase in the Ge^{2+} and Ge^{4+} content have been detected, which could be due to the increased oxygen diffusion after annealing. As a result, it can be
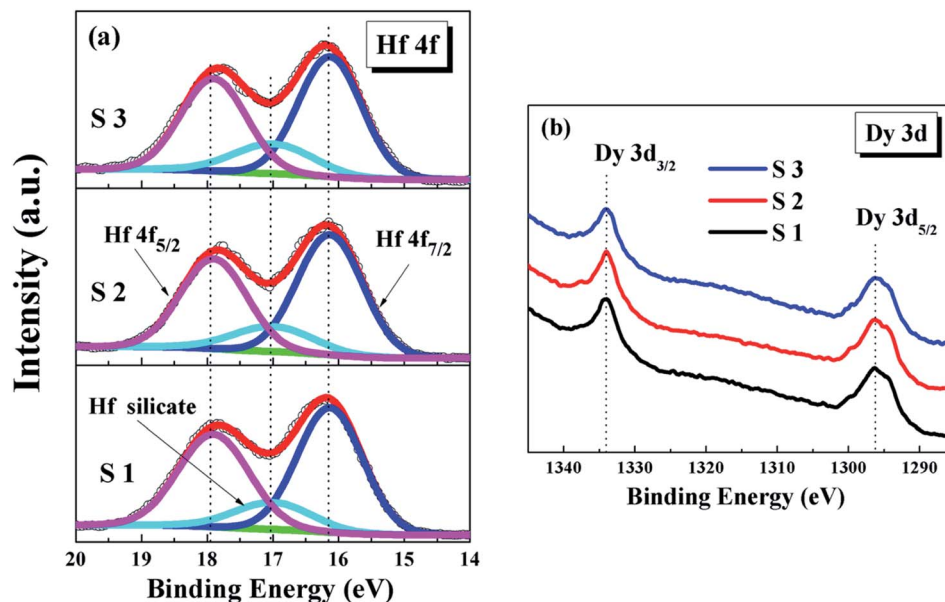
Fig. 5 (a) Hf 4f and (b) Dy 3d XPS core-level spectra for samples S1–S3.

concluded that the 400 °C-annealed S4 sample displays a degraded interface quality and inevitably leads to further degradation in the electrical performance such as an unacceptable flat band voltage and generation of hysteresis. However, as the annealing temperature continues to increase, there is an increasing trend for the Ge^{1+}, Ge^{2+} and Ge^{3+} content and a decreasing trend for the Ge^{4+} content, indicating that higher temperature annealing favors an increase in the

interface stability. In combination with Table 1, it can be further observed that the germanate continues to decrease with the increasing annealing temperature. This could be due to the increased packing density of the dielectric films with the increase in the annealing temperature, which hinders inter-diffusion and Ge re-diffusion to some extent. Finally, there is a continuous slight increment in the total amount of Hf–O and Dy–O content listed in Table 1, which could be due to the fact
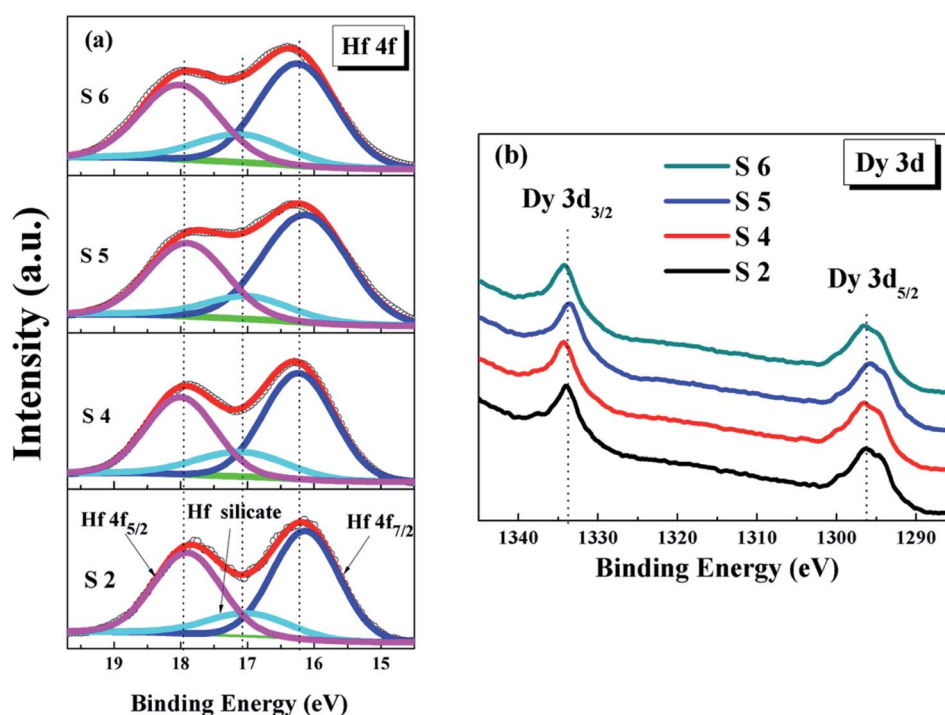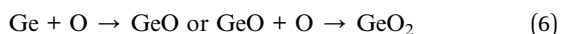

Fig. 6 (a) Hf 4f and (b) Dy 3d XPS core-level spectra for samples S2, S4, S5 and S6.

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that the higher temperature annealing accelerates the oxygen diffusion in the HfDyO$_x$ films. In addition, the annealing temperature dependent O 1s core-level spectra of the HfDyO$_x$/Ge gate stacks were also investigated, as demonstrated in Fig. 4b and Table 2. With the increase in the annealing temperature, it can be clearly observed that the content of the Hf–O peak area is decreasing, while the Dy–O peak area is increasing, which may due to different interface dipoles between the dielectric film and the Ge substrate. In the case of the S2 sample, the atomic percentage of Hf : Dy is estimated to be 76 : 24 based on the Hf–O/Dy–O peak-area ratio, which is equivalent to the mole fraction of $(HfO_2)_{0.76}(Dy_2O_3)_{0.24}$. When the annealing temperature is increased to 600 °C, the content of both tends to be in the equilibrium state. In the case of the dielectrics, the doping amount of Dy in the film is slightly increased as the annealing temperature is increased. The reason for this is that the components are sufficiently fused to each other at higher temperatures. This could lead to an increase in the density and crystallinity of the films. Of course, this fusion is limited owing to the limited Hf and Dy content, which is shown to be essentially flat when the temperature is increased to 600 °C. In addition, in combination with Table 2, it can be further observed that the germanate content continues to decrease and the Ge–O content increases slightly with the increase in the annealing temperature. This is consistent with the results of the previous XRD analysis. The corresponding Hf 4f and Dy 3d XPS spectra are shown in Fig. 6. As shown in Fig. 6a, it can be seen that the Hf-germanate decreases gradually from the S2 to the S6 sample. From Fig. 6b, a tendency to shift towards low binding energy can be observed for the Dy 3d spectra, indicating the full oxidation of the HfDyO$_x$ films after the higher-temperature-induced oxygen diffusion. To explain the evolution of the interface chemistry related to the annealing temperature, the exact mechanism is summarized and displayed in two different reaction processes in the high-k/Ge interface.

The oxide growth process, following the reaction, results in the generation of the GeO$_x$ layer.

$$Ge + O \rightarrow GeO \text{ or } GeO + O \rightarrow GeO_2 \qquad (6)$$

Another process is the oxide desorption process through the following reaction:

$$Hf(Dy) + O + Ge \rightarrow Hf(Dy)GeO \text{ or } Hf(Dy) + GeO \qquad (7)$$

The desorption of the volatile products, such as GeO and Hf(Dy)GeO, can occur at temperatures of less than 390 °C,[20] which tends to hinder the growth of the interfacial layer. Therefore, it can be inferred that with the increase in the annealing temperature the oxide desorption process is better than the oxide growth process, which explains why the annealing process does not result in an optimized interface layer.

3.3 Band alignment characterization

The transmittance and absorption spectra of the HfDyO$_x$ films deposited on quartz glass wafers were explored using UV-Vis
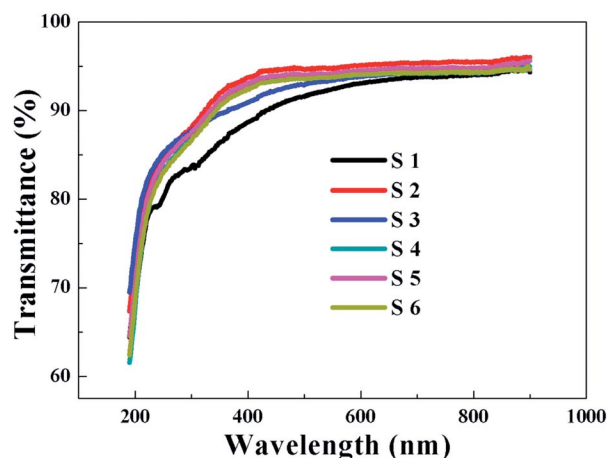

Fig. 7 Transmittance spectra of the HfDyO$_x$ films for samples S1–S6.

spectroscopy. Fig. 7 shows the transmittance spectrum of all of the HfDyO$_x$ films. It can be clearly observed that the transmittance of all of the samples is more than 90% in the visible light region, indicating that all of the samples have a high transmittance and there is great potential application in transparent semiconductor devices. In the past few years, transparent electronic products have been highly regarded, therefore HfDyO$_x$ dielectric films can be used as one of the most promising materials for next-generation flat panel displays, owing to the high transmittance and excellent electrical properties. Furthermore, it is well known that the energy band gap E_g of the dielectric film can be inferred based on the obtained absorption spectra. As we know, HfDyO$_x$ is a direct band gap insulator and the optical energy band gap (E_g) can be obtained by plotting $(\alpha h\nu)^2$ versus $(h\nu)$, as shown in Fig. 8. Comparing sample S1 with S2, it can be seen that the E_g of the HfDyO$_x$ films results in an acceptable shift ranging from 5.52 to 5.84 eV with the increase in the Dy doping content. The increase in E_g can be attributed to the fact that the appropriate increase in the Dy doping content facilitates the reduction of oxygen vacancies in the dielectric film and compensates for the oxidation charge defect of the film. Correspondingly, the defects in the dielectric film are mainly oxygen vacancies, therefore its reduction implies the increase in the energy band gap.[21] However, comparing sample S2 with S3, it has been observed that a reduction in E_g is detected when continuing to increase the Dy doping concentration, which can be attributed to the smaller E_g for Dy$_2$O$_3$ ($\sim$4.8 eV).[22] In the case of the 10 W-deposited film, with an increase in the annealing temperature, the E_g of the HfDyO$_x$ films is maintained at about 5.80 eV and no substantial shift was observed.

Considering the power consumption of the device, obtaining a small gate leakage current is the key. A sufficient injection barrier can be effective for limiting the gate leakage current, which implies that the band offsets are certainly more than 1 eV. It is generally known that the band offset is the difference between the valence band maximum (VBM) and the conduction band minimum (CBM). Therefore, the valence band maximum
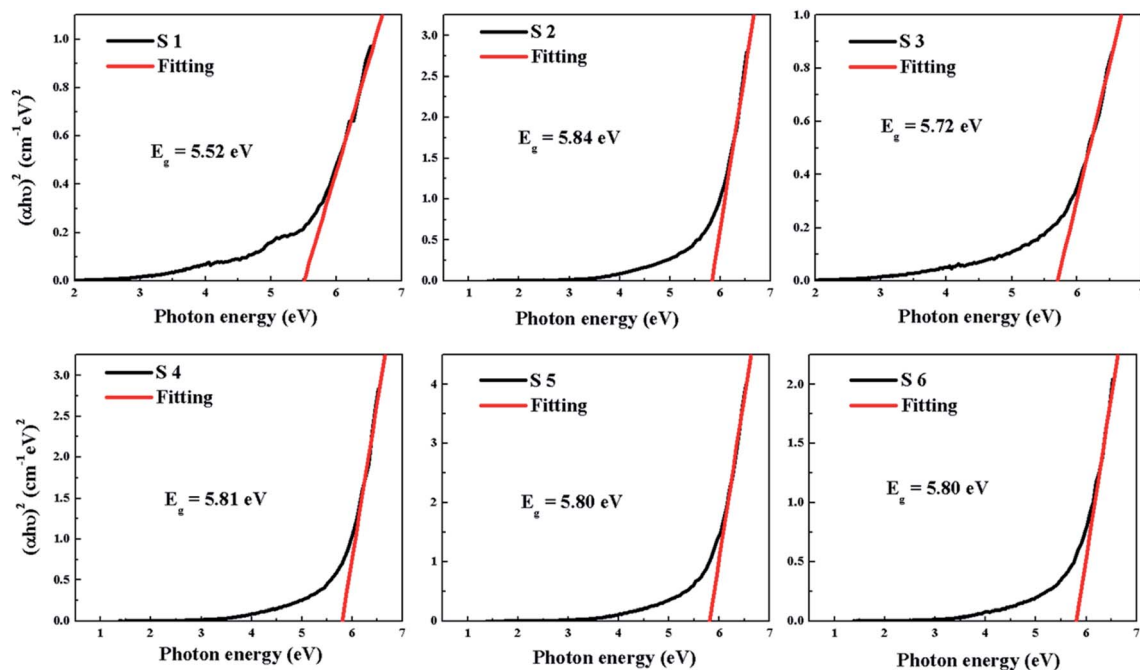
Fig. 8   The band gap of the HfDyO$_x$ films for samples S1–S6.

differentials between the HfDyO$_x$ films and the Ge substrates can be written as:

$$\Delta E_v(\text{HfDyO}_x\text{–Ge}) = E_v(\text{HfDyO}_x) - E_v(\text{Ge}) \quad (8)$$

As highlighted in Fig. 9, the valence band edge (E_v) is measured using the linear epitaxial method. It can be seen that the extrapolated valence band edge of Ge is 0.26 eV, and the valence band offsets (ΔE_v) between the HfDyO$_x$ dielectric films and the Ge substrates were calculated to be 1.82, 1.93, 1.91, 2.07, 1.91, and 2.21 eV, respectively, corresponding to the S1–S6 samples. On the basis of Kraut's method,[22] the valence-band alignment of the dielectric films can be extrapolated by

combining the ΔE_v values and the band gap of the HfDyO$_x$ films and Ge, the conduction band offset ΔE_c can be described using the following formula:

$$\Delta E_c(\text{HfDyO}_x\text{–Ge}) = E_g(\text{HfDyO}_x) - \Delta E_v(\text{HfDyO}_x\text{–Ge}) - E_g(\text{Ge}) \quad (9)$$

Here, the energy gap of the Ge substrate is 0.67 eV. As highlighted in Fig. 10, the ΔE_c values for the S1–S6 samples were determined to be 3.04, 3.25, 3.15, 3.08, 3.23 and 2.93 eV, respectively, indicating that the barrier height of all of the HfDyO$_x$/Ge gate stacks is more than 1 eV. Considering that the ΔE_c is closely related to the tunneling leakage current, the high
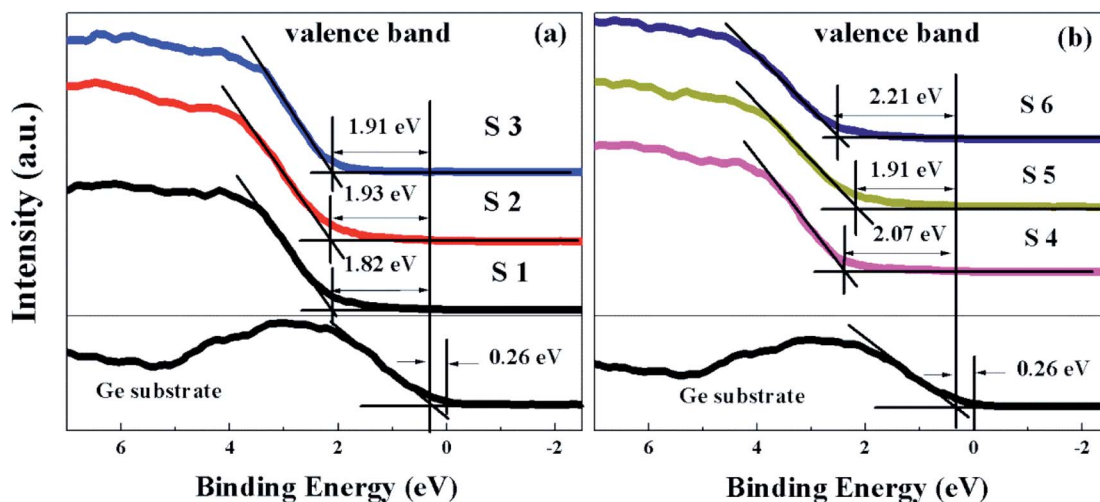

Fig. 9   The difference between the VBM for (a) samples S1–S3 and (b) samples S4–S6.
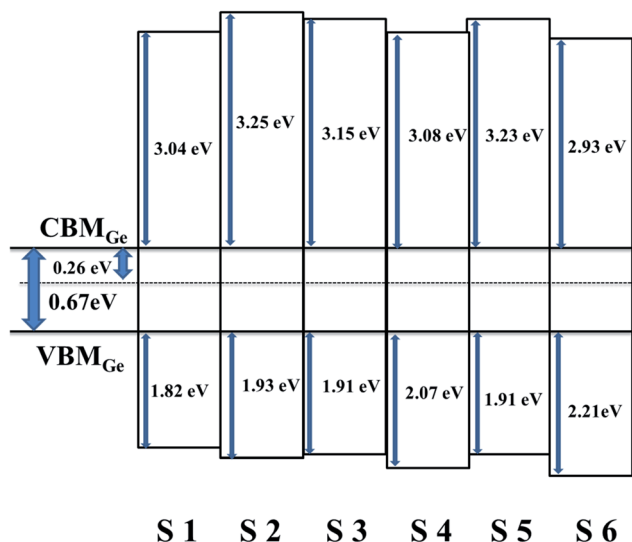
Fig. 10 Schematic band diagrams for samples S1–S6.

ΔE_c indicates a small leakage current to a certain extent.[23] Based on Fig. 10, it can be noted that the optimized ΔE_v of 3.25 eV for the S2 sample demonstrates potential application as a high-k

gate dielectric in Ge-based MOS devices. It was also found that the S2 sample has the smallest leakage current, which is discussed in the following section.

3.4 Electrical performance characterization of the Ge-MOS device

3.4.1 $C–V$ characteristics. The $C–V$ characteristic curves of all of the samples undergoing different deposition conditions and annealing temperatures are shown in Fig. 11. All of the extracted electrical performance parameters are summarized in Table 3. As exhibited in Fig. 11a, the high frequency (1 MHz) $C–V$ characteristics for the S1–S3 samples were measured using the double sweep forward and backward from reverse method with the gate voltage. It can be clearly seen that the saturation capacitance (C_{ox}) in the accumulation region does not display a linear increase with the increase in the sputtering power. The trend of increasing first and then decreasing was observed, indicating that the dielectric constant first increases and then decreases. In addition, it can also be noted that only the S2 sample displays an obvious saturation zone, depletion zone and inversion zone. This implies achievement of an effective unpinning Fermi level. This can be mainly attributed to the optimized interface quality and the reduced oxygen vacancy in
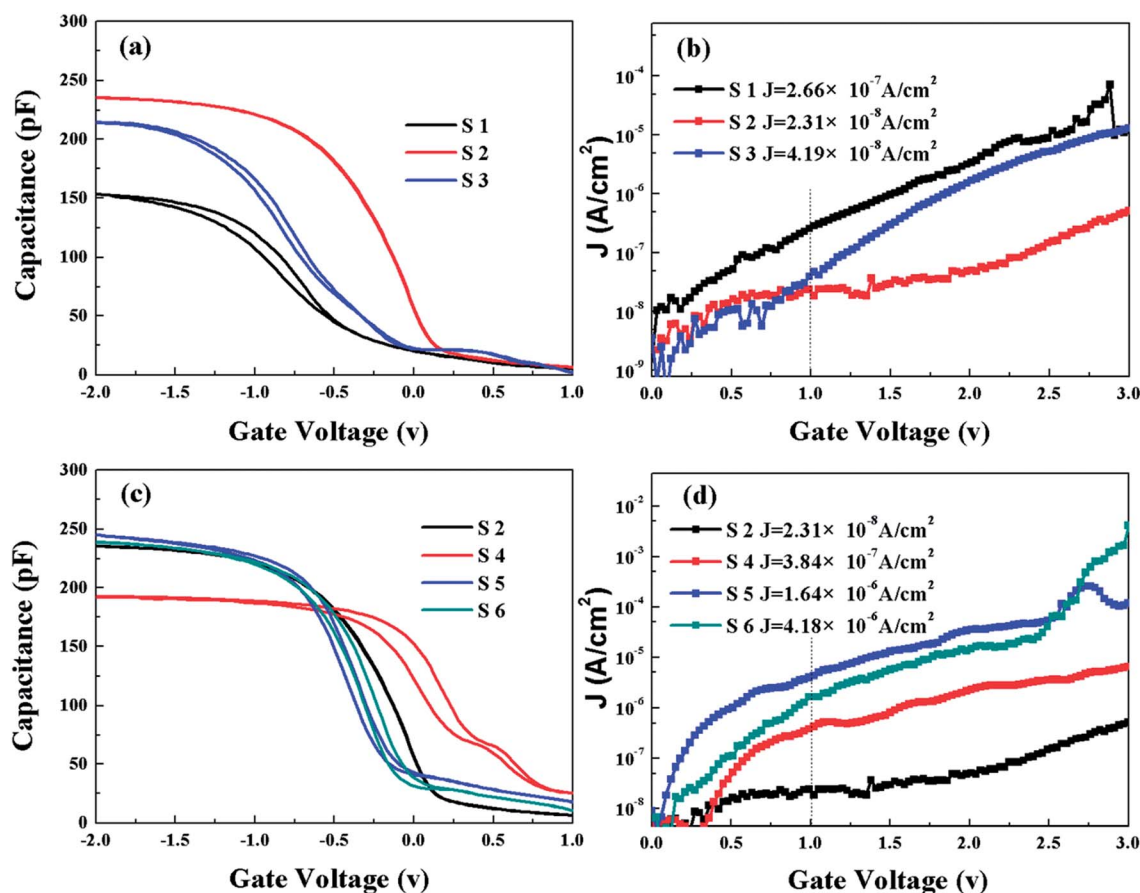

Fig. 11 (a) Capacitance–voltage ($C–V$) characteristics for samples S1–S3. (b) Leakage current density–voltage ($J–V$) characteristics for samples S1–S3. (c) Capacitance–voltage ($C–V$) characteristics for samples S2, S4, S5 and S6. (d) Leakage current density–voltage ($J–V$) characteristics for samples S2, S4, S5 and S6.

the dielectric film. However, compared to the S2 sample, the S3 sample displays a degraded electrical performance, including the negative V_{fb} (−0.6 V), an increased hysteresis value (−0.06 V), and a reduced C_{ox}, as presented in Table 1. This could be due to the excessive Dy doping which introduces the formation of the germanate and low-valence Ge ions in the interface layer. Furthermore, the generation of germanate and low-valence Ge oxides will generate a Fermi-level pinning effect,[24] resulting in the degraded electrical properties. To investigate the effect of annealing temperature on the HfDyO$_x$/Ge MOS capacitors, the C–V characteristics for S2–S6 samples are shown in Fig. 11c. Compared to the S2 sample without annealing, it can be clearly seen that the S4 sample with 400 °C annealing has a significant positive V_{fb} (0.3 V), an unacceptable hysteresis value (−0.12 V) and a minimal C_{ox}. The S5 and S6 samples, corresponding to 500 and 600 °C annealing, also have a negligible negative V_{fb} and hysteresis value. This could be attributed to the Ge re-diffusion on the interface leading to the formation of large amounts of Ge oxide. This is also clearly demonstrated in the XPS analysis described above. Furthermore, the reason for the sharp decline in the electrical properties of the S4 sample may be due to the distinct increase in unstable low-valence Ge ions (Ge^{2+} and Ge^{4+}) in the interfacial layer. Furthermore, in the case of the S2 sample, the reduced value of V_{fb} could be attributed to the introduction of a reduced positive charge and/or a captured negative charge by appropriately increasing the Dy doping. At the same time, a vanishing hysteresis could be due to a decrease in the interfacial state and the improvement of trap behavior.

In addition, combined with the V_{fb}, ΔV_{fb} and C_{ox}, the other essential electrical parameters can be extracted, including the permittivity (K), the oxide-charge density (Q_{ox}), the border trapped oxide charge density (N_{bt}) and the EOT of the HfDyO$_x$/Ge gate stacks, as listed in Table 3, respectively. As demonstrated in Table 3, the EOT value was confirmed to be 6.17, 2.46, 3.06, 3.67, 2.43 and 2.52 nm, corresponding to the S1–S6 samples, respectively. It can be easily found that the S2 sample processes a thinner EOT, indicating a larger K value caused by the optimized interfacial layer and a high quality dielectric film. After annealing, no satisfactory reduction in EOT values was observed, which indicates that annealing has no obvious suppression effect on the growth of the interfacial layer. Combined with the extracted electrical parameters, it can be noted that the S2 sample has diminished negative oxide-charge density, meaning the least amount of oxygen vacancies in the high-k dielectrics. For the S3 sample, it can be observed that the

increased Q_{ox} and N_{bt} is caused by the existing and the addition of further trapped positive oxide charges or positive charges in the interfacial layer. This can also be confirmed by the fact that the excess Dy doping can facilitate the inter-diffusion and the Ge re-diffusion.[25–27] As exhibited in Table 3, an increase in the Q_{ox} and N_{bt} has been observed for the annealed HfDyO$_x$/Ge gate stacks, indicating the degraded interface chemistry and the increased gate leakage current.

3.4.2 J–V characteristics and current conduction mechanisms. The typical J–V characteristic curves of all of the devices can be found using the HfDyO$_x$/Ge MOS capacitors, as exhibited in Fig. 11b and d. For the S1–S3 samples, when the gate voltage is set at 1 V, the gate-leakage-current–density is determined to be about 2.66×10^{-7}, 2.31×10^{-8} and 4.19×10^{-8} A cm^{-2}, respectively, as shown in Fig. 11b. It is clearly shown that the gate leakage current density has a tendency to first decrease and then increase with the increasing Dy doping concentration. This can be primarily attributed to the fact that the appropriate Dy-doping content in the HfDyO$_x$ films can reduce the dangling bonds and inhibit the trapping charge on the interfacial layer, resulting in a suppressed leakage current. As displayed in Fig. 11d, the gate-leakage-current–density is determined to be about 3.84×10^{-7}, 1.64×10^{-6} and 4.18×10^{-6} A cm^{-2} at 1 V, respectively, corresponding to 400, 500 and 600 °C-annealed samples. Compared to the S2 sample, the leakage current after annealing has increased to some extent owing to the degraded interface quality. As a result, it can be concluded that the S2 sample without thermal treatment demonstrates an optimized electrical performance, implying that the suitable rare-earth-doping HfO$_2$ possesses an optimized interfacial quality and an excellent dielectric performance.

In this work, the J–V characteristics of all devices were derived from the electrons tunneling from the semiconductor (Ge) to the metal (Al), resulting in different tunneling mechanisms by applying a positive voltage in the Al/HfDyO$_x$/Ge MOS capacitor. To study the influence of the Dy-doping and annealing on the carrier conduction mechanisms for the corresponding capacitors, some leakage current conduction mechanisms (CCMs) have been thoroughly analyzed. Fig. 11b and d depicts the J–V curves of different amounts of Dy-doping and the annealing temperature dependent samples and an increase in the tunneling current density has been observed with the increased gate voltage. This could be attributed to the transformation of the CCMs at various tunneling regions, including the Schottky emission (SE), Poole–Frenkel (PF)

Table 3 Parameters of the S1–S6 MOS capacitors extracted from the C–V and J–V curves

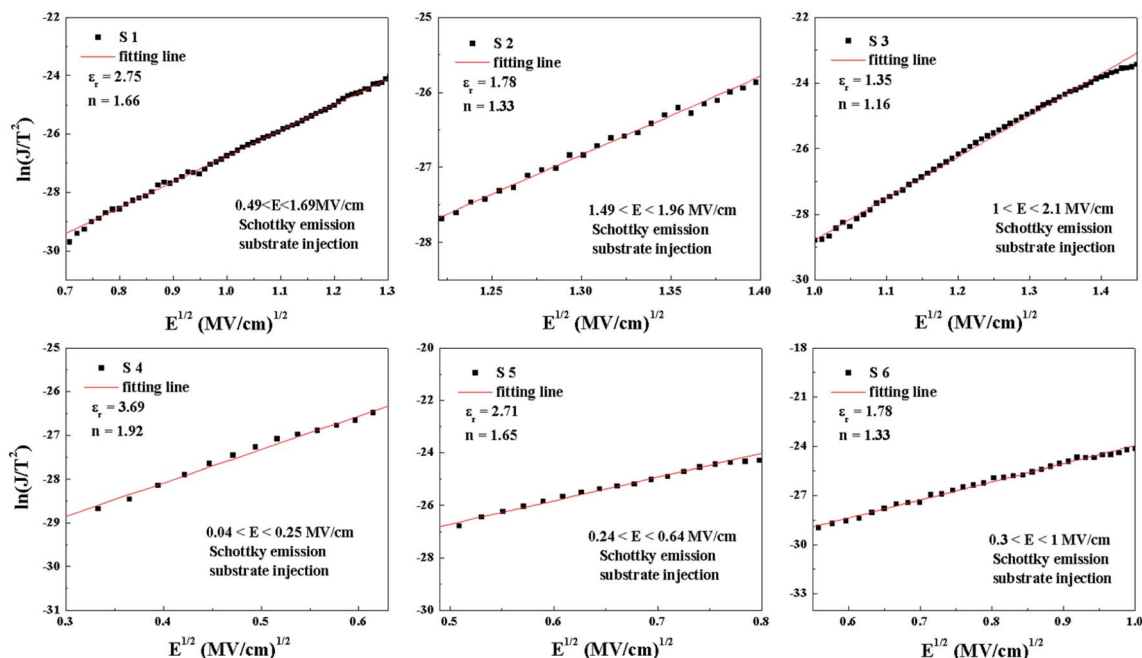| Sample	EOT (nm)	k	V_{fb} (V)	ΔV_{fb} (V)	Q_{ox} (cm^{-2})	N_{bt} (cm^{-2})	J (A cm^{-2})
S1	6.17	9.47	−0.57	−0.17	1.80×10^{12}	5.11×10^{11}	2.66×10^{-7}
S2	2.46	22.4	0.07	—	-1.87×10^{11}	—	2.31×10^{-8}
S3	3.06	19.09	−0.6	−0.06	2.68×10^{12}	2.56×10^{11}	4.19×10^{-8}
S4	3.67	15.92	0.3	−0.12	-1.02×10^{12}	4.56×10^{11}	3.84×10^{-7}
S5	2.43	21.72	−0.11	−0.09	6.83×10^{11}	4.39×10^{11}	1.64×10^{-6}
S6	2.52	20.92	−0.15	−0.07	8.60×10^{11}	3.34×10^{11}	4.18×10^{-6}

Fig. 12 The SE emission mechanism: $\ln(J/T^2)$ versus $E^{1/2}$ plots for samples S1–S6.

emission and Fowler–Nordheim (FN) tunneling.[28] In order to investigate the influence of different doping contents and annealing temperatures on the CCMs of the Al/HfDyO$_x$/Ge capacitors under substrate injection, several CCMs were systematically analyzed and evaluated.

The occurrence of the SE mechanism is caused by the thermal excitation charge, which obtains sufficient energy and then passes through the interface barrier from the gate electrode or semiconductor substrate to the dielectric. The PF emission mechanism can be attributed to the thermally excited electrons that have either been captured or emitted from the traps and have entered the conduction band of the dielectrics to form the gate leakage current. Under a high electric field, the carriers will tunnel through the insulator, that is, electrons are injected into the conduction band of the oxide through the triangular barrier, the dominant CCMs are governed by FN
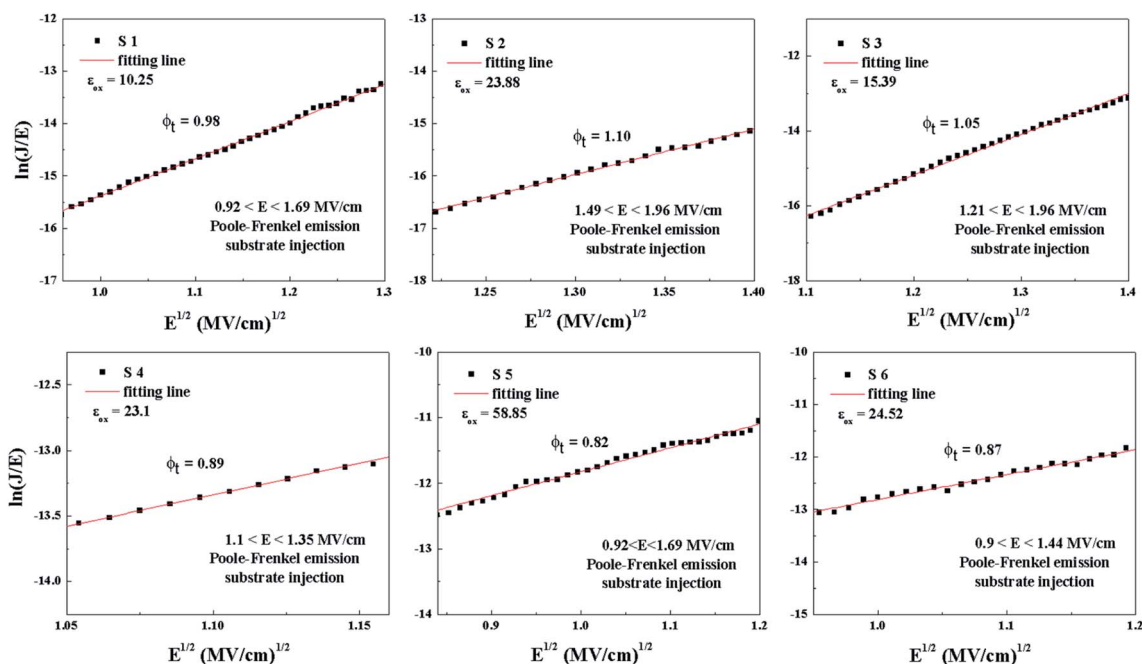

Fig. 13 The PF tunneling mechanism: $\ln(J/E)$ versus $E^{1/2}$ plots for samples S1–S6.
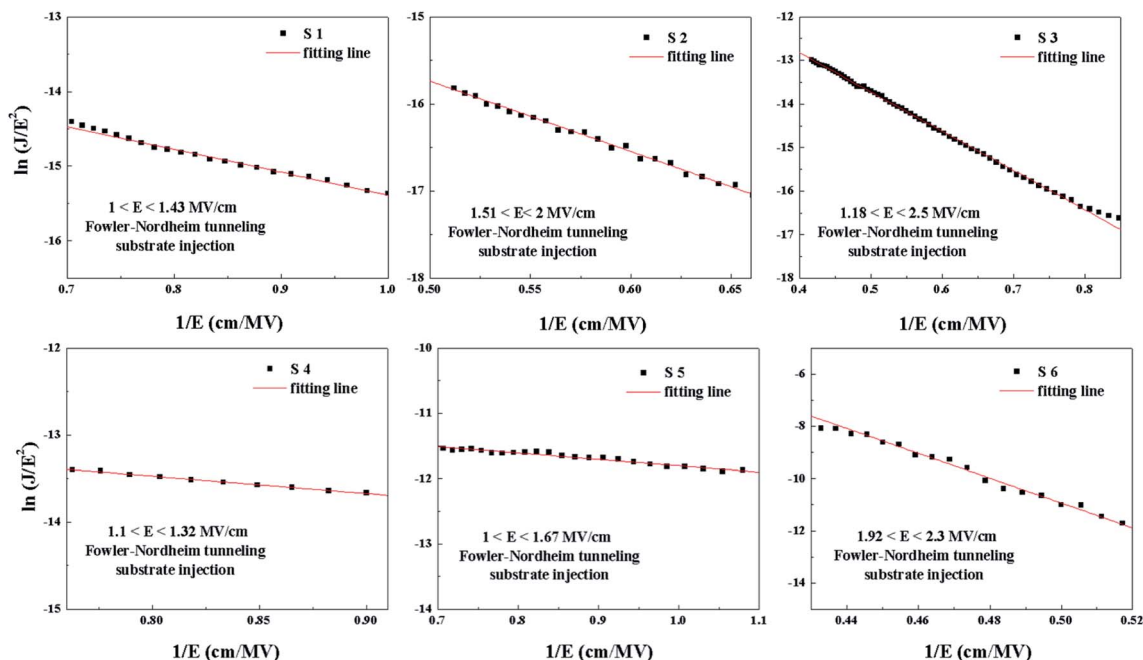
Fig. 14   The FN tunneling mechanism: $\ln(J/E^2)$ versus $1/E$ plots for samples S1–S6.

tunneling. All of the mechanisms from the SE emission, PF emission, and FN tunneling can be expressed using the following formulas:[29–31]

$$J_{SE} = A^* T^2 \exp\left[\frac{-q\left(\varphi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}\right)}{\kappa_B T}\right] \quad (10)$$

$$J_{PF} = CE \exp\left[\frac{-q\left(\varphi_t - \sqrt{qE/\pi\varepsilon_0\varepsilon_{ox}}\right)}{\kappa_B T}\right] \quad (11)$$

$$J_{FN} = \frac{q^3 E^2}{16\pi^2 \hbar \phi_{ox}} \exp\left[-\frac{4\sqrt{2m_J^* \varphi_B^{3/2}}}{3\hbar qE}\right] \quad (12)$$

In which A^* is the effective Richardson constant, κ_B and φ_B are the Boltzmann constant and the Schottky barrier height, φ_t is the trap energy level, ε_0 and ε_r are the vacuum dielectric constant and the optical dielectric constant, m_T^* is the tunneling effective mass of the gate dielectric film, and the electric field can be stated as $E = (V - V_{fb})/t_{ox}$, respectively. Fig. 12 shows the good linear behavior of $\ln(J/T^2)$ versus $E^{1/2}$ in the low electric field region, indicating that the dominant CCMs may conform with the SE emission under substrate injection. In addition, based on the linear fitting lines slope $= \frac{1}{kT}\sqrt{\frac{q^3}{4\pi\varepsilon_0\varepsilon_r}}$, the optical dielectric constant ε_r and the refractive index $n = \varepsilon_r^{1/2}$ can be extracted and are exhibited in Fig. 12.[32,33] It can be noted that the values of ε_r and n have been calculated to be (2.75, 1.66), (1.78, 1.33), (1.35, 1.16), (3.69, 1.92), (2.71, 1.65) and (1.78, 1.33), corresponding to samples S1–S6, respectively. The n values of S2, S3 and S5 deviate from the theoretical value of 2.1 and the experimental value of 1.6–1.9 in previous reports,[34,35]

which means that only the current conduction mechanism (CCM) of the S1, S4 and S6 samples satisfies the SE mechanism at a lower electric field.

The plots of $\ln(J/E^2)$ versus $E^{1/2}$ for the S1–S6 samples are demonstrated in Fig. 13. According to the linear fitting lines slope $= \frac{\sqrt{q^3/\pi\varepsilon_0\varepsilon_{ox}}}{k_B T}$, the values of the dielectric constant ε_{ox} can be extracted and are exhibited in Fig. 13. It can be easily seen that the PF emission becomes dominant as CCMs exist in the corresponding samples at different electric field. The values of ε_{ox} have been calculated to be 10.25, 23.88, 15.39, 23.1, 58.85 and 24.52, corresponding to the S1–S6 samples, respectively. As the ε_{ox} value of the S5 sample deviates from the measured value, this indicates that the S5 sample is not governed by the PF emission at $0.92 < E < 1.69$ MV cm^{-1}. The trap energy levels (φ_t) in the HfDyO$_x$ thin films are analyzed by the intercept of the red fitting linear plots: intercept $= \ln B - \frac{q\phi_t}{\kappa_B T}$ and are highlighted in Fig. 13, which is in good agreement with our previous investigation.[36]

In the FN model, $\ln(J/E^2)$ and $1/E$ conform to the linear relationship. Fig. 14 shows $\ln(J/E^2)$ versus $1/E$ under substrate injection. It can be seen that the CCMs in the higher electric region appears to follow the FN model under substrate injection. Based on the CCMs analysis, it can be inferred that the dominant CCMs evolve from SE emission, PF emission to FN tunneling with an increase in the electric field.

4.   Conclusions

In this work, the effects of different deposition and annealing conditions on the interface chemistry and electrical properties of TMA-passivated HfDyO$_x$/Ge gate stacks have been

investigated systematically. The evolution of the microstructural, interfacial chemistry, and electrical properties of sputtering-driven HfDyO$_x$ gate dielectrics have been investigated using XRD, XPS, and detailed electrical measurements. XRD analyses have confirmed that the crystallinity of the sputtering-deposited HfDyO$_x$ dielectric films depends on the sputtering power and the annealing temperature. Characterization *via* XPS has revealed that 10 W-driven dielectrics demonstrate excellent interface characteristics. This is mainly attributed to the substantial reduction of unstable Ge oxides and the sufficient substitution of Ge for oxygen vacancies in the dielectric films. However, in view of the experimental results, the annealing treatments result in interface performance degradation. Electrical measurements based on a 10 W-deposited HfDyO$_x$/Ge capacitor without annealing exhibit optimized electrical parameters, such as a larger permittivity of 22.4, a smaller flat band voltage of 0.07 V, negligible hysteresis, a lower oxide charge density of $\sim10^{11}$ cm^{-2}, and the lowest leakage current density of 2.31×10^{-8} A cm^{-2}. The doping concentration and annealing temperature dependent CCMs in HfDyO$_x$/Ge devices have been investigated and it was revealed that the dominant CCMs evolve from SE emission to PF emission to FN tunneling with an increase in the electric field. As a result, it can be concluded that 10 W-deposited HfDyO$_x$ gate dielectrics demonstrate satisfactory interface quality and improved electrical performance, indicating their potential application for use in Ge-based MOSFET devices.

Conflicts of interest

The authors declare no conflicts of interest.

Acknowledgements

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