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Research progress on solutions to the sneak path issue in memristor crossbar arrays

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Since the emergence of memristors (or memristive devices), how to integrate them into arrays has been widely investigated. After years of research, memristor crossbar arrays have been proposed and realized with potential applications in nonvolatile memory, logic and neuromorphic computing systems. Despite the promising prospects of memristor crossbar arrays, one of the main obstacles for their development is the so-called sneak-path current causing cross-talk interference between adjacent memory cells and thus may result in misinterpretation which greatly influences the operation of memristor crossbar arrays. Solving the sneak-path current issue, the power consumption of the array will immensely decrease, and the reliability and stability will simultaneously increase. In order to suppress the sneak-path current, various solutions have been provided. So far, some reviews have considered some of these solutions and established a sophisticated classification, including 1D1M, 1T1M, 1S1M (D: diode, M: memristor, T: transistor, S: selector), self-selective and self-rectifying memristors. Recently, a mass of studies have been additionally reported. This review thus attempts to provide a survey on these new findings, by highlighting the latest research progress realized for relieving the sneak-path issue. Here, we first present the concept of the sneak-path current issue and solutions proposed to solve it. Consequently, we select some typical and promising devices, and present their structures and properties in detail. Then, the latest research activities focusing on single-device structures are introduced taking into account the mechanisms underlying these devices. Finally, we summarize the properties and perspectives of these solutions.

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1. Introduction

Information transfer between the central processing unit (CPU) and the memories in von Neumann systems inevitably imposes limits on the performance and scalability of the architecture and results in large additional power consumption. This problem becomes more severe for tasks needing vast vector matrix multiplication (VMM) computing, such as real-time image recognition, data classification, and natural language processing, where state-of-the-art von Neumann systems difficultly work to match the performance of an average human brain.[1] A potential candidate hardware neuromorphic network, which mimics the operations of the human brain, has recently aroused much attention. Among numerous solutions to realize the required functions, neuromorphic networks based on memristors appear extremely promising. One of the crucial obstacles for an efficient memristor crossbar array is the so-called sneak path current problem, which decreases the reliability of the array by importing error when programing/reading the resistance state of memristors. Vast research studies are dedicated to solve this sneak-path current issue. Some general reviews[2–5] dealing with fundamental mechanisms, materials and architectures of memristors have partially addressed the sneak-path current problem and its solutions. Generally speaking, most of the early studies focused on structures, including one transistor-one memristor (1T1M), one diode-one memristor (1D1M) and one selector-one memristor (1S1M). Besides the multiple device solutions mentioned above, single-device systems, including self-selective memristors and self-rectifying memristors, have also drawn large amounts of attention due to their simple structure. These solutions are not only classified based on their *I–V* characteristics, but also depending on the composition of the devices in a memory cell. For a specific category, the devices differ from each other in terms of their intrinsic physical mechanisms. In this review, we introduce the concept of the sneak-path current issue and basics associated with its solutions. Especially, typical and promising devices are presented in detail. Finally, we summarize the properties and perspectives of these solutions.

1.1 VMM based on memristor crossbar arrays

Memristor crossbar arrays whose discrete conductance states stand for synaptic weights could accomplish efficient brain-inspired computation. Massive parallelism could be performed in an analog manner using their intrinsic physical laws. Fig. 1a shows a typical memristor crossbar array. Memristors are located at each cross point of top electrodes (rows) and bottom electrodes (columns). The total current out of every column is a summation of the current through each memristor on this column following Kirchhoff's current law, while the current through the memristor is the multiplication of input voltage and memristor conductance following Ohm's law. This column current follows the formula: $I_j = \sum_i V_i G_{ij}$. In the same way, the charges collected from each column of the crossbar are

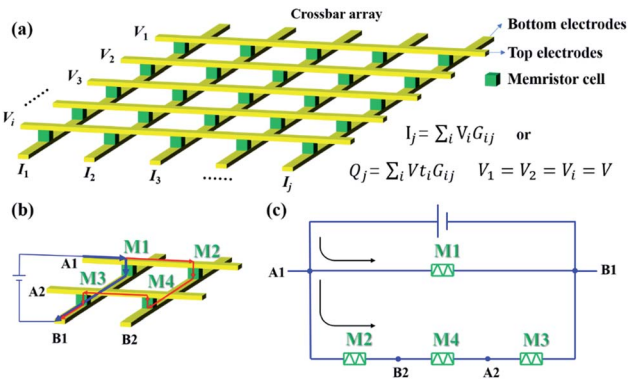

Fig. 1 Diagrams show (a) a crossbar array, (b) the sneak-path issue in the crossbar array, and (c) the equivalent circuit of the sneak-path issue.

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expressed as: $Q_j = \sum_i V t_i G_{ij}$, when input voltage pulses keep a constant amplitude of V and vary their widths (t_i). Thus, vector matrix multiplication (VMM), which is the basis for parallel computation in artificial neural networks, could be implemented by memristor crossbar arrays. In this VMM process by memristor crossbar arrays, the value of a matrix cell is encoded as the analogue memristor conductance of the crossbar array, the input vector is encoded as different voltage pulse amplitudes (widths) to the rows of the crossbar, and the VMM outputs correspond to currents (charges) collected from columns of the memristor crossbar.[6–8] For the current domain VMM method, according to Ohm's law, a strict linear current–voltage (I–V) characteristic of the memristor is required so that voltage pulse amplitudes are easily encoded as input vectors for multiplication computing. On the contrary, the charge domain VMM method tolerates nonlinear current because the voltage pulse widths are encoded as input vectors with a fixed voltage pulse amplitude. Furthermore, the fixed amplitude immensely simplifies the peripheral circuits in the charge domain VMM method. Both analog approaches finish the VMM computing in a single step, regardless of the matrix size, attracting huge interest for implementing brain-inspired computation.[9]

1.2 Sneak path current issue

During the analog VMM computing, the memristor conductances (resistances) in the crossbar array need to be duly updated. One of the crucial obstacles in the resistance programing and reading process is the so-called sneak path current problem. Fig. 1b and c show the case of sneak-path current in a 2 × 2 crossbar array. When we intend to apply a voltage between A1 and B1 lines to switch the resistance state of memristor one (M1), the blue path is the desired current path. However, current could also un-intentionally flow through the red path which is called the sneak path current. Not only does it lead to incorrect reading of the resistance state of memristors, but it also disturbs the precise resistance modulation of the array because M2, M3 and M4 memristors in series also experience the voltage. The sneak path currents also induce high energy consumption. Vast research studies are devoted to this urgent and significant task to eliminate or suppress the sneak path current issue in memristor crossbar arrays.

1.3 Programing and reading schemes in memristor crossbar arrays

The sneak path current could be effectively suppressed by designing the bias scheme for the programing and reading process. As shown in Fig. 2, the resistance of memristors sandwiched between word lines and bit lines is programed or read under two common types of write bias schemes: the $V/2$ method[10] and $V/3$ method.[11] In the $V/2$ scheme, the selected word line and selected bit line are applied full voltage (V) and 0 voltage, respectively. The unselected word lines and bit lines are applied half voltage ($V/2$). As a result, the selected memristor is under V bias, half-selected memristors are under $V/2$ bias, and unselected memristors are under no bias. As for the $V/3$ bias

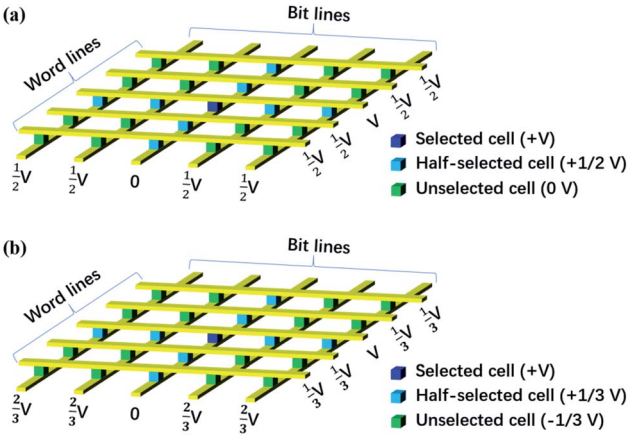

Fig. 2 Schematics of the $\frac{1}{2}V$ bias method (a) and $\frac{1}{3}V$ method (b).

scheme, the selected word line and selected bit line are applied full voltage (V) and 0 voltage, respectively. The unselected word lines are applied $V/3$, whereas the unselected bit lines are applied $2V/3$. Accordingly, the selected memristor is under V bias, half-selected memristors are under $V/3$ bias, and unselected memristors are under $-V/3$ bias. Note that more than one selected cell could be programed parallelly in the memristor crossbar array. The $V/2$ bias in the $V/2$ method and $\pm V/3$ bias in the $V/3$ method inevitably contribute to energy consumption. The nonlinear I–V curves give a lower energy consumption than the linear one. For a specific array size and nonlinearity, the $V/3$ method is more energy efficient for small arrays; as the array size increases and the number of selected cells decreases, the $V/2$ method achieves greater energy efficiency.[12]

These bias schemes are effective ways to update and obtain states of the memristor crossbar array. However, for realization of efficient states update in situation where voltage pulses is messaged and complicated, such as spike neural network, and for a lower energy consumption, device level to suppress sneak path currents issue for precise resistance modulation of the array is necessary.

2. Solutions to the sneak path current issue

2.1 1T1M

The 1T1M cell structure is an effective solution to the sneak-path current issue. The 1T1M crossbar array is called the active crossbar array, where the series transistor plays the role of a switch. When the series field effect transistor is in the ON-state, it behaves much like a wire with high conductance. Consequently, the voltage can entirely drop across the memristor no matter the polarity of the biased voltage, which facilitates the state switching of the memristor. When the series field effect transistor is in the OFF-state, nearly no current flows through the cell and no voltage drops across the memristor. *Via* deliberately manipulating the ON–OFF state of transistors, precise selection of a designated memory cell can be realized.

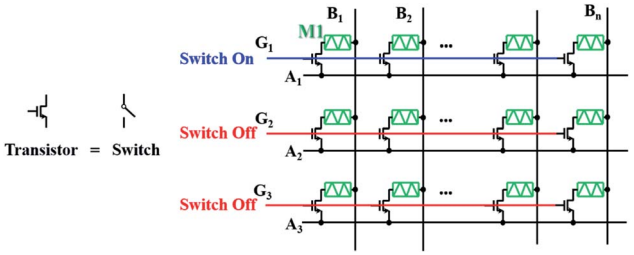

Fig. 3 Schematic diagram of a 1T1M crossbar.

A typical schematic diagram of the 1T1M crossbar array is shown in Fig. 3. Here the line which activates memristors is called the bit line (B), and the gate line (G) controls the ON/OFF state of the cell. Bit-lines and gate-lines are usually perpendicular to each other. For example, when one control operation from A_1 and B_1 is implemented on M1 (gate-line 1 in the ON state), the other adjacent gate-lines are set to the OFF state to avoid crosstalk. Thus, the sneak path currents can be efficiently suppressed to enable accurate resistance programming and reading in the 1T1M crossbar array. The 1T1M has a cell area of $8F^2$, which is relatively large and limits the scaling of the array and integration density. To minimize as much as possible the scaling issue, a high channel conductance of transistors is preferred. On the other hand, CMOS transistors take advantage of their sophisticated fabrication techniques and scalability, whereby large 1T1M crossbar arrays could be easily achieved. Furthermore, by offering compliance currents, the gate lines in the 1T1M crossbar array assist in obtaining the linear and symmetric conductance increase and decrease with minimal cycle-to-cycle and device-to-device variations.[13] This is favored by the time-efficient current domain VMM computing.

Therefore, 1T1M crossbar arrays have already been widely studied.[6,13–24] Wu's group fabricated a 128 × 8 1T1M crossbar array of TiN/TaO_x/$HfAlyO_x$/TiN devices.[25] Using this 1024-cell array with parallel online training, a grey-scale face classification is demonstrated for the first time experimentally. The energy consumption is 1000 times less than that of the Intel Xeon Phi processor with off-chip memory and the accuracy on test sets is close to the result using a central processing unit. Xia and Yang's groups built up a 128 × 64 Ta/HfO_2 1T1M crossbar array and used it for efficient analogue signal and image processing and other machine learning tasks.[6,13,26,27] Based on the 1T1M crossbar array, they further demonstrated *in situ* training of feed-forward and recurrent convolutional memristor networks.[28]

Very recently, Wu's group demonstrated reliable and uniform analogue switching behaviors in the 2048 1T1M crossbar array of TiN/TaO_x/HfO_x/TiN devices.[29] By integrating eight 2048-cell 1T1M crossbar arrays on a printed circuit board (PCB) and a field-programmable gate array evaluation board (ZC706, Xilinx), they successfully built a five-layer memristor-based CNN and performed MNIST image recognition with a high accuracy of more than 96 per cent. They demonstrated that the energy efficiency in memristor-based CNN neuromorphic systems is two orders of magnitude greater than that of the state-of-the-art graphics-processing units.[29] Despite the slightly overshadowed scaling issue, the 1T1M crossbar arrays show great potential for neuromorphic application.

2.2 1D1M

The 1D1M crossbar array with a unit cell area of $4F^2$ is a promising architecture for high-density memory due to its excellent scalability. As shown in Fig. 4a, the 1D1M cell structure is composed of two elements: one diode and one memristor, and these two devices are connected in series. The current of a forward-biased diode is relatively large while the current is blocked when the diode is reverse-biased. By connecting a unipolar resistive switching device to this diode in series, this double-device structure displays a resistive switching behavior with a rectifying property.[30] Consequently, this rectifying property can be used to inhibit sneak current, as implied by the red dashed line in Fig. 4a and b. In addition, the series diode also acts as an external load resistor to suppress the overflow current during the resistance transition, which significantly improves the cycle-to-cycle distribution of the integrated cells.[30,31]

Some requirements must be satisfied for a series diode in the passive crossbar array. A high rectification ratio, defined as the ratio between forward and reverse currents, is the most crucial one. A higher rectification ratio eliminates more sneak-path currents and allows larger passive crossbar arrays. Another performance concerned is the forward current density. Since the forward current should be high enough to switch the series memristor, a higher forward current density allows a smaller

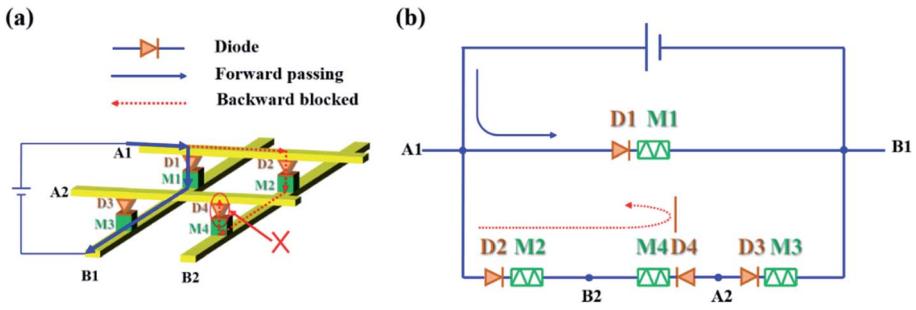

Fig. 4 (a) A diagram and (b) equivalent circuit of a 2 × 2 crossbar array containing memory elements and diodes in series, in which the sneak path current is inhibited.

Table 1 Partially reported 1D1M structure

D	M	Current density[a]	Fabrication temperature	Ratio[b]	Endurance	Retention	Current array size	Ref.
Pt/TiO_2/Ti Schottky	Ti/SiO_x/Pt unipolar	10^2 A cm^{-2} (2 V)	≤200 °C	10^5 (±2 V)	300 (1D1M)	$>10^5$ s	8 × 8	32
Pt/TiO_2/Ti Schottky	Pt/TiO_2/Pt unipolar	$>10^4$ A cm^{-2} (2 V)	Near room temperature	10^9 (±2 V)	10^8 (D), 500 (1D1M)	10^4 s	4 × 4 × 2 (integrated 2 layer)	33
Pt/$InZnO_x$/CuO_x/Pt p–n junction	Pt/Ti-doped NiO/Pt unipolar	10^4 A cm^{-2} (2 V)	Room temperature	10^2 (±1 V)	100 (1D1M)	—	8 × 8	30
Pt/n-type Si Schottky	Pt/Ta_2O_5/Pt unipolar	$>10^6$ A cm^{-2} (1 V)	—	10^2 (±1 V)	10^3 (1D1M)	10^4 s	—	31
Pt/a-IGZO/Cu Schottky	Pt/HfO_2/Cu bipolar	10^2 A cm^{-2} (1 V)	Room temperature	10^3 (±0.5 V)	10^8 (D)	—	—	34
Ni/TiO_2/Ti Schottky	Al/STN/Pt bipolar	10^4 A cm^{-2} (1 V)	100 °C	10^3 (±0.5 V)	—	$>10^5$ s	—	35

[a] The forward current density of the series diode. [b] The ratio is defined as the ratio between forward and reverse currents of the lowest resistance state of the 1D1M unit.

cell area of the diode and a higher integration density. Other factors such as endurance, a low temperature fabrication process and compatibility with CMOS technology are also considered when approaching their commercial application. Some recent advances of 1D1M structures, concerning parameters mentioned above, are summarized in Table 1.

Yoon *et al.* reported a 1D1M crossbar memory array fabricated by physical vapor deposition methods at low temperature.[32] The unit consists of a nanoporous SiO_x film and a TiO_2 oxide-based diode and shows uniform and stable memory performances even under mechanical deformation, while the endurance of 300 should be optimized. The low temperature fabrication process and flexible properties allow compatibility with not only conventional semiconductor processes, but also flexible memory applications. Using near-room-temperature physical vapor deposition methods, Kyung *et al.* fabricated 1D1M units with a TiO_2-based Schottky diode and unipolar resistance switching TiO_2.[33] Based on these outstanding units whose rectification ratio is as high as 1.4×10^9, they demonstrated a double-layer-stacked ($4 \times 4 \times 2$) 1D1M crossbar array, confirming the possible route for the multi-stacked memory structure.[33]

It is noted that the 1D1M method prefers unipolar memristors where the set and reset processes occur at the same voltage polarity, because the voltage mainly drops across the diode and hardly switches the resistance back in the bipolar one when the cell is reversely biased. Since the bipolar-type memory is more appropriate in most neural networks where resistance states are altered by simple voltage pulses with different voltage polarities, diodes satisfying bipolar memristors are required. This makes it necessary for the diode to meet at least two necessary requirements: (1) high forward current density and low reverse current density as in a regular diode to guarantee forward resistive switching and to suppress the sneak path currents. (2) Enough reverse current density at the voltage larger than the breakdown voltage (so called Zener voltage) to guarantee reverse resistive switching. When a forward voltage is applied to update resistance state of the intended memristor, only the middle cell in the sneak paths (D4M4 in Fig. 4) sustains an ultrahigh resistance state due to the reversed series diode and accommodates most of the applied voltage. To eliminate unintended programming, the amplitude of the reverse threshold voltage should be higher than the forward threshold voltage in the integrated one diode and one bipolar memristor unit. Despite some advances of bipolar 1D1M devices,[34,35] the array application of 1D1M for bipolar memristors is still in its early stage.

2.3 1S1M

In a 1S1M array, a two-terminal selector device is connected to each memristor cell in series keeping the unit cell area of $4F^2$. The selector is actually a bidirectional highly nonlinear resistor. The selector and memristor can be stacked on top of each other, giving a higher density potential than the 1T1M scheme. As sketched in Fig. 5a and b, the *I–V* curve of the 1S1M structure shows very low current at half read (also program) voltage (high

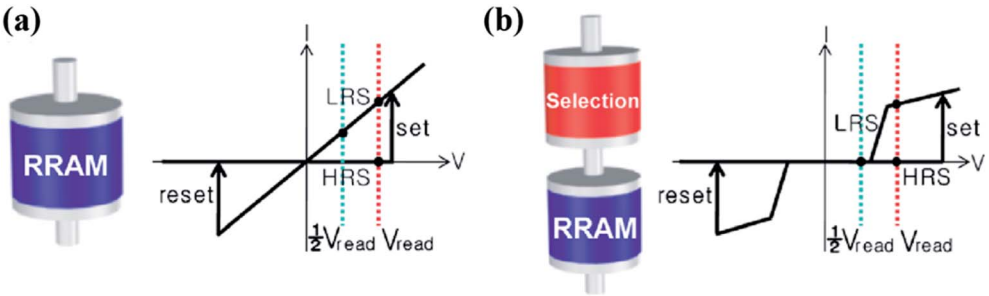

Fig. 5 (a) Schematic diagram of the bipolar Resistive-RAM (RRAM) without a selection device (left), and the corresponding *I*–*V* model (right). (b) Schematic diagram of the bipolar RRAM with a selection device (left), and the corresponding *I*–*V* model (right) (reproduced from ref. 36, Copyright 2011, with permission of AIP Publishing).

resistance), while the resistive switching of the memristor occurs in the high voltage region.[36] The nonlinearity k of an *I*–*V* curve is defined as $k = I(V_{op})/I(V_{op}/2)$, where V_{op} is the operation voltage applied to the selected cell for reading or writing. As discussed in Part 1.3, during the programing/reading process in the 1S1M crossbar array, full voltage is only applied to selected cells, while half voltage is biased on these half-selected cells for the $V/2$ method and $|V/3|$ is biased on half-selected and unselected cells for the $V/3$ method. Thus, the nonlinear property can effectively prevent the sneak effect in the 1S1M crossbar array. Consequently, the nonlinear *I*–*V* curve of the 1S1M unit can use the charge domain method when performing the VMM computing.

Similar to the requirements of a series diode in Part 2.2, high nonlinearity and large current density in the high voltage region benefit a large and dense crossbar array. The large current at high voltage is essential for the resistive switching of the series memristor, and a bigger nonlinearity of the *I*–*V* curve also results in higher resistance within the low voltage region, which benefits low energy consumption. Other factors such as endurance, a low temperature fabrication process and compatibility with CMOS technology are also considered when approaching their commercial application. Especially, the endurance of a selector should be significantly greater than that of its series memristor because the selector is turned on for every programming and reading event. The tunneling barrier[37,38] and n–p–n[39] or p–n–p[40] junctions are commonly used in selectors. Ovonic threshold switching (OTS) behavior could also be used to achieve high nonlinearity for oxide capacitor devices; this requires the threshold resistive switching to occur transiently (less than 10 ns).[41] Some recent advances of the 1S1M structure, concerning parameters mentioned above, are summarized in Table 2. The following are carefully picked examples, categorized by their intrinsic physical mechanisms, in which their merits, drawbacks and opportunities are discussed.

2.3.1 Tunneling barrier selectors. Tunneling barrier structures have been widely utilized in Resistive-RAM (ReRAM or RRAM) selectors due to their intrinsic nonlinear *I*–*V* curves. Compared with single-layer barrier structures, trilayer tunneling barriers are more attractive because of the enhanced nonlinearity.[37,38] In Choi's work,[38] a selector with a structure of $Pt/TaN_{1+x}/Ta_2O_5/TaN_{1+x}/Pt$ has been proposed, where 3 nm TaN_{1+x}/2.5 nm Ta_2O_5/3 nm TaN_{1+x} serves as a trilayer tunneling

Table 2 Partially reported 1S1M structure

S	M	Current density[a]	Fabrication temperature	Nonlinearity[b]	Endurance of S	Dynamics[c]	Ref.
$Pt/TaN_{1+x}/Ta_2O_5/TaN_{1+x}/Pt$, tunneling barrier	$Pt/TaN_{1+x}/Pt$	10^3 A cm^{-2}	400 °C	10^4	10^8	—	38
$TaN/ITO/Co_3O_4/ITO/TaN$, n–p–n	$TaN/Al_2O_3/ZrO_2/Al_2O_3/TaN$	6.5 A cm^{-2}	Room temperature	10^3	10^7	—	39
$Pt/CoO_x/IGZO/CoO_x/Pt$, p–n–p	$Pt/TaO_x/TiN$	0.1 A cm^{-2}	—	10^4	10^4	—	40
$Ag/HfO_x/Ag$, OTS	$Pd/Ta_2O_5/TaO_x/Pd$	>10^4 A cm^{-2}	200 °C	10^{10}	10^8	75 ns, 300 ns	42
$TiN/Nb_{1-x}O_2/Pt$, OTS	$Cu/HfO_2/Pt$	>10^6 A cm^{-2}	—	10^2	10^{12}	<10 ns, <10 ns	41
W/SiTe/W, OTS	—	10^7 A cm^{-2}	Room temperature	10^5	10^8	2 ns, 7 ns	43
TiN/SiTe/Ag, OTS	—	>10^2 A cm^{-2}	300 °C	10^4	10^5	30 ns, 5.1 μs	44
TiN/GeSe/TiN, OTS	—	10^3 A cm^{-2}	300 °C	10^7	10^5	100 ns, 300 ns	45
Ti/CuO-NW/Ti, OTS	—	—	—	10^4	10^5	—	46

[a] The highest current density of the series selector. [b] The nonlinearity is obtained from the selector. For the ovonic threshold switching (OTS) selectors, this value is obtained as selectivity (R_{high}/R_{low}, ratio between resistances before and after threshold switching). [c] The switch speed for the transition (up) and delay (down) in these OTS selectors.

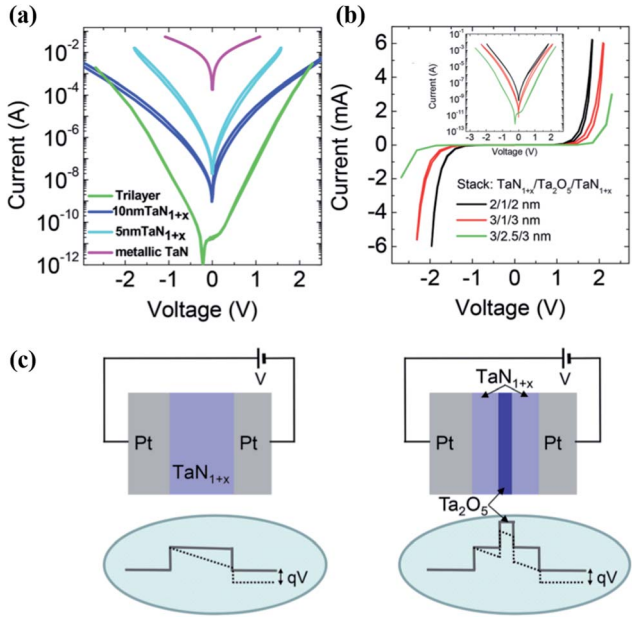

Fig. 6 (a) *I–V* curves through metallic TaN and single TaN_{1+x} layer barriers with two different thicknesses (5 and 10 nm) and trilayer (3 nm TaN_{1+x}/2.5 nm Ta_2O_5/3 nm TaN_{1+x}) barriers. (b) *I–V* curves through three trilayer devices with the thickness of each layer being 2/1/2, 3/1/3, and 3/2.5/3 nm. The inset is in the semilog plot. (c) Schematic band diagrams of the single and trilayer barrier structures (reproduced from ref. 38, Copyright 2015, with permission of John Wiley & Sons, Inc).

barrier. The *I–V* characteristics are shown in Fig. 6a and b and the energy band diagrams are shown in Fig. 6c. The high voltage decreases the height and effective width of the trilayer tunneling barrier simultaneously, resulting in a significantly larger nonlinearity of $>10^4$ than that in a single tunneling barrier structure. This trilayer tunneling barrier selector is capable of a high endurance of $>10^8$ cycles.

Despite the merits of trilayer tunneling barriers, such as large nonlinearity and high endurance, tunnel selectors are promising due to the following reasons: the nonlinearity results from the intrinsic physical mechanisms, which are well understood and reproduced by accurate mathematical modeling. The intrinsic abrupt high currents don't need assistance of Joule heating, and are independent of temperature. These characteristics benefit low energy consumption and wide available temperature windows. Furthermore, tunnel selectors possess the advantages of intrinsic speed and reproducibility of their *I–V* curves. One of the challenges is that fabricating high-quality ultrathin films usually needs a high temperature process.[47,48] High-quality tunnel selectors processed at room temperature, such as organic tunneling junctions,[49] are under explored.

2.3.2 OTS selectors. The OTS is known to be fast, instantaneous, abrupt, volatile, repeatable and field-dependent. Thus, OTS devices are extensively used as selectors.[41–46] Midya *et al.* reported an OTS selector based on metal filament formation and the rupture mechanism.[42] The structure is composed of Pd/Ag/HfO_x/Ag/Pd (Fig. 7a). Fig. 7c shows the nonlinear *I–V* curves and the illuminated mechanism is shown in Fig. 7b; when a positively biased voltage is applied, the formation of the Ag filament decreases the resistance of the selector at the threshold voltage, leading to an abrupt increase of current. When the voltage sweeps back, the filament rupture event occurs due to the diffusion potential, the Nernst potential and Gibbs–Thomson effect. Because of the symmetry of this structure, it exhibits similar electrical properties at reverse-biased voltage (Fig. 7c). The ovonic threshold switching based on filament formation and the rupture mechanism always give ultrahigh nonlinearity, for example, 10^{10} in this Pd/Ag/HfO_x/Ag/Pd case. Combining this selector with a bipolar resistive device such as Pd/TaO_x/Ta_2O_5/Pd (Fig. 7d), the memory cell exhibits nonlinear resistive switching with a slightly degraded nonlinearity (Fig. 7e). This filament-based selector could exhibit an endurance of up to 10^8 cycles. The transition time is about 75 ns for filament formation and 250 ns for filament rupture. The outstanding nonlinearity and endurance behaviors in the Pd/Ag/HfO_x/Ag/Pd selector are appealing, while the mediocre transition time which may degrade the speed of series memristors needs to be optimized.

To improve the transition time, Lv and Liu's groups designed an ovonic threshold switching selector governed by the pure electron transition effect.[41] In their $Nb_{1-x}O_2$ based selector, the threshold switching is triggered by local thermal runaway which reduces the energy barrier. There are no ions moving or phase transitions in the threshold switching process. Consequently, the speed of less than 10 ns and an ultra-high endurance of up to 10^{12} cycles are obtained, while the nonlinearity is 500, in this pure electron selector. Other pure electron OTS selectors based on SiTe with a transition of 2 ns and a delay of 7 ns are reported.[43] Corresponding endurance and nonlinearity are 10^8 cycles and 10^5, respectively. The OTS selectors based on the pure electron mechanism provide a promising prospect for large and dense crossbar arrays.

2.3.3 p-/n-Type semiconductor-based selectors. p-/n-Type oxide semiconductors are plausible to be designed as selectors with good uniformity performance because of the mature controllability of lattice mismatch and doping profiles of p–n hetero-junctions. Bae *et al.* reported a selector entirely based on oxide semiconductor p–n–p junctions with a structure of p-CoO_x/n-IGZO/p-CoO_x (ref. 40) (Fig. 8a). Unlike conventional bipolar transistors connecting all three terminals (*i.e.* emitter, base and collector electrodes), this device is open-based and is used as a two-terminal selector. Fig. 8d shows the schematic band diagram of the device. At zero or low bias voltage, the whole device is analogous to two anti-connected diodes, which leads to a suppressed current density. However, when a larger voltage (>threshold voltage) is applied, the top of the valence band of the collector exceeds the bottom of the conduction band of the base, enabling a large number of electrons to inject into the base from the collector. Therefore, the current rapidly increases at this point resulting in a nonlinearity of 10^4. Because of the symmetry of the device, the *I–V* curves (Fig. 8b) are highly symmetric at both voltage polarities. Finally, as shown by the *I–V* curves in Fig. 8c, by combining this selector, the Pt/TaO_x/TiN structure presents excellent nonlinear resistive switching behavior.

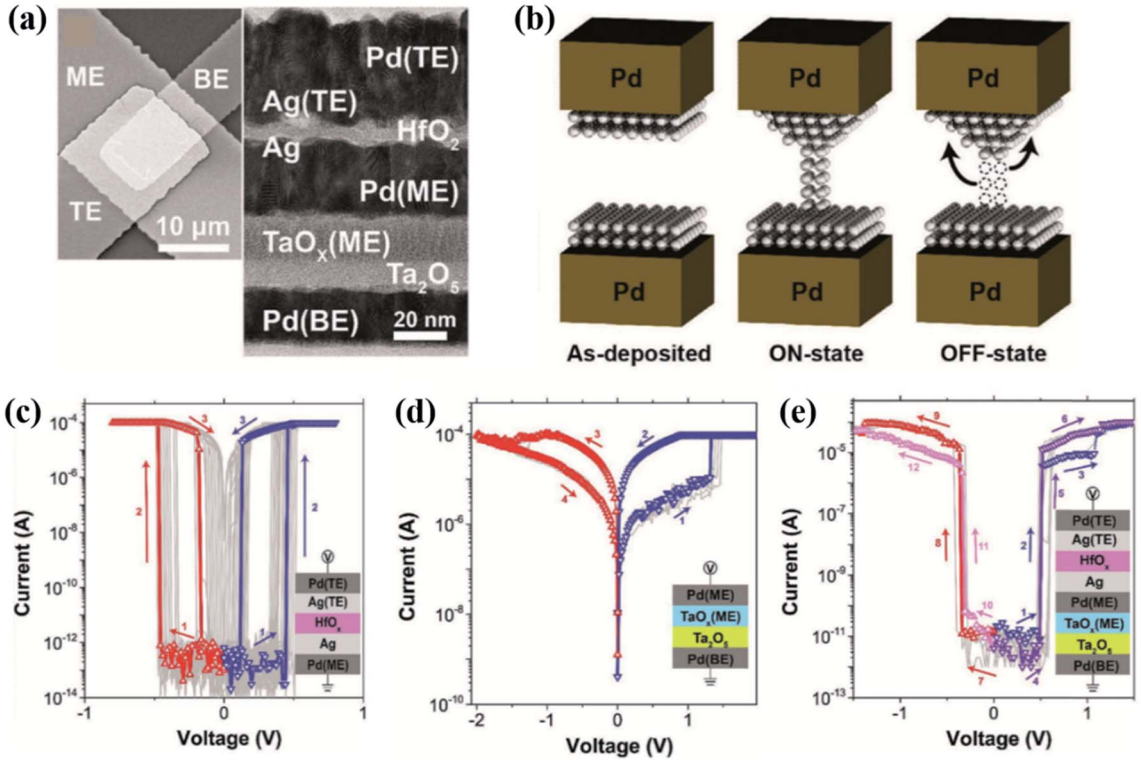

Fig. 7 (a) Structure of the integrated 1S-1R device consisting of a Pd/Ta_2O_5/TaO_x/Pd memristor and a Pd/Ag/HfO_x/Ag/Pd selector highlighted by SEM and cross-sectional TEM techniques. (b) Schematic diagram of the filament during the threshold switching process. (c) Repeatable bidirectional threshold switching of the individual Pd/Ag/HfO_x/Ag/Pd selector. (d) Repeatable bipolar resistive switching of the individual Pd/Ta_2O_5/TaO_x/Pd memristor. (e) Repeatable nonlinear resistive switching of integration of the selector and memristor (reproduced from ref. 42, Copyright 2017, with permission of John Wiley & Sons, Inc).

Similarly, a highly nonlinear n–p–n selector is also reported.[39] One resistor device connecting the proposed n–p–n selector demonstrates a high nonlinearity of 10^3, excellent endurance of 10^7 cycles, fast switching speed (60 ns), and stable retention (10^4 s) at 100 °C.[39] The successful operation of the p–n–p or n–p–n selector and one memristor with the 1S1R architecture contributes a new route for advancing crossbar arrays. One of the challenges is the low current density in the p–n–p and n–p–n structures, which hinders a high-density crossbar array.

3. Single-device memory cell structure

A single memristor device with either self-nonlinear or self-rectifying *I–V* characteristics could suppress the sneak path currents without other assistant cells in a crossbar array, and is a great improvement to simplify the memory cell, which reduces the cost, and benefits highly integrated crossbar arrays. By listing necessary parameters as in 1D1T and 1S1T structures, recent advances of these single-device memristors used in crossbar arrays are summarized in Table 3. The following is a careful introduction separated as self-selective memristors and self-rectifying memristors.

3.1 Self-selective memristors

Self-selective memristors exhibit self-nonlinear *I–V* characteristics as the overall feature of 1S1T. Recently, various self-selective devices have been realized. Most devices have a bi-layer structure, but based on different physical mechanisms. The following are some typical examples categorized by mechanisms.

3.1.1 Interface phase transition. Huang *et al.* reported a self-selective device with a Pt/TiO_2/fluorine-doped tin oxide (FTO) structure.[50] Fig. 9a shows the nonlinear resistive switching *I–V* curves with a nonlinearity of ~10 in the device. The resistive switching is attributed to metallic filaments formed by oxygen vacancy drifting, while the nonlinearity in the device was attributed to a gradual transition of the sub-oxide phase in the TiO_{2-x} suboxide region near FTO electrodes. As schematized in Fig. 9b–e, the as-deposited device undergoes a formation process, where abundant heat generated by Joule heating facilitates the oxidation of TiO_2. Because the nanorods grow from bottom to top, the diameter of the nanorods near the top electrode is smaller than that at the bottom electrode, increasing the porosity of TiO_2 nanorods near the top electrode, which facilitates the top side to absorb more O_2. Consequently, the top layer becomes an oxygen-rich region (TiO_2), while the bottom layer is oxygen-deficient suboxide (TiO_{2-x}). Numbers of non-stoichiometric

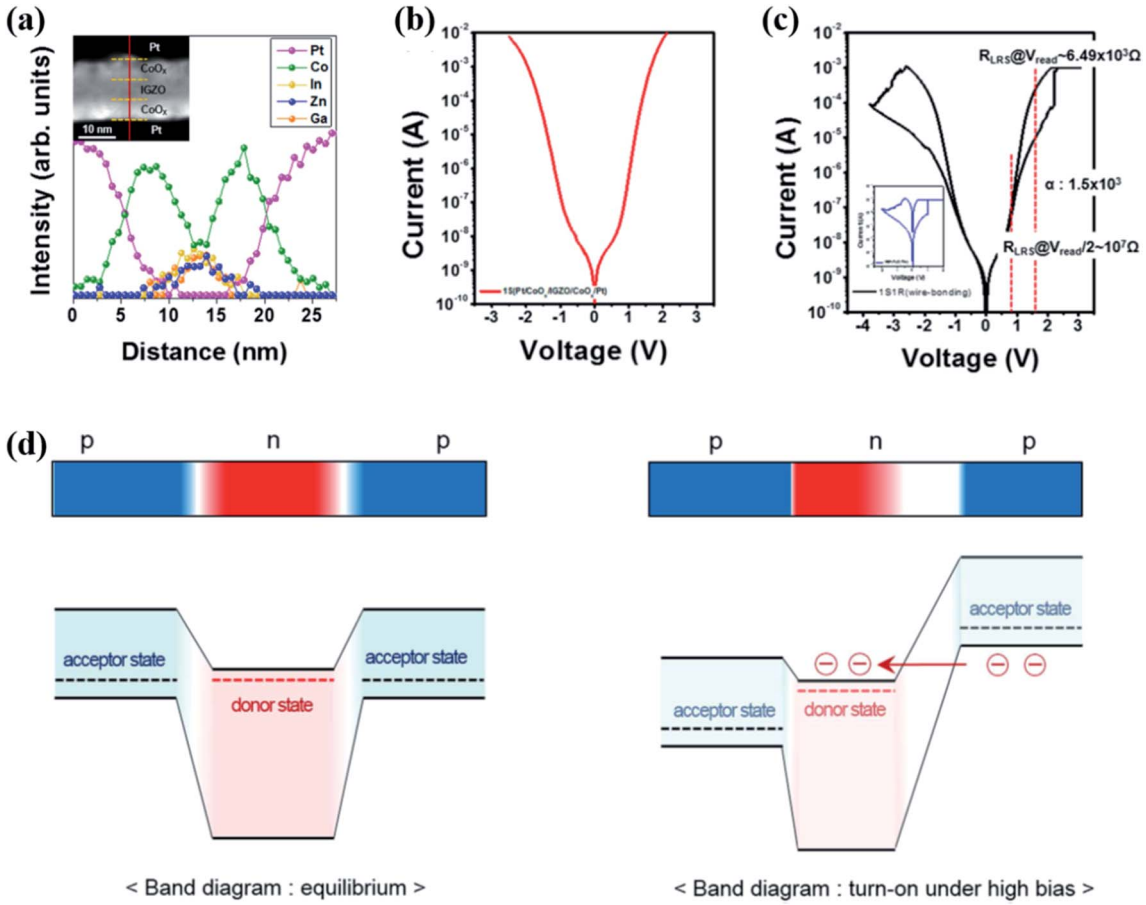

Fig. 8 (a) High-resolution EDS (HR-EDS) elemental line profile across a line of the STEM image, where the inset shows a dark-field STEM image of the Pt/CoO_x/IGZO/CoO_x/Pt frame. (b and c) *I*–*V* curves of a CoO_x/IGZO/CoO_x selector (b) and electrical connection unit containing both the Pt/CoO_x/IGZO/CoO_x/Pt selector and Pt/TaO_x/TiN memristor (c). (d) Schematic band diagram of the device p(emitter)–n(base)–p(collector) under zero (low) and high (above threshold) voltage bias, respectively (reproduced from ref. 40, Copyright 2015, with permission of Springer Nature).

Ti suboxides (Ti_nO_{2n-1}, the so-called Magnéli phase), including Ti_2O_3, Ti_3O_5, Ti_4O_7, Ti_5O_9,[64] have been shown to demonstrate the gradual transition from the metal to the insulator. Some other materials, such as VO_x,[65] are also reported to display self-selective resistive switching performance.

Table 3 Partially reported single-device memristors used in crossbar arrays

Structure	Mechanisms[a]	Fabrication temperature	Nonlinearity or ratio[b]	Endurance	Retention	Ref.
Pt/TiO_2-NRs/FTO, self-selective	Interface phase transition	350 °C	10	—	10^3 s	50
W/WO_3/WO_x/W, self-selective	Tunneling barrier	500 °C	8.8	—	10^3 s	51
Pd/TaO_x/HfO_2/Pd, self-selective	Tunneling barrier	300 °C	10^3	—	—	52
TiN/HfO_2/TaO_x/Ti, self-selective	Tunneling barrier	—	10^2	10^7	10^4 s	53
TiN/HfO_2/TiO_x/Ru, self-selective	Tunneling barrier	—	10^3	10^7	10^4 s	54
Au/h-BN/G/h-BN/Ag, self-selective	Volatile Ag filament	120 °C	10^{10}	10^6	10^6 s	55
Pt/Ta_2O_5/HfO_{2-x}/TiN, self-rectifying	Schottky barrier	280 °C	10^3	10^3	10^4 s	56
Pt/TiO_2/HfO_{2-x}/TiN, self-rectifying	Schottky barrier	280 °C	10^3	10^3	10^6 s	57
Pt/TaO_y/NP TaO_x/Ta, self-rectifying	Schottky barrier	—	10^4	10^3	10^4 s	58
Pt/C/NbO_x/TiN, self-rectifying	Asymmetric potential barrier	Room temperature	10^6	—	—	59
Pt/HfO_2/n^+-Si, self-rectifying	Asymmetric potential barrier	300 °C	10^5	10^3	10^4 s	60
Pt/NbO_x/TiO_y/NbO_x/TiN, self-rectifying	Asymmetric potential barrier	300 °C	10^5	10^3	10^3 s	61
Al/Cu-pMSSQ/Al, self-rectifying	Asymmetric potential barrier	160 °C	10^2	—	—	62
p-Si/SiO_2/n-Si, self-rectifying	Asymmetric potential barrier	400 °C	10^5	—	10^5 s	63

[a] The mechanism of self-nonlinear or self-rectifying memristors. [b] The nonlinearity is for self-selective memristors and the ratio is for self-rectifying memristors.

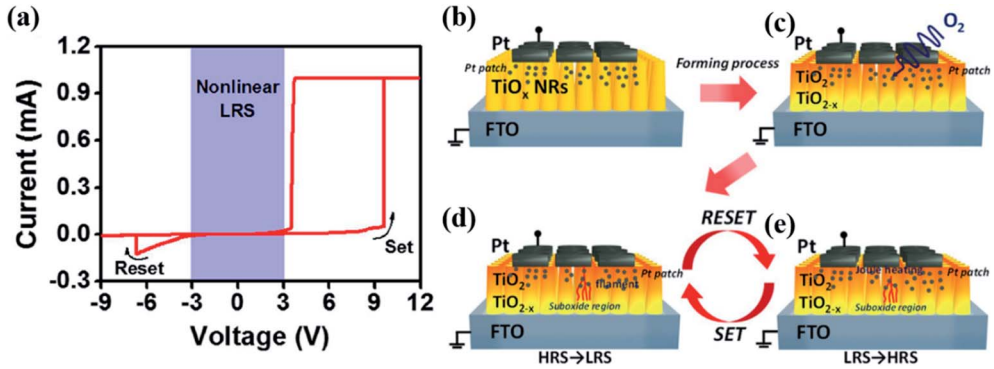

Fig. 9 (a) Nonlinear *I*–*V* curves of the Pt/TiO_2 NRs/FTO device. (b–e) Schematics of the nonlinear resistive switching mechanism. Four states: (b) the original state, (c) after the formation process, (d and e) back and forth switching between the set process and the reset process (reproduced from ref. 50, Copyright 2017, with permission of Springer Nature).

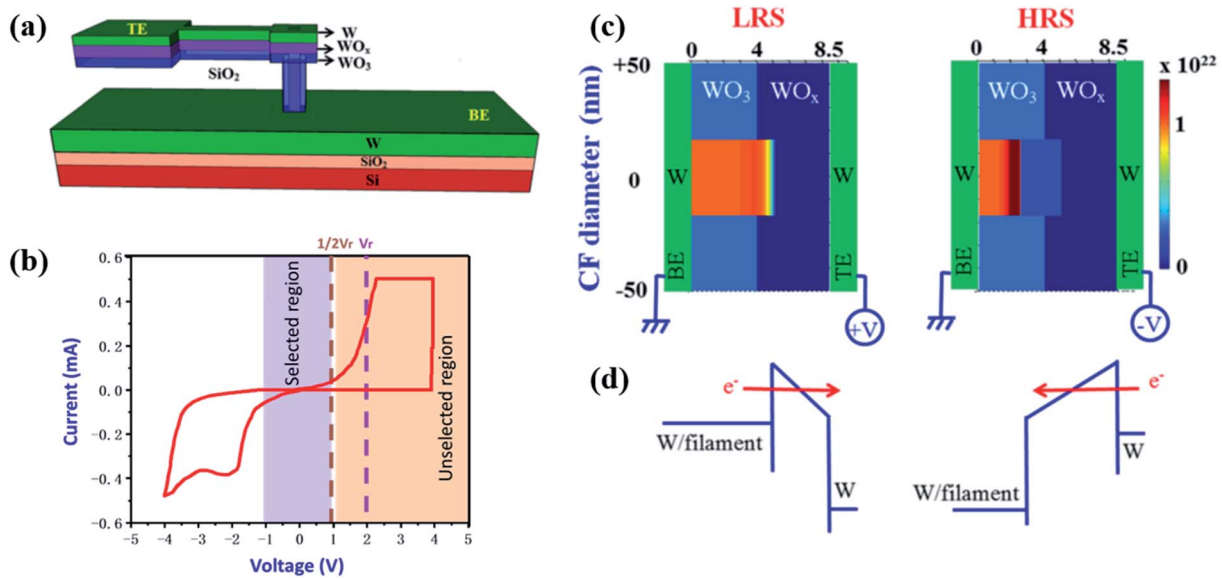

Fig. 10 (a) Schematic diagram of a W/WO_3/WO_x/W resistive switching memory device. (b) *I*–*V* curves of the device. (c and d) Schematic diagram of the oxygen-vacancy filament of the device at both LRS and HRS (c) and the corresponding energy band diagram (d) (reproduced from ref. 51, Copyright 2016, with permission of Springer Nature).

3.1.2 Tunneling barrier. Stimulated by the nonlinearity of the tunneling barrier, the device adding a tunneling barrier in their structure is proposed as a self-selective one. Chakrabarti *et al.* reported a self-selective device with a W/WO_3/WO_x/W structure[51] (Fig. 10a). Fig. 10c shows the schematic diagram of the resistive filament for the low resistance state (LRS) and high resistance state (HRS), respectively. Due to the gap barrier near the top electrode (TE), the Fowler–Nordheim (F–N) tunneling (Fig. 10d) under high bias gives the nonlinearity of the *I*–*V* curves. The *I*–*V* curves present nonlinear resistive switching (Fig. 10b). Wang *et al.* demonstrated nonlinear *I*–*V* curves in the Pd/TaO_x/Ta/Pd junction (Fig. 11a), whose conductance mechanism arises from tunneling or thermionic emission.[52] The energy band diagram is shown in Fig. 11b. Under positively biased voltage, both tunneling and thermionic electron emission contribute to the current. At reversely biased voltage, only the tunneling electron transport dominates the current. These tunneling and thermionic emission mechanisms give the nonlinear conductance behavior (Fig. 11c). Replacing Ta by HfO_2 as the switching layer, the unit shows a nonlinear resistive switching and the *I*–*V* curves agree well with the simulation based on these aforementioned mechanisms (Fig. 11d). This integrated device shows a high nonlinearity (5×10^3) in the low resistance state and could be considered as a self-selective memristor device.

By designing a bilayer structure of HfO_2/TaO_x, where the HfO_2 layer plays the role of the tunneling barrier[53], Lv and Liu's groups realized self-selective resistive devices with outstanding properties, including high nonlinearity (>10^2) and high endurance (>10^7). Interestingly, based on these self-selective resistive devices, an 8-layer 3D vertical RRAM architecture with 5 nm size and 4 nm vertical pitch was demonstrated. Bayat *et al.* designed a Pt/Al_2O_3/TiO_{2-x}/Ti/Pt memristor whose nonlinearity arises

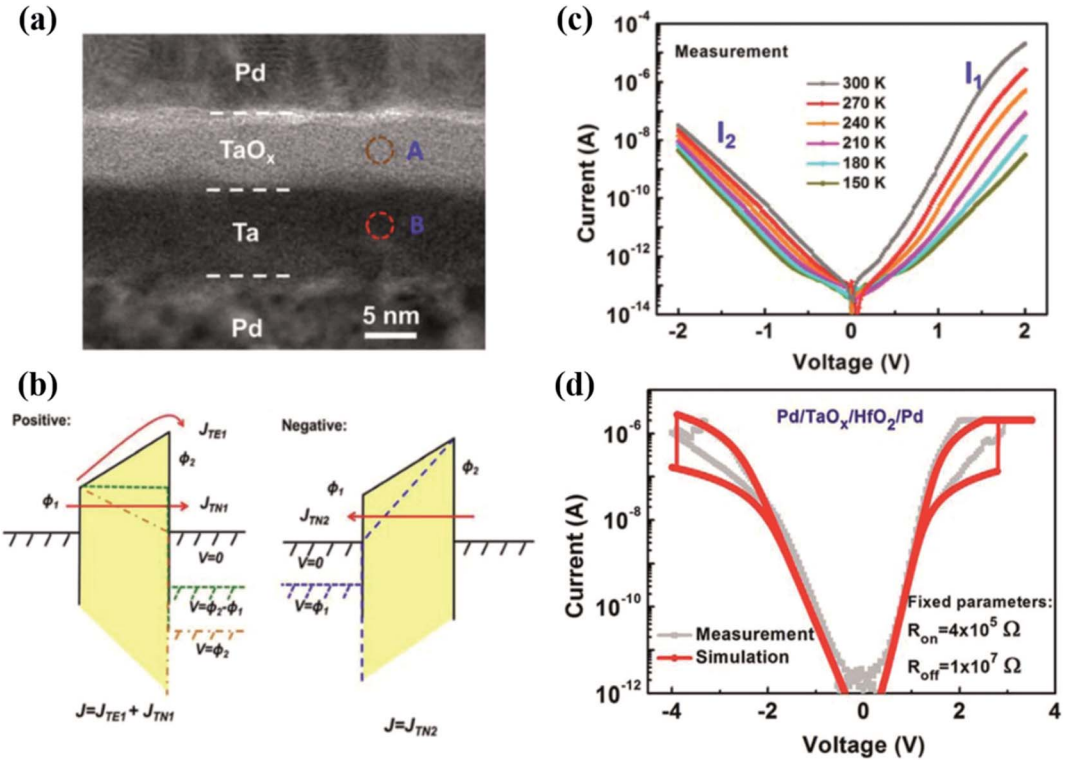

Fig. 11 (a) The high resolution cross-sectional TEM image of a Pd/TaO_x/Ta/Pd device. (b) Schematic diagrams of the band diagram of the Pd/TaO_x/Ta/Pd tunneling junction under positive and negative bias. (c) *I–V* curves of the Pd/TaO_x/Ta/Pd device at different temperatures from 150 K to 300 K. (d) *I–V* curves of the Pd/TaO_x/HfO_2/Pd device, the red lines represent the simulation using fixed values of $R_{on} = 4 \times 10^5\ \Omega$ and $R_{off} = 1 \times 10^7\ \Omega$ (reproduced from ref. 52, Copyright 2015, with permission of Royal Society of Chemistry).

from the alumina tunneling barrier.[66] Passive 20 × 20 crossbar arrays based on this nonlinear memristor were fabricated, in which leakage currents are sufficiently suppressed. Assisted by *ex situ* training, these passive 20 × 20 crossbar arrays achieve classification fidelity within 3% of that obtained in simulations[66].

3.1.3 Volatile filament in van der Waals heterostructure. Sun *et al.* proposed a self-selective memory cell based on the Au/h-BN/G/h-BN/Ag van der Waals heterostructure (Fig. 12a),[55] where h-BN and G are hexagonal boron nitride and graphene respectively. Non-volatile boron vacancy filaments and volatile silver filaments are formed in Au/h-BN/G and G/h-BN/Ag structures, respectively. In the cell integrating the non-volatile and volatile structures together, the graphene layer efficiently blocks the diffusion of volatile silver filaments (Fig. 12c), resulting in a highly nonlinear resistive switching with a self-selectivity of 10^{10} and an on/off resistance ratio of more than 10^3 (Fig. 12b). Based on these self-selective memory cells, a 12 × 12 crossbar array is demonstrated. Due to the high self-selectivity of 10^{10}, a code of "SKKU" was successfully programmed using 144 binary bits for four letters (SKKU) in their 12 × 12 crossbar array.[55] Taking into account the on-the-way wafer ability of 2D materials, efficient crossbar arrays using van der Waals heterostructures on flexible substrates are expectable.

3.2 Self-rectifying memristor

In contrast to selector-less memristors whose *I–V* curves are nonlinear, self-rectifying memristors are single-stack devices where reverse current is extremely small. Therefore, self-rectifying memristors resemble bipolar 1D1M structures. Thus, as discussed in Part 2.2, to eliminate the unintended programming, the amplitude of the reverse threshold voltage should be higher than that of the forward threshold voltage in self-rectifying memristors. The self-rectifying property mostly originates from the asymmetric barrier due to the Schottky contact or asymmetric potential in the devices, while various mechanisms contribute to these memristive behaviors. The following are some typical examples.

3.2.1 Self-rectifying memristors based on poly(-methylsilsesquioxane) (PMSSQ). Wu *et al.* reported a well-designed flexible structure where copper (Cu) ions are non-uniformly doped into a PMSSQ polymer.[62] PMSSQ is a hole-injection material.[67] In Wu's work, ultraviolet-visible absorption spectra confirmed that the energy gap decreases with increasing Cu concentration. As shown in Fig. 13a, the device has a structure of Al/lightly-doped layer/highly-doped layer/Al. The schematic energy band diagrams under positive and negative biases are also shown. The currents here are dominated by the contact barrier using positive bias. When positive bias is applied to the device, the contact barrier under positive bias (pre-electrode side) is small, and holes tunnel into the

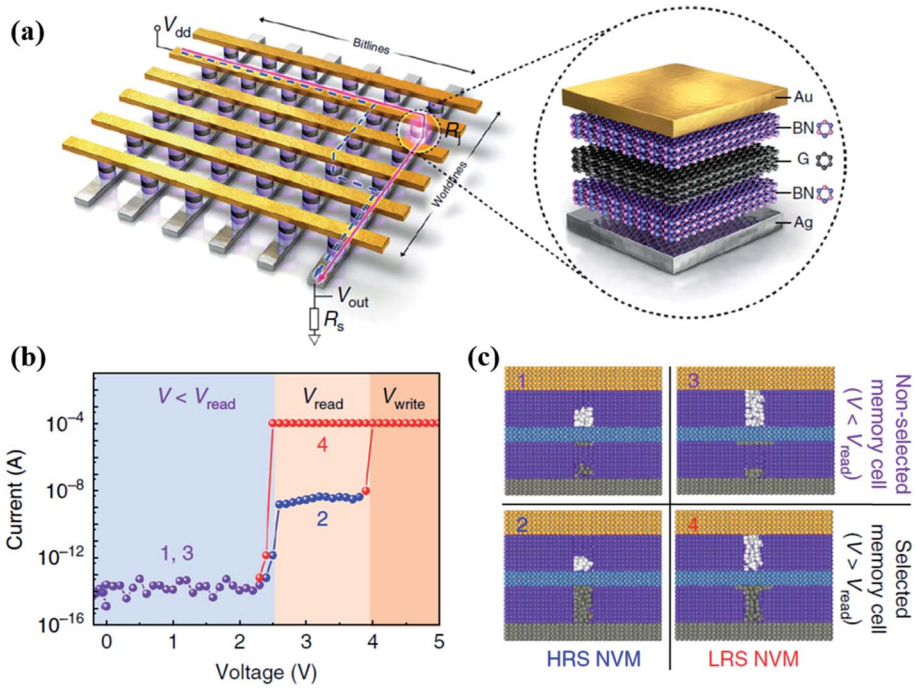

Fig. 12 (a) Schematic of the Au/h-BN/G/h-BN/Ag van der Waals heterostructure in the crossbar array architecture. (b) *I*–*V* curves of an Au/h-BN/G/h-BN/Ag memory cell in the crossbar array. (c) Schematic pictures of the Au/h-BN/G/h-BN/Ag memory cell for the four states in (b). States "1" and "3" represent the high-resistance state and low-resistance state of unselected cells, respectively. States "2" and "4" represent the high-resistance state and low-resistance state of a selected memory cell, respectively. A complete conductive silver filament is formed in state "2" and state "4". A complete conductive boron vacancy filament is formed in state "3" and state "4". The gray, purple, blue, yellow and white spheres represent silver, hexagonal boron nitride, graphene, gold and boron vacancies, respectively (reproduced from ref. 55, Copyright 2019, with permission of Springer Nature).

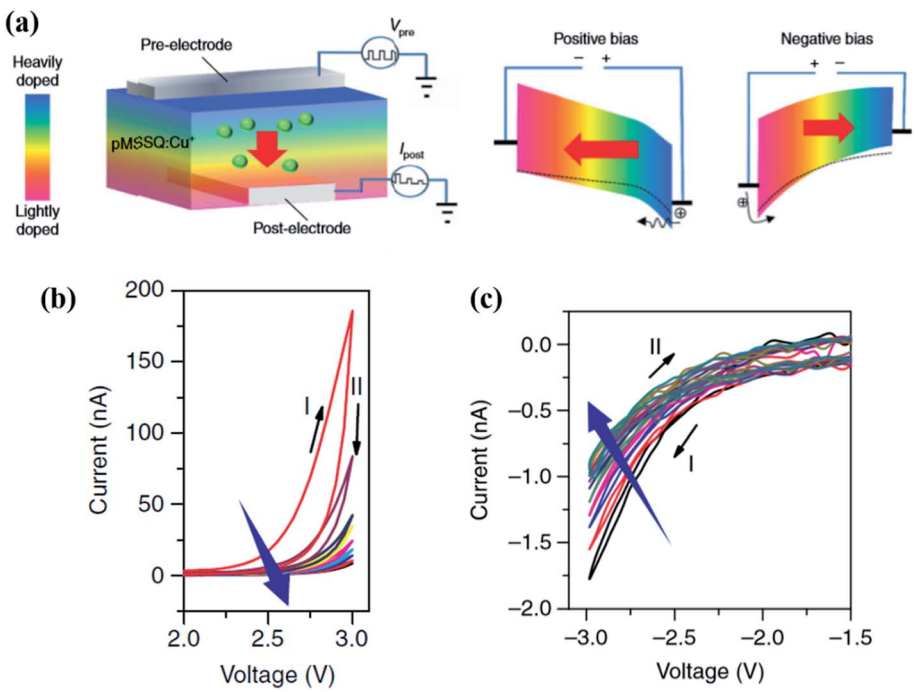

Fig. 13 (a) Schematic diagram and band structure of the sandwiched structure of Al (bottom electrode)/lightly doped layer/highly doped layer/Al (top electrode), and the kinetic model of carrier transportation under both polarization of voltage bias. (b) *I*–*V* curves under consecutive positive bias sweeps. (c) *I*–*V* curves under consecutive positive bias sweeps after the positive bias sweeps (reproduced from ref. 62, Copyright 2017, with permission of Springer Nature).

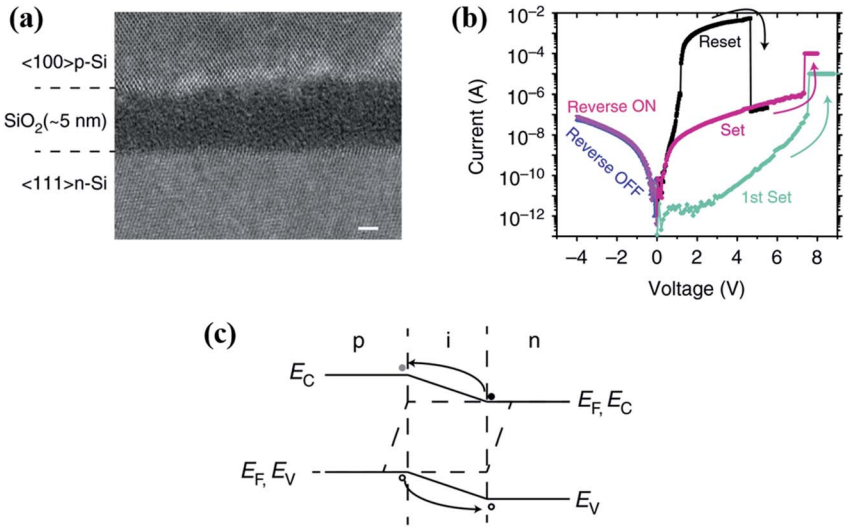

Fig. 14 (a) Cross-sectional TEM image of the Si/SiO_2/Si device shows a single crystalline structure for the top and bottom electrodes and the 5 nm amorphous SiO_2 switching layer. Scale bar, 2 nm. (b) A typical unipolar resistive switching *I*–*V* curve of the Si/SiO_2/Si device. The n-Si bottom electrode was grounded while the bias was applied to the p-Si top electrode. (c) The band diagram in LRS under a forward bias describes a piece of non-degenerated silicon bridge between two degenerate silicon electrodes. The excess holes flow from the p-type electrode to the n-type electrode while the electrons flow from the n-type electrode to the p-type electrode (reproduced from ref. 63, Copyright 2017, with permission of Nature Publishing Group).

PMSSQ (F–N tunneling), leading to a large current. Simultaneously, copper ions are drifted away from the pre-electrode, increasing the barrier height and decreasing the conductance. As shown in Fig. 13b, the current is relatively large under the first forward voltage sweeping and gradually dwindles under repeated forward voltage sweepings. When negative bias is applied to the device, the contact barrier under positive bias (post-electrode side) is big, holes inject into the PMSSQ with a thermionic emission mechanism, and the current is small (Fig. 13c). It is noted that the conductance increases (under positive read voltage) while the currents decrease with these repeated negative voltage sweepings. The switching of tunneling and thermionic emission mechanisms between positive and negative biases leads to the self-rectifying property of this single-device memristor with a rectifying ratio of 100. Meanwhile, the drifting of Cu ions under an applied field enables multi-level states of the device. This unique *I*–*V* characteristic facilitates its application in neuromorphic networks. Three-dimensional (3D) device networks based on this flexible structure are successfully realized, which shows the feasibility of using them in future electronic devices involving hierarchical neural networks.[62]

3.2.2 All-silicon-based self-rectifying memristor. Li *et al.* reported an all-silicon-based memristor with a structure of p-Si/SiO_2/n-Si[63] (Fig. 14a). A conducting channel made of a non-degenerate semiconductor is formed between the top p and bottom n silicon, and the energy band diagram is shown in Fig. 14c. This all-silicon-based memristor shows a repeatable unipolar resistive switching behavior with a rectifying ratio of 10^5 and ON/OFF ratio of 10^4 (Fig. 14b), which effectively suppresses the sneak-path current and enables larger array operations without discrete selectors. Suppression of both intra- and inter-layer sneak-path currents is experimentally confirmed in 3D crossbar arrays made of these all-silicon-based memristors. The fabrication of such a device is highly compatible with the current CMOS process, which indicates its practical suitability.

3.2.3 Charge-trap-associated self-rectifying memristor. Generally, electron effect-based resistive devices show highly uniform switching performances. By inducing a Schottky contact or asymmetric electrodes (asymmetric potential barrier in the device) into an electron trapping/detrapping system, a charge-trap-associated self-rectifying memristor is obtained.[56,57]

Kim *et al.* designed a low-current and self-rectifying Pt/NbO_x/TiO_y/NbO_x/TiN device[61] (Fig. 15a), where the memristive behavior is attributed to the electron trapping/detrapping process while the asymmetric potential barriers induce a self-rectifying ratio of $\sim 10^5$. The schematic energy band diagram of the device is shown in Fig. 15b; a trap energy as deep as 0.8 eV is formed in the TiO_y layer. The as-deposited devices experienced a 300 °C atmosphere during the fabrication process, which facilitates the trap sites to be filled with electrons. The *I*–*V* curves are shown in Fig. 15a, and the corresponding evolution of energy diagrams is shown in Fig. 15c. As mentioned above, electrons are trapped in the trap sites initially. These electrons attract positive charges to accumulate at the interface of the electrodes, leading to a built-in electric field pointing toward the trap sites. Under this circumstance, the whole barrier height increases, giving a high resistive state (HRS). When positively biased voltage is applied, the Fermi level of the Pt electrode is pulled down, and electrons are released to the Pt electrode. This detrapping process leads the device to the low resistive state (LRS). There can also be a trapping process from the TiN electrode to the trap sites, which is much weaker than the detrapping process because of the longer tunneling distance between

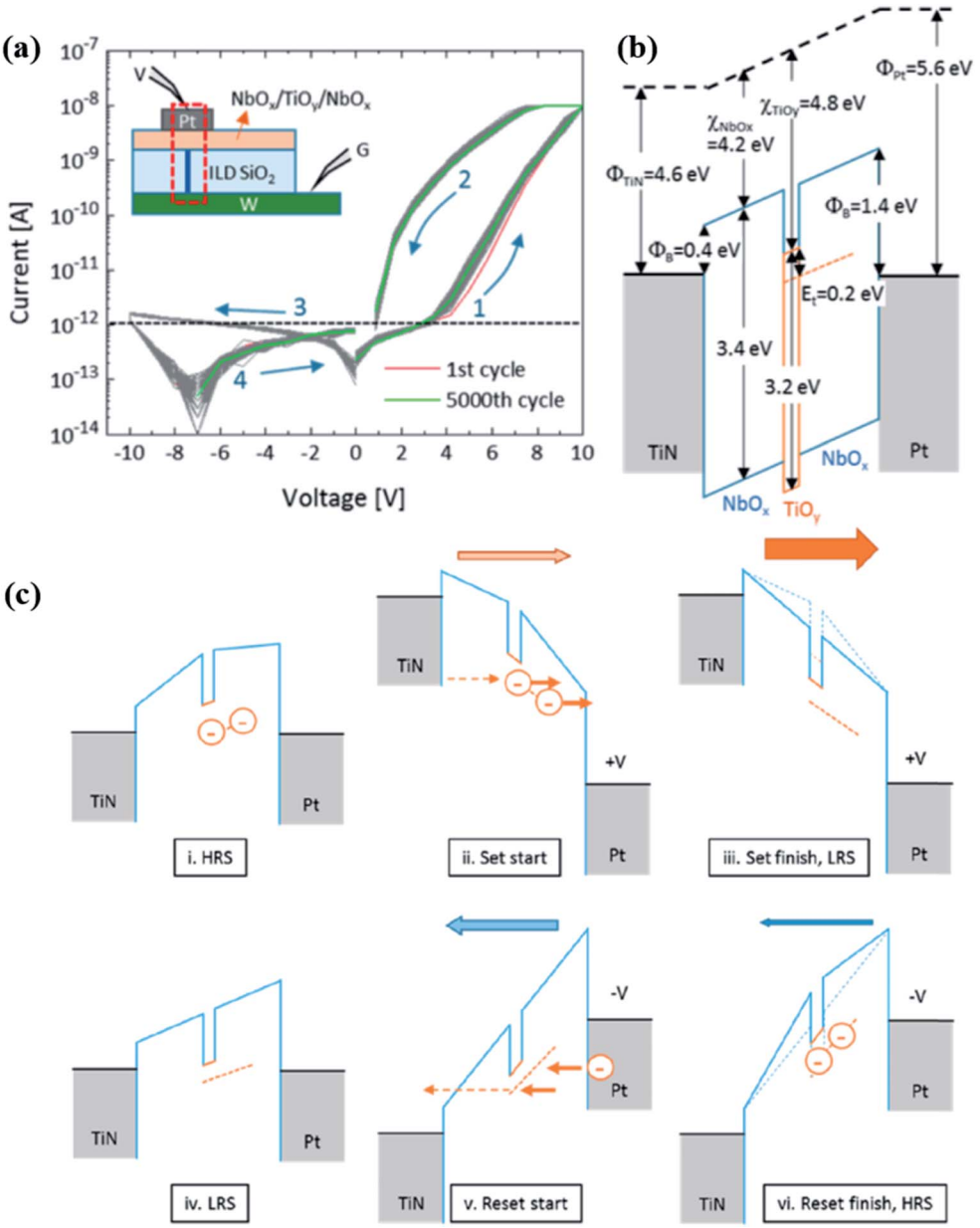

Fig. 15 (a) *I*–*V* curves of the Pt/NbO_x/TiO_y/NbO_x/TiN device. Inset shows the structure of the device and the test setup for the measurement. (b) The energy band diagram of the device. (c) Diagram of the charge capture and decapture process in the device. (i) The HRS, electrons fill the trap sites. (ii and iii) A positive set bias is applied on the Pt electrode, (iv) LRS, the trapped electrons can be released. (v and vi) A negative reset bias is applied, and the HRS is restored (adapted from ref. 61, Copyright 2016, with permission of American Chemical Society).

the TiN and trap sites. Similarly, the memristor is switched back to the HRS when the negatively biased voltage sweeps.

Wang *et al.* designed a synaptic memory of Pt/C/NbO_x/TiN.[59] The charge trapping and detrapping in the NbO_x film dominate the resistive switching. The inserted C layer plays a role of forming an asymmetric potential barrier in the device, resulting in a self-rectifying ratio of 10^6. The high self-rectifying ratio of 10^6 effectively eliminates sneak path currents, and thus the conductance in a crossbar array can be efficiently programed. Excellent classification accuracy (95.7%) of handwritten digits is achieved by a simulation of two-layer perceptron neural networks based on these self-rectifying Pt/C/NbO_x/TiN devices.

There are also other self-rectifying memristors associating memristive mechanisms such as interaction of composition dependent thermal conductivity and oxygen-ion migration,[58,68–70] electron tunneling controlled by ferroelectric surfaces,[71,72] and interfacial trap site engineering.[73] Most reported self-rectifying memristors do not show an abrupt increase and decrease of conductance. These properties indicate that self-rectifying memristors have great potential application for neuromorphic networks. However, most reported self-rectifying memristors suffer from an important issue of poor endurance (Table 3). This may be due to the fact that a high barrier is usually induced to achieve self-rectification, which inevitably needs a higher voltage operation for

programing the states. Reducing the syndrome of high voltage needs to be explored.

4. Perspectives

Memristors are new non-volatile electronic memory devices with programmable resistance that has enormous potential application in tomorrow's electronics. One of the appealing aspects is that memristor crossbar arrays can be an ideal candidate for hardware neuromorphic networks. The memristor crossbar array can implement algorithms more efficiently with much lower power consumption. However, to realize this attractive prospect, the sneak-path current issue must be overcome. Thanks to the efforts of researchers in the academic domain over the years, quite a number of solutions have been proposed to solve this sneak-path problem, and each specific category of solutions has been developed at a more and more sophisticated level, which improves the possibility for real applications.

As a matter of fact, a potential solution is the 1T1M structure. Due to its high compatibility with the CMOS process, 1T1M has become the most practical approach. The transistor in this structure could precisely manipulate the ON/OFF state of the cell, which mitigates the sneak path currents and half-select issues during array programming and reading. Moreover, the gate voltage could provide controllability of the synaptic weight by regulating the limit resistance of the cell, which is significant for application in neuromorphic networks, such as, by offering compliance currents, the gate lines in the 1T1M crossbar array assist in obtaining the linear and symmetric conductance increase and decrease with minimal cycle-to-cycle and device-to-device variations, which is favorable for time-efficient current domain VMM computing.

However, 1T1M has a cell area of $8F^2$, which is relatively large and limits the scaling of the array and integration density. To minimize as much as possible the scaling issue, a high channel conductance of transistors is preferred. Despite the large cell area, CMOS transistors take advantage of their sophisticated fabrication techniques and scalability, whereby vast 1T1M crossbar arrays are fabricated and demonstrated to perform well in various complicated information processing operations.

In a passive array, which has a cell area of $4F^2$, a much higher packing density and 3D stackability are achieved. On the other hand, it suffers from half-select issues, resulting in large energy consumption during the programming and reading of the cells in large-scale arrays. To overcome this issue, a high rectification ratio or nonlinearity must be induced to memristors by connecting a series diode or nonlinear selector or by itself. The series diode or nonlinear selector doesn't increase footpoints, thus sustaining the advantage of high packing density and stackability.

For the 1D1M structure, a higher rectification ratio and bigger forward current density allow larger and denser crossbar arrays. The series diode also acts as an external load resistor to suppress the overflow current during the resistance transition, which significantly improves the cycle-to-cycle distribution of the integrated cells. Recently, the forward/reverse ratio of the series diode has been continuously increased. The application of this solution is not only subject to unipolar memristors but extends to bipolar devices. The TiO_2-based Schottky diode with a rectification ratio as high as 1.4×10^9 and an endurance of 10^8 cycles is very promising for application in large crossbar arrays.

As for 1S1M, to reduce the energy consumption and improve the performance of programming and reading of the cells in large-scale arrays, selector devices with high nonlinearity must be created. Nonlinear selectors based on the tunneling barrier, OTS and p-/n-combination have been vastly researched in these 3 years. The nonlinearity of tunneling barrier selectors results from the intrinsic physical mechanism. The abrupt high currents don't need assistance of Joule heating, and are independent of temperature, which benefits low energy consumption and wide available temperature windows. The tunnel selectors also possess excellent speed and reproducibility. One of the drawbacks is the high temperature fabrication process, limiting its further integrating. Low temperature tunneling barrier selectors need to be explored. The biggest stumbling block for p–n–p and n–p–n selectors is the low current density, which needs a large cell area to switch the accompanied memristor and hinders a high-density crossbar array. The outstanding nonlinearity and endurance behaviors in ion-based OTS selectors are appealing. But the dynamics of ions is slower compared with electrons; electron-based OTS selectors usually possess a transition time less than 10 ns, and are also capable of high endurance, such as an ultrahigh endurance of 10^{12} in $Nb_{1-x}O_2$ based and 10^8 in SiTe based selectors. OTS selectors based on the pure electron mechanism are promising for large and dense crossbar arrays.

Self-selective and self-rectifying memristors show great potential for solving the sneak-path current issue with a simple structure. These two aforementioned solutions using a single device instead of two move a step further in down-scaling (including the cost). Self-rectifying memristors usually suffer from poor endurance due to the high voltage operation. Self-nonlinear selectors based on either CMOS-compatible oxides or van der Waals Materials are promising for huge and dense crossbar arrays. One note is recalled that VMM computation in 1S1M or single-device memristor crossbar arrays is limited to the charge domain method (by modulating the pulse width or number) due to the nonlinear *I–V* curves.

In short, this fast-growing field of research is still in its infancy and we hope this overview concerning the sneak-path current problem will benefit the field and arouse the curiosity and inventiveness of researchers and engineers from chemistry, physics, materials science, electronics and computing science.

Conflicts of interest

There are no conflicts to declare.

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Notes and references

1 G. W. Burr, R. M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler, K. Virwani, M. Ishii, P. Narayanan, A. Fumarola, L. L. Sanches, I. Boybat, M. Le Gallo, K. Moon, J. Woo, H. Hwang and Y. Leblebici, *Adv. Phys.: X*, 2016, **2**, 89–124.

2 B. Hudec, C.-W. Hsu, I. T. Wang, W.-L. Lai, C.-C. Chang, T. Wang, K. Fröhlich, C.-H. Ho, C.-H. Lin and T.-H. Hou, *Sci. China Inf. Sci.*, 2016, **59**, 061403.

3 S. Gi, I. Yeo, M. Chu, S. Kim and B. Lee, *International SoC Design Conference (ISOCC)*, 2015, p. 215.

4 F. Pan, S. Gao, C. Chen, C. Song and F. Zeng, *Mater. Sci. Eng., R*, 2014, **83**, 1–59.

5 J. Y. Seok, S. J. Song, J. H. Yoon, K. J. Yoon, T. H. Park, D. E. Kwon, H. Lim, G. H. Kim, D. S. Jeong and C. S. Hwang, *Adv. Funct. Mater.*, 2014, **24**, 5316–5339.

6 M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, J. J. Yang, Q. Xia and J. P. Strachan, *Adv. Mater.*, 2018, **30**, 1705914.

7 F. Cai, J. M. Correll, S. H. Lee, Y. Lim, V. Bothra, Z. Zhang, M. P. Flynn and W. D. Lu, *Nat. Electron.*, 2019, **2**, 290–299.

8 H. Jiang, K. Yamada, Z. Ren, T. Kwok, F. Luo, Q. Yang, X. Zhang, J. J. Yang, Q. Xia, Y. Chen, H. Li, Q. Wu and M. Barnell, *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018.

9 Q. Xia and J. J. Yang, *Nat. Mater.*, 2019, **18**, 309–323.

10 Y. Chen, G.-Y. Jung, D. A. A. Ohlberg, X. Li, D. R. Stewart, J. O. Jeppesen, K. A. Nielsen, J. F. Stoddart and R. S. Williams, *Nanotechnology*, 2003, **14**, 462–468.

11 Y.-C. Chen, C. F. Chen, C. T. Chen, J. Y. Yu, S. Wu, S. L. Lung, R. Liu and C.-Y. Lu, *IEEE International Electron Devices Meeting (IEDM)*, 2003, vol. 03, p. 905.

12 A. Ciprut and E. G. Friedman, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2018, **26**, 711–719.

13 C. Li, D. Belkin, Y. Li, P. Yan, M. Hu, N. Ge, H. Jiang, E. Montgomery, P. Lin, Z. Wang, W. Song, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang and Q. Xia, *Nat. Commun.*, 2018, **9**, 2385.

14 S. Yu, Z. Li, P.-Y. Chen, H. Wu, B. Gao, D. Wang, W. Wu and H. Qian, *IEEE International Electron Devices Meeting (IEDM)*, 2016, vol. 16, p. 416.

15 R. Mochida, K. Kouno, Y. Hayata, M. Nakayama, T. Ono, H. Suwa, R. Yasuhara, K. Katayama, T. Mikawa and Y. Gohou, *Symposium on VLSI Technology Digest of Technical Papers*, 2018, p. 175.

16 S. Ambrogio, P. Narayanan, H. Tsai, R. M. Shelby, I. Boybat, C. di Nolfo, S. Sidler, M. Giordano, M. Bodini, N. C. P. Farinha, B. Killeen, C. Cheng, Y. Jaoudi and G. W. Burr, *Nature*, 2018, **558**, 60–67.

17 Y. Shi, L. Nguyen, S. Oh, X. Liu, F. Koushan, J. R. Jameson and D. Kuzum, *Nat. Commun.*, 2018, **9**, 5312.

18 C.-X. Xue, W.-H. Chen, J.-S. Liu, J.-F. Li, W.-Y. Lin, W.-E. Lin, J.-H. Wang, W.-C. Wei, T.-W. Chang, T.-C. Chang, T.-Y. Huang, H.-Y. Kao, S.-Y. Wei, Y.-C. Chiu, C.-Y. Lee, C.-C. Lo, Y.-C. King, C.-J. Lin, R.-S. Liu, C.-C. Hsieh, K.-T. Tang and M.-F. Chang, *IEEE International Solid-State Circuits Conference (ISSCC)*, 2019, vol. 24.1, p. 388.

19 Y. Zhou, H. Wu, B. Gao, W. Wu, Y. Xi, P. Yao, S. Zhang, Q. Zhang and H. Qian, *Adv. Funct. Mater.*, 2019, **29**, 1900155.

20 H. Tsai, S. Ambrogio, C. Mackin, P. Narayanan, R. M. Shelby, K. Rocki, A. Chen and G. W. Burr, *Symposium on VLSI Technology Digest of Technical Papers*, 2019, vol. T82.

21 C.-H. Wang, C. McClellan, Y. Shi, X. Zheng, V. Chen, M. Lanza, E. Pop and H.-S. P. Wong, *IEEE International Electron Devices Meeting (IEDM)*, 2018, vol. 18, p. 528.

22 Y. Zhang, Z. Zhou, P. Huang, M. Fan, R. Han, W. Shen, L. Liu, X. Liu and J. Kang, *Silicon Nanoelectronics Workshop (SNW)*, 2019.

23 C. Mohan, L. A. Camuñas-Mesa, E. Vianello, L. Periniolla, C. Reita, J. M. de la Rosa, T. Serrano-Gotarredona and B. Linares-Barranco, *Microelectron. Eng.*, 2018, **198**, 35–47.

24 H.-X. Zheng, Y.-C. Zhang, X.-H. Ma, Y. Hao, S. M. Sze, M.-C. Chen, T.-C. Chang, Y.-T. Su, W.-C. Chen, W.-C. Huang, P.-Y. Wu, Y.-F. Tan and Y.-L. Xu, *IEEE Trans. Electron Devices*, 2019, **66**, 4706–4709.

25 P. Yao, H. Wu, B. Gao, S. B. Eryilmaz, X. Huang, W. Zhang, Q. Zhang, N. Deng, L. Shi, H. P. Wong and H. Qian, *Nat. Commun.*, 2017, **8**, 15199.

26 C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, J. Zhang, W. Song, N. Dávila, C. E. Graves, Z. Li, J. P. Strachan, P. Lin, Z. Wang, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang and Q. Xia, *Nat. Electron.*, 2017, **1**, 52–59.

27 C. Li, Z. Wang, M. Rao, D. Belkin, W. Song, H. Jiang, P. Yan, Y. Li, P. Lin, M. Hu, N. Ge, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang and Q. Xia, *Nature Machine Intelligence*, 2019, **1**, 49–57.

28 Z. Wang, C. Li, P. Lin, M. Rao, Y. Nie, W. Song, Q. Qiu, Y. Li, P. Yan, J. P. Strachan, N. Ge, N. McDonald, Q. Wu, M. Hu, H. Wu, R. S. Williams, Q. Xia and J. J. Yang, *Nature Machine Intelligence*, 2019, **1**, 434–442.

29 P. Yao, H. Wu, B. Gao, J. Tang, Q. Zhang, W. Zhang, J. J. Yang and H. Qian, *Nature*, 2020, **577**, 641–646.

30 M. Song, H. Lee, D. H. Seo, H.-J. Lee, J.-S. Kim, H.-S. Cho, H.-K. Lyu, S. Seo and M.-J. Lee, *IEEE J. Electron Devices Soc.*, 2018, **6**, 905–909.

31 D. K. Lee, G. H. Kim, H. Sohn and M. K. Yang, *Appl. Phys. Lett.*, 2019, **115**, 263502.

32 J. Yoon, Y. Ji, S.-K. Lee, J. Hyon and J. M. Tour, *Adv. Electron. Mater.*, 2018, **4**, 1700665.

33 K. J. Yoon, G. H. Kim, S. Yoo, W. Bae, J. H. Yoon, T. H. Park, D. E. Kwon, Y. J. Kwon, H. J. Kim, Y. M. Kim and C. S. Hwang, *Adv. Electron. Mater.*, 2017, **3**, 1700152.

34 Q. Wu, G. Yang, C. Lu, G. Xu, J. Wang, B. Dang, Y. Gong, X. Shi, X. Chuai, N. Lu, D. Geng, H. Wang, L. Li and M. Liu, *IEEE Trans. Electron Devices*, 2019, **66**, 9.

35 K.-J. Lee, Y.-C. Chang, C.-J. Lee and Y.-H. Wang, *Vacuum*, 2017, **140**, 35–41.

36 J. Shin, I. Kim, K. P. Biju, M. Jo, J. Park, J. Lee, S. Jung, W. Lee, S. Kim, S. Park and H. Hwang, *J. Appl. Phys.*, 2011, **109**, 033712.
37 M. Wang, X. Lian, Y. Pan, J. Zeng, C. Wang, E. Liu, B. Wang, J. J. Yang, F. Miao and D. Xing, *Appl. Phys. A: Mater. Sci. Process.*, 2015, **120**, 403–407.
38 B. J. Choi, J. Zhang, K. Norris, G. Gibson, K. M. Kim, W. Jackson, M. X. Zhang, Z. Li, J. J. Yang and R. S. Williams, *Adv. Mater.*, 2016, **28**, 356–362.
39 D. Kumar, R. Aluguri, U. Chand and T.-Y. Tseng, *IEEE Trans. Electron Devices*, 2019, **66**, 1296–1301.
40 Y. C. Bae, A. R. Lee, G. H. Baek, J. B. Chung, T. Y. Kim, J. G. Park and J. P. Hong, *Sci. Rep.*, 2015, **5**, 13362.
41 Q. Luo, J. Yu, X. Zhang, K.-H. Xue, J.-H. Yuan, Y. Cheng, T. Gong, H. Lv, X. Xu, P. Yuan, J. Yin, L. Tai, S. Long, Q. Liu, X. Miao, J. Li and M. Liu, *Symposium on VLSI Technology Digest of Technical Papers*, 2019, vol. T236.
42 R. Midya, Z. Wang, J. Zhang, S. E. Savel'ev, C. Li, M. Rao, M. H. Jang, S. Joshi, H. Jiang, P. Lin, K. Norris, N. Ge, Q. Wu, M. Barnell, Z. Li, H. L. Xin, R. S. Williams, Q. Xia and J. J. Yang, *Adv. Mater.*, 2017, **29**, 1604457.
43 Y. Koo, S. Lee, S. Park, M. Yang and H. Hwang, *IEEE Electron Device Lett.*, 2017, **38**, 568–571.
44 B. Song, H. Xu, S. Liu, H. Liu and Q. Li, *IEEE J. Electron Devices Soc.*, 2018, **6**, 674–679.
45 B. Song, H. Xu, S. Liu, H. Liu, Q. Liu and Q. Li, *Appl. Phys. A: Mater. Sci. Process.*, 2019, **125**, 772.
46 C.-H. Huang, K. Matsuzaki and K. Nomura, *Appl. Phys. Lett.*, 2020, **116**, 023503.
47 A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthelemy and J. Grollier, *Nat. Mater.*, 2012, **11**, 860–864.
48 W. Huang, Y. W. Fang, Y. Yin, B. Tian, W. Zhao, C. Hou, C. Ma, Q. Li, E. Y. Tsymbal, C. G. Duan and X. Li, *ACS Appl. Mater. Interfaces*, 2018, **10**, 5649–5656.
49 B. B. Tian, J. L. Wang, S. Fusil, Y. Liu, X. L. Zhao, S. Sun, H. Shen, T. Lin, J. L. Sun, C. G. Duan, M. Bibes, A. Barthelemy, B. Dkhil, V. Garcia, X. J. Meng and J. H. Chu, *Nat. Commun.*, 2016, **7**, 11502.
50 C. H. Huang, T. S. Chou, J. S. Huang, S. M. Lin and Y. L. Chueh, *Sci. Rep.*, 2017, **7**, 2066.
51 S. Chakrabarti, S. Samanta, S. Maikap, S. Z. Rahaman and H. M. Cheng, *Nanoscale Res. Lett.*, 2016, **11**, 389.
52 M. Wang, J. Zhou, Y. Yang, S. Gaba, M. Liu and W. D. Lu, *Nanoscale*, 2015, **7**, 4964–4970.
53 Q. Luo, X. Xu, T. Gong, H. Lv, D. Dong, H. Ma, P. Yuan, J. Gao, J. Liu, Z. Yu, J. Li, S. Long, Q. Liu and M. Liu, *IEEE International Electron Devices Meeting (IEDM)*, 2017, vol. 17, p. 48.
54 X. Xu, Q. Luo, T. Gong, H. Lv, S. Long, Q. Liu, S. S. Chung, J. Li and M. Liu, *Symposium on VLSI Technology Digest of Technical Papers*, 2016.
55 L. Sun, Y. Zhang, G. Han, G. Hwang, J. Jiang, B. Joo, K. Watanabe, T. Taniguchi, Y. M. Kim, W. J. Yu, B. S. Kong, R. Zhao and H. Yang, *Nat. Commun.*, 2019, **10**, 3161.
56 J. H. Yoon, S. Yoo, S. J. Song, K. J. Yoon, D. E. Kwon, Y. J. Kwon, T. H. Park, H. J. Kim, X. L. Shao, Y. Kim and C. S. Hwang, *ACS Appl. Mater. Interfaces*, 2016, **8**, 18215–18221.
57 J. H. Yoon, D. E. Kwon, Y. Kim, Y. J. Kwon, K. J. Yoon, T. H. Park, X. L. Shao and C. S. Hwang, *Nanoscale*, 2017, **9**, 11920–11928.
58 S. Choi, S. Jang, J.-H. Moon, J. C. Kim, H. Y. Jeong, P. Jang, K.-J. Lee and G. Wang, *NPG Asia Mater.*, 2018, **10**, 1097–1106.
59 W. Wang, R. Wang, T. Shi, J. Wei, R. Cao, X. Zhao, Z. Wu, X. Zhang, J. Lu, H. Xu, Q. Li, Q. Liu and M. Liu, *IEEE Electron Device Lett.*, 2019, **40**, 1407–1410.
60 X. Zhang, H. Ji and R. Jiang, *IEEE Trans. Electron Devices*, 2019, **66**, 3337–3341.
61 K. M. Kim, J. Zhang, C. Graves, J. J. Yang, B. J. Choi, C. S. Hwang, Z. Li and R. S. Williams, *Nano Lett.*, 2016, **16**, 6724–6732.
62 C. Wu, T. W. Kim, H. Y. Choi, D. B. Strukov and J. J. Yang, *Nat. Commun.*, 2017, **8**, 752.
63 C. Li, L. Han, H. Jiang, M. H. Jang, P. Lin, Q. Wu, M. Barnell, J. J. Yang, H. L. Xin and Q. Xia, *Nat. Commun.*, 2017, **8**, 15666.
64 J. Woo, D. Lee, G. Choi, E. Cha, S. Kim, W. Lee, S. Park and H. Hwang, *Microelectron. Eng.*, 2013, **109**, 360–363.
65 M. Son, X. Liu, S. M. Sadaf, D. Lee, S. Park, W. Lee, S. Kim, J. Park, J. Shin, S. Jung, M.-H. Ham and H. Hwang, *IEEE Electron Device Lett.*, 2012, **33**, 718–720.
66 F. M. Bayat, M. Prezioso, B. Chakrabarti, H. Nili, I. Kataeva and D. Strukov, *Nat. Commun.*, 2018, **9**, 2331.
67 D. Kessler, M. C. Lechmann, S. Noh, R. Berger, C. Lee, J. S. Gutmann and P. Theato, *Macromol. Rapid Commun.*, 2009, **30**, 1238–1242.
68 P. Kumbhare and U. Ganguly, *IEEE Trans. Electron Devices*, 2018, **65**, 2479–2484.
69 Q. Luo, X. Zhang, Y. Hu, T. Gong, X. Xu, P. Yuan, H. Ma, D. Dong, H. Lv, S. Long, Q. Liu and M. Liu, *IEEE Electron Device Lett.*, 2018, **39**, 664–667.
70 B. Tian, P. Nukala, M. B. Hassine, X. Zhao, X. Wang, H. Shen, J. Wang, S. Sun, T. Lin, J. Sun, J. Ge, R. Huang, C. Duan, T. Reiss, M. Varela, B. Dkhil, X. Meng and J. Chu, *Phys. Chem. Chem. Phys.*, 2017, **19**, 16960–16968.
71 M.-X. Jia, Z.-Q. Ren, Y.-D. Liu, Y. Cheng, R. Huang, P.-H. Xiang, X.-D. Tang, B.-B. Tian, N. Zhong and C.-G. Duan, *Appl. Phys. Lett.*, 2019, **114**, 102901.
72 N. Yang, Z. Q. Ren, C. Z. Hu, Z. Guan, B. B. Tian, N. Zhong, P. H. Xiang, C. G. Duan and J. H. Chu, *Nanotechnology*, 2019, **30**, 464001.
73 J. H. Park, D. S. Jeon and T. G. Kim, *ACS Appl. Mater. Interfaces*, 2017, **9**, 43336–43342.