PAPER

Interface chemistry and leakage current mechanism of HfGdON/Ge gate stack modulated by ALD-driven interlayer

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In current manuscript, a Ge metal-oxide-semiconductor (MOS) capacitor based on HfGdON/Ge gate stacks with an ALD-driven passivation layer has been fabricated, and its interfacial and electrical properties are compared with those of its counterparts that have not undergone passivation treatment. Electrical analyses revealed that the HfGdON/Al$_2$O$_3$/Ge MOS device exhibits improved performance, including larger permittivity, negligible hysteresis, reduced flat band voltage, good capacitance–voltage behavior, and lower interface state and border trapped oxide charge density. All of these improvements can be ascribed to the suppressed growth of unstable Ge oxides, thus reducing the defective states at or near the HfGdON/Ge interface and improving the interface quality. In addition, detailed analyses of the current conduction mechanisms (CCMs) for Ge MOS capacitors with different passivation treatment were investigated systematically.

1. Introduction

Germanium (Ge) has been attracting increasing attention as a channel material in metal-oxide-semiconductor field-effect transistors (MOSFETs), owing to its high carrier mobility, resulting in a large drive current, and small band gap for supply voltage scaling, as compared to the conventional Si channel material.[1–3] However, the absence of a high-quality MOS interface, such as the SiO$_2$/Si interface, has inhibited the development of Ge-based MOSFET devices, due to the volatility of GeO$_x$ species.[3,4] One important challenge associated with Ge-MOSFETs is the formation of native oxide on the Ge surface, resulting in an extremely high density of interface states (D_{it}) and Fermi-level pinning at the high-k/Ge interface. Therefore, achieving a high-quality and thermodynamically stable insulator on Ge needs to be realized for the successful application of Ge-based MOSFETs.

To address this issue, the use of different surface-passivation techniques on Ge substrates upon gate stack formation has been intensively explored to prevent the performance degradation of Ge-based MOSFETs, such as surface nitridation,[5] sulfur passivation,[6] high-quality epitaxial layer growth,[7] and the adoption of various passivation layers, *e.g.* GeO$_2$, SiO$_2$, and rare earth oxides.[8–10] However, nitridation treatment usually requires high temperatures, which limits the thermal budget. For sulfur passivation, the formation of large surface states in the Ge energy band gap renders elemental S passivation less desirable for high-performance MOSFET devices.[11] The adoption of low-k passivation layers, such as a few nanometer-thick GeO$_2$ and SiO$_2$, deteriorates device performance by increasing the equivalent oxide thickness (EOT). As a result, it can be concluded that although these processes have shown improvements in device performance, the D_{it} levels are still too high to make Ge channels a viable alternative to Si in the short term. The development of an alternative passivation process for the Ge surface is therefore required. In previous studies, a native-oxide-free interface has been detected in an atomic-layer-deposited (ALD) passivation layer,[12,13] which proves this method to be effective in guaranteeing good interface properties without increasing the EOT.

Due to their good thermal stability, suppressed formation of oxygen vacancies and suitable band offsets, HfGdON high-k gate dielectric materials have been attracting increasing attention for Ge-based MOSFETs.[14] Similar to other high-k gate dielectrics, a HfGdON gate dielectric layer directly deposited on Ge also exhibits anomalous characteristics with larger frequency dispersion, hysteresis, and also low effective mobility, originating from interface pinning induced by native oxides.[13] Therefore, pretreatment and the passivation of the Ge substrate prior to the Hf-based high-k gate dielectric deposition to minimize oxide formation and eliminate the Fermi level pinning effect is still necessary. The electrical properties of a HfGdON/Ge gate stack with an interface passivation layer have been

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previously reported.[14] However, observations of the evolution of the interface chemistry of Ge/HfGdON gate stacks, as well as the band alignment and electrical properties of Ge/HfGdON originating from an ALD-derived self-cleaning passivation layer, have not been fully identified yet. In the current work, the effect of an ALD-derived ultrathin Al_2O_3 and AlON passivation layer on the interfacial properties of HfGdON/Ge gate stacks was investigated systematically. For comparison, the evolution of the interfacial properties of a HfGdON/Ge gate stack without a passivation layer was also demonstrated. As a result, improved electrical properties have been achieved with a small gate leakage current, low interface state density, and high device reliability for the Ge-based MOS device.

2. Experimental

N-type Ge (100) wafers were cleaned in acetone for 5 min at 75 °C to remove organic contamination, followed by ethanol solution. They were then washed with a mixed solution (NH_3-·H_2O : H_2O_2 : H_2O = 2 : 1 : 7) for 5 min at room temperature. Then, the Ge wafers were dipped in 1% buffered HF solution to remove any native oxide on the surface and other impurity ions that had adhered to the surfaces of the wafers. After N_2 drying, the wafers were immediately transferred to an ALD system. Al_2O_3 and AlON ultrathin passivation layers of about 1 nm thick were deposited on the surface of the as-cleaned Ge substrates using a TMA precursor with a purity of 99.999%. Finally, HfGdON thin films were deposited on Ge wafers covered with different passivation layers by sputtering a HfGdO target (99.99%) in Ar/N_2 under ambient conditions. The film composition and chemical bonding states were investigated by X-ray photoelectron spectroscopy (XPS) measurements using an ESCALAB 250Xi system, equipped with an Al K_α radiation source (1487.6 eV), and all the collected data were corrected using the binding energy of the C 1s peak of 284.8 eV. To explore the electrical properties, Al/HfGdON/Al_2O_3(AlON)/Al MOS capacitors were fabricated by patterning the sputtering-driven Al-capped top electrode with a diameter of 300 μm *via* a shadow mask method, and a low-resistance ohmic contact was formed by sputtering Al on the backside of the wafer, followed by forming gas (H_2 5% + N_2 95%) annealing (FGA). An Agilent B1500A semiconductor parameter analyzer combined with Cascade Probe Station was used to measure the high-frequency (1 MHz) capacitance–voltage (C–V) and gate leakage current density *vs.* gate voltage (J_g–V_g) curves of the samples. All the electrical tests were carried out in a dark box at room temperature.

3. Results and discussion

To investigate the effect of the passivation layers on the interfacial properties of the HfGdON thin films, XPS measurements were carried out to examine the interfacial chemical state of the HfGdON/Ge stacks. As shown in Fig. 1a, for the sample with the Al_2O_3 passivation layer, two fitted peaks for Al 2p are located at binding energies of 74.8 and 74.4 eV, attributed to Al–O and Hf–Al–O bonding states.[15] When using the AlON passivation layer,

another peak located at 73.6 eV was detected, which corresponds to the Al–N bonds at the interfacial layer. The emergence of the Al–N bonds may be caused by passivation layer formation. It should be noted that no obvious Al–N bond formation between the HfGdON and Al_2O_3 layers was observed. Fig. 1b displays the evolution of Hf 4f spectra as a function of different passivation layers. Compared with the reported values of 16.2 and 17.8 eV for the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peaks of HfO_2, the binding energies corresponding to Hf 4f spectra demonstrate a slight shift towards higher values, indicating the formation of HfGdON films.[16] After passivation, the binding energies for the Hf 4f spectra shift towards lower values, which can be attributed to the formation of a HfAlO interfacial layer.

To further confirm the evolution of the interfacial chemical bonding states, much attention was paid to the Ge 3d and O 1s XPS spectra of HfGdON/Ge gate stacks with different passivation layers. In Fig. 2a, the two peaks located at the lower binding energies are attributed to the Ge substrate and the third one centered at 32.0 eV can be assigned to the GeON component.[17] However, for the Ge/HfGdON gate stack without a passivation layer, a new peak at 32.50 eV was observed, which is due to the Ge–O bond states, indicating that a GeO_2 interfacial layer is formed between the HfGdON sample and the Ge substrate.[17,18] After applying the AlON passivation layer, the intensity of the Ge–O bond decreases, indicating that the GeO_2 interfacial layer can be partly suppressed. It should be noted that no deleterious Ge–O bonding is detected for the sample with the Al_2O_3 passivation layer. The full removal of the GeO_2 interfacial component can be attributed to the ALD-derived Al_2O_3 passivation layer with self-cleaning effect. A similar phenomenon has been observed in our previous work.[19] Fig. 2b shows the O 1s core-level spectra of the HfGdON/Ge gate stack with different passivation layers. For the sample without a passivation layer, the four fitted peaks, located at binding energies of 529.7, 531.0, 531.9 and 532.4 eV, originate from the O–Hf, O–Gd, GeON and GeO_2 bonding states, respectively.[18,20] When inserting Al_2O_3 and AlON as a passivation layer, peaks located at 530.8 and 531.1 eV appear, which can be assigned to Hf–Al–O and O–Al (Gd). However, it is difficult to distinguish between the O–Gd and O–Al bonds, due to their similar binding energies (531.0 eV for Gd–O and 531.2 eV for Al–O).[21] The peak located at 532.4 eV disappears when the Al_2O_3 passivation layer is applied, indicating that the GeO_2 interfacial layer is effectively suppressed, which is in good agreement with previous Ge 3d spectra. As a result, it can be inferred that the HfGdON/Al_2O_3/Ge gate stack demonstrated optimized interface chemistry, and excellent CMOS device performance is expected.

In the application of high-k gate dielectrics to CMOS devices, the precise determination of the band offset (BO) is a major concern. It is critical to the success of a MOSFET containing a high-k gate dielectric that the BO between the high-k gate dielectric and the semiconductor is at least 1 eV. Based on the method proposed by Kraut et al.,[22] the valence band alignment (ΔE_v) of HfGdON/Ge gate stacks with different passivation layers could be determined by measuring the VB maximum (E_{VBM}) difference between the high-k stacks and the Ge substrate, as expressed by the following equation:
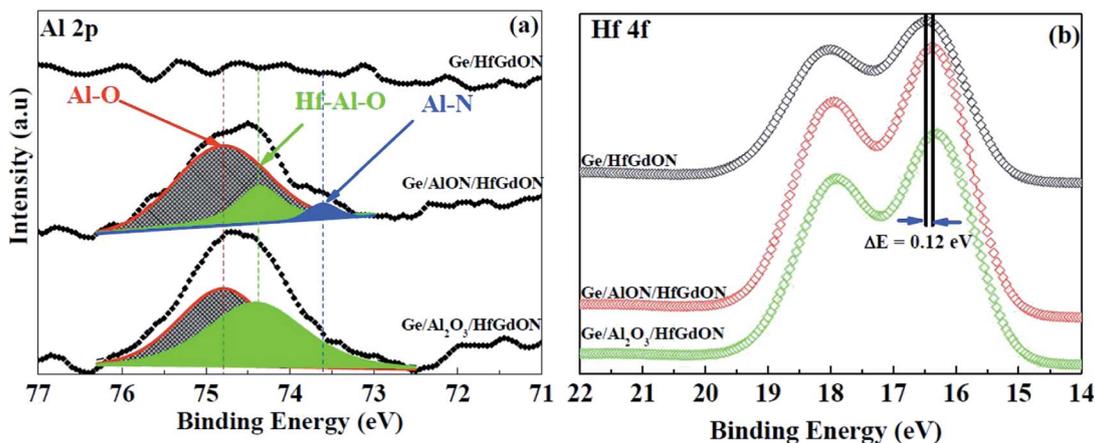
Fig. 1 Al 2p (a) and O 1s (b) core level spectra of HfGdON/Ge gate stacks with different passivation layers.

$$\Delta E_{\mathrm{v}} = E_{\mathrm{VBM}}^{\mathrm{stack}} - E_{\mathrm{VBM}}^{\mathrm{Ge}} \tag{1}$$

The ΔE_{v} values for the HfGdON/Ge heterojunctions with different passivation layers, shown in Fig. 3a, are calculated to be 0.86, 1.33 and 1.25 eV. The conduction band offset (ΔE_{c}) was obtained simply subtracting the valence band offset and the energy gap of the Ge substrate and HfGdON film. Taking into account the measured energy band gap of sputtering-deposited HfGdON (5.64 eV), together with the Ge energy band gap of 0.59 eV, ΔE_{c} of 3.72 eV was deduced for the AlON passivation layer, whereas 3.80 eV was obtained for the Al_2O_3 passivation layer, as demonstrated in Fig. 3b. An increase in ΔE_{c} was detected after Al_2O_3 passivation, which can be attributed to reduction in the interfacial layer. Based on Fig. 3b, it can be seen that the ΔE_{v} of the HfGdON/Ge gate stack without the passivation layer is only 0.86 eV, which cannot meet the primary requirements of high-k dielectrics. After inserting passivation layers, an increase in ΔE_{v} and ΔE_{c} was observed, which makes the HfGdON/Ge gate stacks with a passivation layer suitable for the fabrication of MOSFETs with a small leakage current induced by Schottky emission.[23]

Fig. 4a shows the typical high frequency (1 MHz) C–V characteristics of Ge MOS capacitors with and without a passivation layer. For the sample without passivation treatment, the existence of a relatively large hysteresis can be attributed to the active defects near the interface or in the bulk HfGdON film.[24] After passivation, negligible hysteresis was detected, implying improved interface quality and decreased interface state density in the dielectric and near or at the interface due to the reduced interface layer.[25] Suppressed low-k layer formation was thus achieved, which results in high accumulation capacitance compared to directly deposited HfGdON. In addition, the extracted positive flat band voltage (V_{FB}) indicates that the native defects/traps in the samples are negative. In contrast with the HfGdON/Ge and HfGdON/AlON/Ge samples, V_{FB} for the HfGdON/Al_2O_3/Ge gate stack shifts towards the negative direction and displays a smaller positive value, indicating the less negative trapped charges, which can be attributed to the reduced defect traps in the film and near the interface.[24] The effective dielectric constant (k), EOT, V_{FB}, hysteresis (ΔV_{FB}), and border trapped oxide charge density (N_{bt}) were extracted from the C–V curves and are listed in Table 1. Due to the suppressed
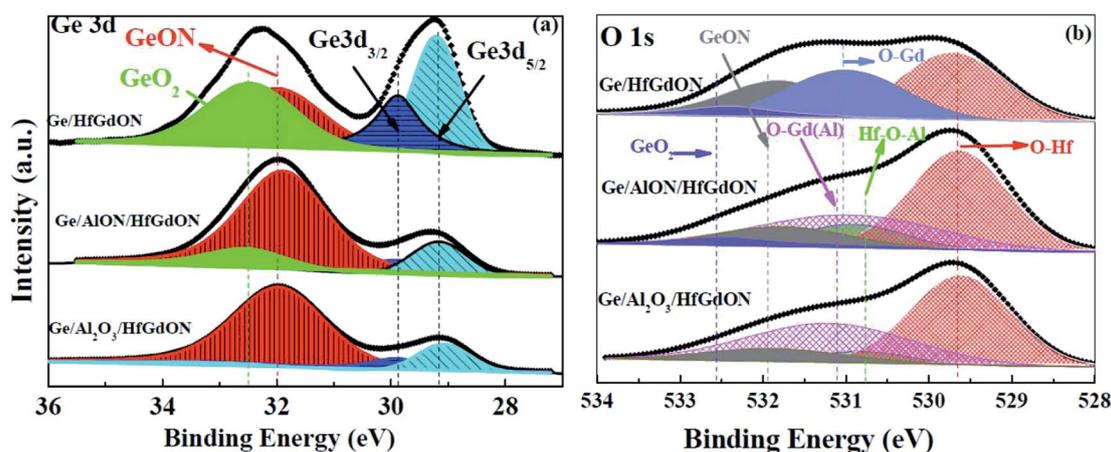

Fig. 2 Ge 3d (a) and O 1s (b) core level spectra of HfGdON/Ge gate stacks with different passivation layers.
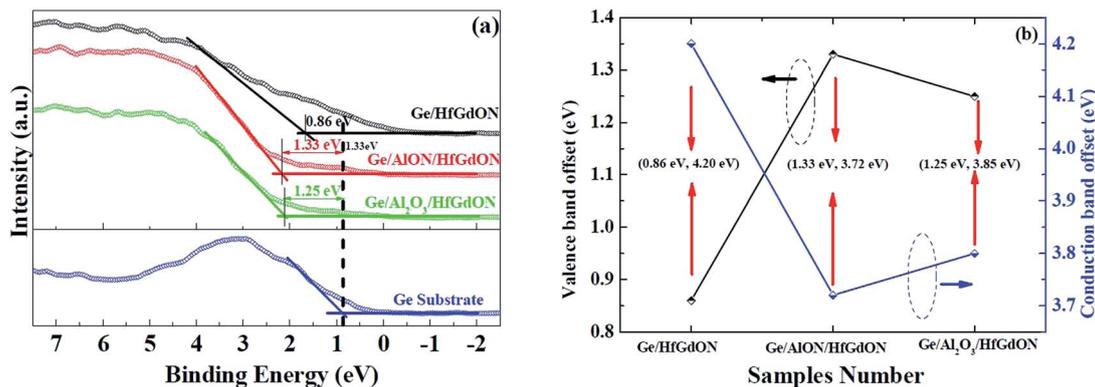
Fig. 3 (a) Valence-band spectra of the Ge substrate and HfGdON/Ge gate stacks with different passivation layers. (b) Determination of band offsets for HfGdON/Ge gate stacks with different passivation layers.

growth of the low-k interfacial layer, HfGdON/Al$_2$O$_3$/Ge achieves the larger k value of 35.70. For N_{bt}, reduction was observed after passivation. As a result, it can be concluded that the presence of the Al$_2$O$_3$ passivation layer helps the formation of a high-quality interface between HfGdON and Ge by reducing interface states and border traps and thus unpinning the Fermi level. Fig. 4b shows the current density–voltage (J–V) characteristics for samples with and without a passivation layer. The larger leakage current for the HfGdON/Ge sample may originate from the interface trap-assisted tunneling, because a high density of interface states exists at the high-k/Ge interface of the unpassivated samples.[24] Suppression of the gate leakage current by applying an Al$_2$O$_3$ passivation layer was clearly observed, which can be attributed to the suppressed interfacial layer growth, reduced oxygen-vacancy-related interface states, or the increased conduction band offset, leading to the reduced trap-assisted tunneling current.

To investigate the current conduction mechanisms (CCMs) of the Ge-based MOS capacitors with and without a passivation layer, several CCMs including Fowler–Nordheim (FN) tunneling, Schottky emission (SE), and Frenkel–Poole (PF) emission were explored. As we know, various CCMs occur in various electric fields, so it is complicated to determine the

Table 1 Parameters extracted from C–V curves

Samples	k	EOT (nm)	V_{FB} (V)	ΔV_{FB} (V)	N_{bt} (cm^{-2})
HfGdON/Ge	28.65	1.91	0.42	0.013	1.47×10^{11}
HfGdON/AlON/Ge	32.50	1.80	0.43	0.004	4.77×10^{10}
HfGdON/Al$_2$O$_3$/Ge	35.70	1.64	0.24	0.001	1.32×10^{10}

exact CCM. In the current work, CCMs were only evaluated under substrate injection.

SE is carrier transportation induced by thermionic emission, in which electrons obtain enough energy after thermal excitation to pass through the metal–dielectric barrier or the dielectric–semiconductor barrier to the dielectric. Based on the SE mechanism,[19] if SE is the dominant mechanism, $\ln(J/T^2)$ versus the $E^{1/2}$ should satisfy a linear relationship. Fig. 5a shows the good linear behavior of $\ln(J/T^2)$ vs. $E^{1/2}$, indicating that the dominant CCM is SE under substrate injection in a low electric field of 0.16–0.64 MV cm^{-1}. Based on the linear fitting, the optical dielectric constant ε_r and the refractive index n have been calculated to be (5.78, 2.40), (3.86, 1.96) and (5.07, 2.25) for substrate injection, corresponding to HfGdON/Ge, HfGdON/AlON/Ge and HfGdON/Al$_2$O$_3$/Ge, respectively. All the obtained
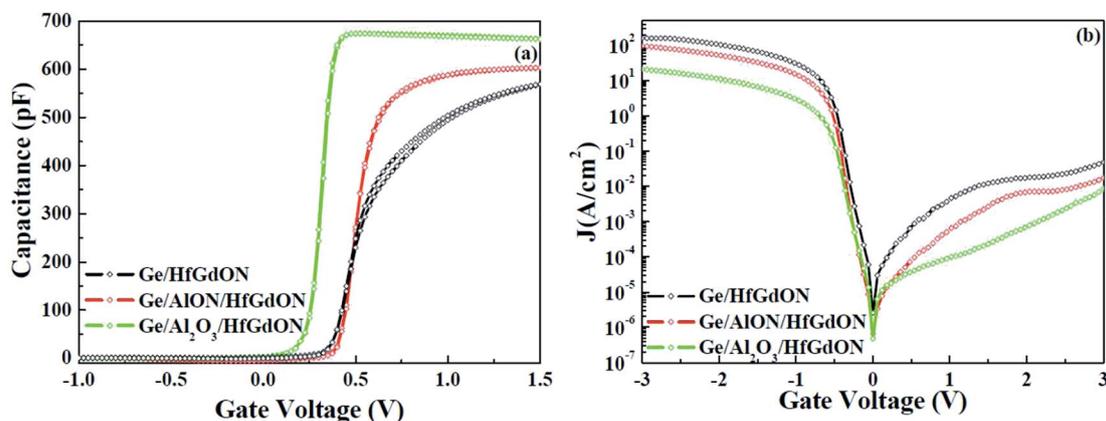

Fig. 4 C–V and J–V characteristics of Ge-based MOS capacitors with different passivation layers.
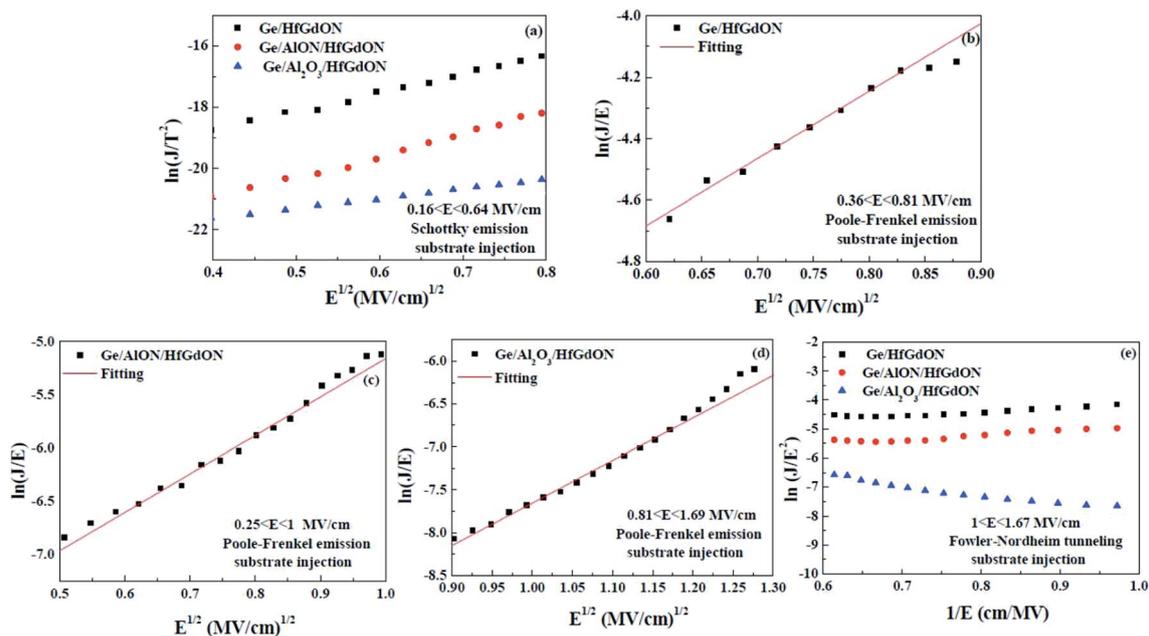
Fig. 5 (a) SE, (b−d) PF emission, and (e) FN tunneling plots for Ge-based MOS capacitor with different passivation layers under substrate injection at room temperature.

ε_r and n values are in good agreement with the reported results, suggesting that the SE emission dominates the CCM under substrate injection in a low electric field.[26,27] Fig. 5b–d present $\ln(J/E)$ vs. $E^{1/2}$ of the three samples for the substrate injection at room temperature. According to the theoretical expressions for the PF mechanism,[28] $\ln(J/E)$ should be proportional to $E^{1/2}$. From the slope of the linear plots, the values of the dielectric constant of the HfGdON films (ε_{ox}) are determined to be 18.9, 31, and 58.85 for the unpassivated, Al_2O_3-passivated, and AlON-passivated samples, respectively. It should be noted that the ε_{ox} value of 58.85 is far from being a reasonable value for the AlON-processed sample. As a result, it can be concluded that the PF emission is the dominant CCM for the unpassivated and Al_2O_3-passivated samples in a medium-strength electric field, whereas this is not the case for the AlON-passivated sample. Normally, in the high electric field regions, the dominant CCM is governed by FN tunneling, which follows the linear relation of $\ln(J/E^2)$ versus $1/E$.[25] Fig. 5e displays $\ln(J/E^2)$ vs. $1/E$ for the three samples at high field regions. The linear relation of $\ln(J/E^2)$ vs. $1/E$ indicates FN tunneling through the HfGdON oxide layer under substrate injection under a high electric field of 1–1.67 MV cm^{-1} at room temperature. According to the previous analysis, it can be concluded that with the increases of the electric field, the dominant CCM change is from SE to FN tunneling and/or PF emission.

4.   Conclusion

In this work, the effects of an ALD-driven passivation interlayer on the interfacial defect states and electrical properties of Ge-based MOS capacitors with a HfGdON gate dielectric have been investigated. Electrical measurements confirm that the HfGdON/Al_2O_3/Ge MOS device demonstrates improved performance, including the largest dielectric constant of 35.70, negligible hysteresis, and lower interface state density and border trapped oxide charge density. XPS investigations reveal that the ALD-derived Al_2O_3 interlayer with self-cleaning effect can effectively suppress the formation of unstable native oxides, and also reduce the oxide traps at and near the high-k/Ge interface, thus leading to the excellent electrical performance for the Ge-based MOS device. The CCM analyses, including SEs, PF emissions and FN tunneling, measured at room temperature, were discussed systematically. As a result, it can be inferred that the ALD-driven Al_2O_3 interlayer possesses optimized interface chemistry and improved electrical performance, highlighting its potential as a promising passivation candidate for the next generation of Ge-based MOSFET devices.

Conflicts of interest

The authors declare no competing financial interest.

Acknowledgements

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