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Low temperature atomic layer deposition of zirconium oxide for inkjet printed transistor applications†

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We report the growth of zirconium oxide (ZrO_2) as a high- k gate dielectric for an inkjet-printed transistor using a low-temperature atomic layer deposition (ALD) from tetrakis(dimethylamido)zirconium (TDMAZr) and water precursors. All the samples are deposited at low-temperature ranges of 150–250 °C. The films are very uniform with RMS roughness less than 4% with respect to their thickness. The atomic force microscopy (AFM) shows a significant change in surface morphology from tapered posts to undulating mountain-like structures with several hundreds of ALD cycles. The results from X-ray diffraction (XRD) analysis exhibit an amorphous to the crystalline structure with temperature variation, which is independent of the thickness of the films. All our samples are hydrophilic as contact angles are less than 90°. The capacitance–voltage (C – V) and conductance–voltage (G_p/ω – V) characteristics of ZrO_2 dielectrics for silicon metal–oxide–semiconductor (MOS) capacitors are studied for different temperatures. For the n-type substrate MOS capacitors, the dielectric constants are estimated to be 7.5–11. Due to the low deposition temperature, a hydrophilic surface, and high k value, the ALD- ZrO_2 dielectric can be compatible for printed transistors. The processes of fabrication and characterization of inkjet-printed graphene transistors is demonstrated using the ZrO_2 dielectric. The possible solvents, surfactant, and the dielectric induced modifications in graphene flakes are demonstrated by Raman spectra. The graphene flakes spread uniformly on the ZrO_2 surface. The functional inkjet-printed graphene transistor characteristics are demonstrated to illustrate the field effect behavior with the ALD- ZrO_2 dielectric.

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1 Introduction

Inkjet printing has emerged as a popular technology for printed electronics.¹ It has many advantages, such as low material wastage, the ability of large area fabrication, a limited number of process steps, low cost, and compatibility with many substrates.^{2,3} Inkjet printed technology for device fabrication is still in its infancy, although significant developments have been reported in printing transistors, memory devices, solar cells, organic light emitting diodes (OLEDs), and sensors.^{4–8} Printed transistors require thin, uniform, and stable gate dielectrics for robust control of the drain current at low temperature.

However, the coffee ring effect on printed patterns causes more flakes aggregation in the perimeter than the center of the defined region.⁹ Consequently, a thick dielectric layer and a high gate voltage are required to introduce field effect behaviors in printed top and back-gated transistors.^{4,10,11} The solution-processed dielectrics are easy to use for printed transistors as they can be deposited at low-temperatures on flexible substrates.¹² Yet, the application of solution-processed dielectrics are limited due to their instability under electrical stress, low film density after evaporation, and adsorption of contaminants from ambient.¹³

The atomic layer deposition (ALD) being a highly smooth, conformal, uniform growth process, could be a promising method of dielectric deposition for inkjet printed transistors.¹⁴ ALD grown materials are used as a buffer layer in flexible transistors, high- k dielectrics, encapsulation layer, for thin film coating, and composite materials.^{15–19} For the bottom-gate coplanar graphene transistors, a surface with contact angle 70–90° is desirable for better adhesion between graphene and underlying dielectric.²⁰ Zirconium oxide (ZrO_2) as a high- k dielectric material can be suitable for inkjet printed transistors for its relatively hydrophobic properties.²¹ Previously, inkjet

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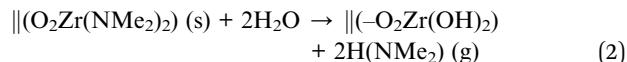
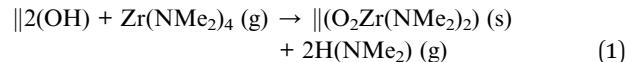
printed carbon nanotube transistor was demonstrated using solution-processed ZrO_2 dielectric.²⁰ However, thermally annealed, solution-processable ZrO_2 had high leakage current, and required UV-curing for proper functioning.^{22,23} The chemical vapor deposition of ZrO_2 from zirconium *tert*-butoxide requires very high temperatures (380–825 °C).²⁴ Even pulse laser deposition of ZrO_2 requires high deposition temperatures (400–600 °C) or high-temperature treatment to promote crystallinity.^{25,26} The ZrO_2 deposited from metal amide precursors can be a potential high- k dielectric for printed and flexible electronics because of their low ALD temperature window (250–350 °C) which many flexible substrates can sustain.^{27–29} The ALD- ZrO_2 from TDMAZr precursor was successfully deposited on graphene and nitrogen doped carbon nanotube (NCNT) nanoflakes to study the nanocomposite materials.^{30,31} The encapsulation layer properties for OLEDs, and dielectric properties on the gallium nitride (GaN) substrate using ZrO_2 from TDMAZr precursor was studied before, but the details of growth kinetics on silicon (Si) are still lacking.^{32–34} All these depositions were limited to 100 cycles and did not include dielectric properties.^{27,33,34} Our study investigates the growth kinetics, orientation, growth saturation, and dielectric properties of ZrO_2 using atomic layer deposition (ALD) from TDMAZr and water precursors. The trend of our contact angle on the ZrO_2 surface with temperature was opposite to the trend shown in ref. 33. We validated and discussed our observations in context of surface roughness and surface chemistry in details. Furthermore, we demonstrated the step-by-step method of fabricating and characterizing printed graphene transistor using ZrO_2 dielectric.

2 Experimental section

2.1 ZrO_2 growth process

The ZrO_2 was deposited using a plasma-enhanced atomic layer deposition (PEALD) reactor (Arradiance Gemstar-6 XT-P) on heavily n-doped silicon (100) substrate after hydrofluoric acid (HF) precleaning followed by nitrogen (N_2) dry for one minute. The substrates were put into the chamber immediately. Purge times were greater than five seconds to avoid non-self-limiting or CVD like growth or multilayer physisorption.²⁷ To find out the conditions of growth saturation, the pulse and purge times were kept constant. TDMAZr was held at 80 °C to provide sufficient Zr precursor vapors in the reactor. Manifold heaters were heated at 115 °C to avoid precursor condensations. Argon was used as the carrier gas and the ALD reactor was kept at 45 mTorr pressure. One ALD cycle was completed with the following steps: (a) a 400 ms dose of TDMAZr, (b) a 20 s purge of excess TDMAZr and byproducts using 100 sccm argon flow, (c) a 50 ms dose of H_2O , and (d) a 20 s argon purge of excess water and byproducts. The depositions were carried out at 150, 200, and 250 °C up to 400 cycles. The ZrO_2 films were characterized using ellipsometer (Wollam M2000), atomic force microscopy (Bruker dimension ICON AFM), X-ray diffraction (Rigaku SmartLab X-ray diffractometer), CV analyzer (Keithley 590), and tensiometer (Falcon, First Ten Angstroms, Inc., Portsmouth,

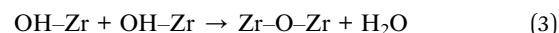
VA) respectively. The following half-reactions were proposed inside the ALD reactor with TDMAZr and water precursors²⁷



$\|$ indicates the surface of the sample. The schematic of the reactions is shown in Fig. S1 (see ESI†).

2.2 Results and discussion

The thickness of ZrO_2 films was measured using an ellipsometer. The thickness of ZrO_2 films changes linearly up to 400 cycles at different temperatures, unless it is diverged at 250 °C as shown in Fig. 1a. At the ALD temperature window (250 °C for TDMAZr precursor), this aberration is expected and observed between 300–400 cycles. Only 2.05 nm was grown over 100 cycles in that region. We further deposited ZrO_2 up to 600 cycles (not shown) at 250 °C and the maximum thickness was 24.71 nm. We conclude that the growth is initially linear with the number of cycles and gets saturated after 300 cycles at the ALD temperature window. The growth per cycle (GPC) is a crucial parameter to predict the film growth at different temperatures. The GPC for ZrO_2 was 0.133, 0.107, and 0.084 nm at 150, 200, and 250 °C respectively. The GPC decreases linearly with an increase of the deposition temperatures. The GPC was 0.64 times lower at 250 °C compared to GPC at 150 °C. This decline of GPC is caused by the increasing desorption of –OH groups with higher temperatures. The dehydroxylation for ALD- ZrO_2 can be described as follows:³⁵



As the film thickness and GPC have linear relations with the number of cycles and temperatures, the deposition rate is highly tunable in atomic scale. The hydrofluoric acid (HF) pretreatment of substrate induces a hydrophobic –H terminated surface on silicon.³⁶ In our case, it is reasonable to believe an atomic layer starts growing from the very first cycle, and the large number of –OH nucleation sites on the silicon surface are created during the first water pulse of the ALD process. At all the deposition temperatures, ALD- ZrO_2 followed a similar growth process *i.e.* layer-by-layer growth mode. At 250 °C, the absence of –OH sites are responsible for growth saturation which will be explained in later section.

For device applications, surface irregularity can influence adhesion and transport properties.³⁷ The surface topology of the films was studied using atomic force microscopy (AFM). The RMS surface roughness curves in Fig. 1b, show linear trends at 150 and 200 °C. However, at first, the roughness rises slightly and then reduces with the number of cycles at 250 °C. This discrepancy in roughness is the result of static adatoms and the presence of residual Zr precursor ligands due to incomplete reaction at low temperatures. At 250 °C, the adatoms are more



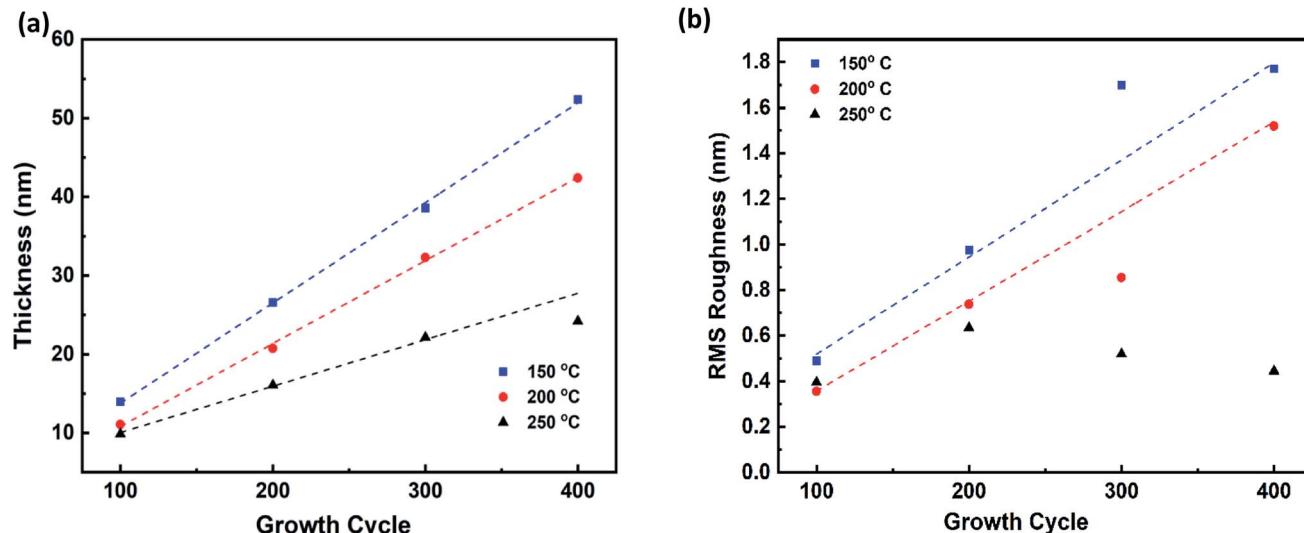


Fig. 1 (a) Ellipsometer thickness of ZrO_2 at different temperatures and number of cycles, (b) RMS roughness of ZrO_2 from AFM measurements.

mobile and the Zr and O ions occupy the positions with the lowest free energy of the crystal.³³ The surfaces are highly smooth as the roughness is less than 4% of the corresponding film thickness. The 3D surface topography of ZrO_2 films at 150 °C is shown in Fig. 2 using an AFM scanned area of 500 × 500 nm². Fig. 2a and b appear like tapered posts. The facets of the crystallites are more visible in Fig. 2c. The surface of Fig. 2d looks like hillocks with multiple valleys between them. These peaks are responsible for the highest surface roughness (1.77 nm) among all the samples, and a clear indication of precursor agglomeration at low temperature as the thermal energy during film growth was not enough to remove the zirconium precursor ligands completely.

The film thickness is a crucial factor in determining the crystal structure and phase of ZrO_2 .³⁸ For 150 and 200 °C, the thickness of the films was deliberately kept high to study the role of thickness on crystallinity. The X-ray diffraction (XRD) measurements were performed in ALD- ZrO_2 films of thickness 63, 46.4, and 22.3 nm for temperatures 150, 200, and 250 °C respectively. Fig. 3a shows the XRD spectra at various temperatures. At a low temperature (150 °C), the structure is amorphous as no noticeable peak is found in the XRD pattern. As the temperature increases, a sharp peak starts appearing in the angular position (2θ) of 33°. The intensity of the peak increases at higher temperatures. At 200 °C, a mixture of amorphous and crystalline states is present in the thin film. Nonetheless,

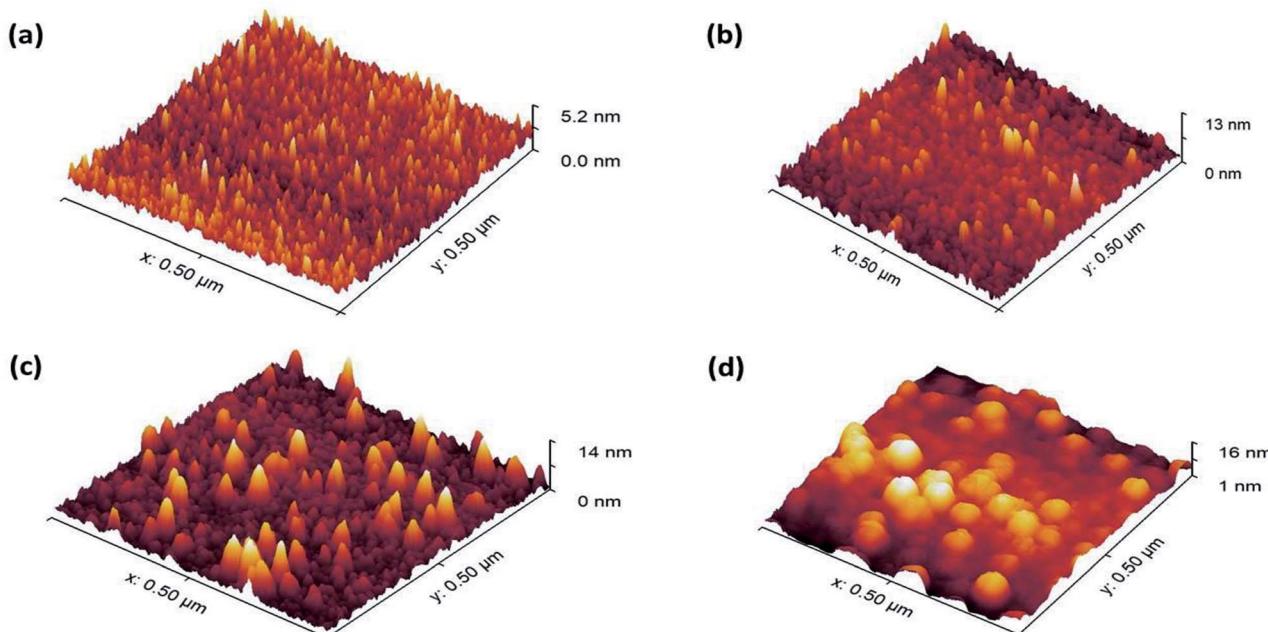


Fig. 2 AFM surface images at 150 °C for growth cycles- (a) 100, (b) 200, (c) 300, (d) 400.

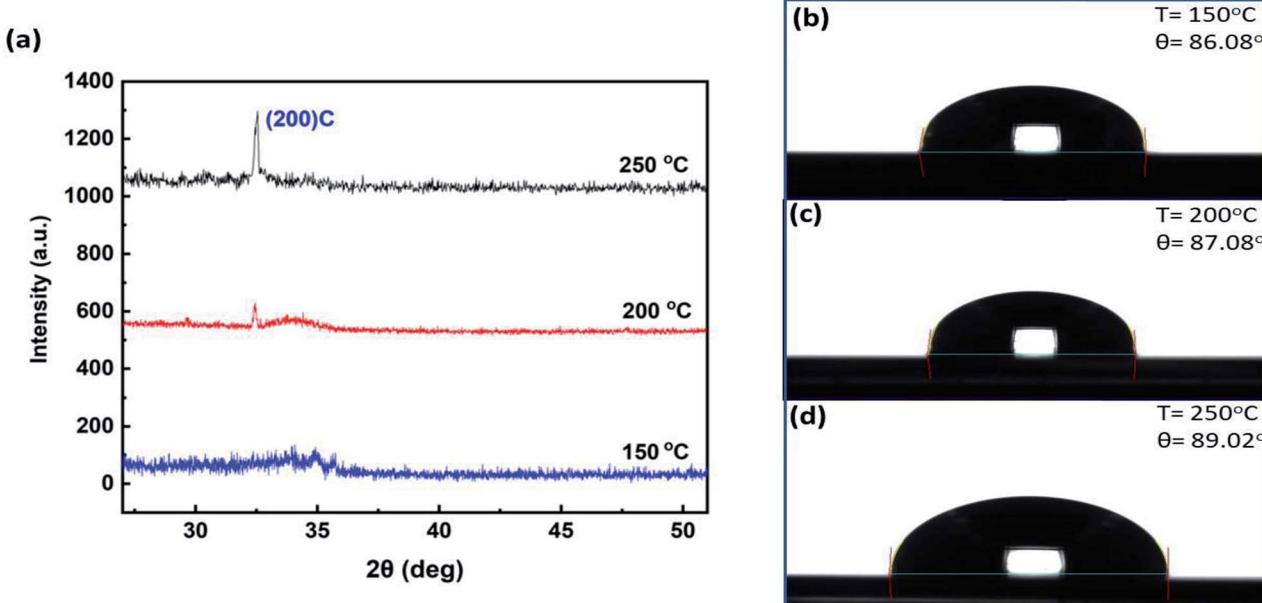


Fig. 3 (a) XRD patterns of ZrO_2 at different temperatures. Measured contact angles on ZrO_2 for 400 cycles at: (b) $150\text{ }^{\circ}\text{C}$, (c) $200\text{ }^{\circ}\text{C}$, (d) $250\text{ }^{\circ}\text{C}$.

a sharp peak at $250\text{ }^{\circ}\text{C}$ in XRD pattern reveals the crystalline state of the deposited ZrO_2 . The peaks of XRD patterns can be indexed as (200) plane with cubic phase structure. Along with deposition, the crystallinity of ZrO_2 is highly tunable from amorphous to crystalline phase with temperature alteration. Instead of the film thickness, the temperature is the crucial factor for crystallinity of ALD- ZrO_2 . The temperature influences the surface mobility of adatoms, reaction mechanism, and the number of nucleation sites. High temperatures promote the dehydroxylation, desorption, surface adatoms mobility and ordering of the structures with minimum surface energy which in turn reduce surface roughness. These phenomena lead to the crystalline structure of solids. With specific temperature provided, less surface roughness indicates more crystalline structure. Fig. S2 in the ESI† shows the variations of 2D surface topology with temperatures. The energy-dispersive spectra (EDS) confirms the presence of Zr, O, Si, and reveals no chemical contamination on the films (see ESI Fig. S3†).

A hydrophilic surface is expected to print an ink using an inkjet printer. To determine the hydrophilicity of our samples, we performed contact angle tests using water droplets as shown in Fig. 3b-d. As the contact angles are less than 90° , the surfaces are hydrophilic in general. As the temperature increased, the films showed more hydrophobic characteristics. Therefore, selection of proper deposition technique for ZrO_2 is critical because hydrophobic ZrO_2 by magnetron sputtering process was reported elsewhere.²¹ Our observations *i.e.* increase of contact angle with temperature, are quite opposite to the study of ref. 33 where a significant decrease of contact angles with temperature elevation was reported. Our claim can be refuted from the surface roughness, and dehydroxylation phenomena at higher temperatures. Water easily spreads on a hydroxylated surface. The $-\text{OH}$ groups promote the hydrogen bonds with water, thus reducing the contact angle. Higher temperature

leads to more dehydroxylation which reduces $-\text{OH}$ nucleation sites on the deposition surface. Consequently, the deficiency of $-\text{OH}$ sites increases the contact angles. Due to dehydroxylation at $250\text{ }^{\circ}\text{C}$, there is a scarcity of $-\text{OH}$ bonds and the surface is nearly hydrophobic. This also strengthens the claim that the absence of $-\text{OH}$ groups are responsible for the growth saturation in 300–400 cycles at $250\text{ }^{\circ}\text{C}$. The desorption effect is dependent on the deposition temperature as well as the time for which the processes were carried out. At $250\text{ }^{\circ}\text{C}$, the $-\text{OH}$ nucleation sites were created during the water pulses of the ALD process. It is also true that a few $-\text{OH}$ groups can stick to the growth surface at $250\text{ }^{\circ}\text{C}$. This high temperature increases the surface adatoms mobility and reorganizes the Zr–O structures based on the minimum surface energy. There should be less defect on the crystalline ALD- ZrO_2 with reduced number of $-\text{OH}$ sites available for nucleation. As the process at $250\text{ }^{\circ}\text{C}$ was carried out for 300–400 cycles (almost 5 hours), the $-\text{OH}$ groups get released (desorbed) from the surface. For longer process time, the absence of $-\text{OH}$ nucleation sites are responsible for the growth saturation.

The roughness of a surface can be related to the contact angle by Wenzel's theory,³⁹ $\cos(\theta_A) = r \cos(\theta_C)$, where θ_A is the apparent contact angle on a rough surface, θ_C is the contact angle on a smooth surface, r is the roughness factor which is the ratio of the real surface area to the projected surface area. According to Wenzel's relation, surface roughness makes the hydrophilic surface more hydrophilic, and the hydrophobic surface more hydrophobic. The roughness, real and projected surface area, and roughness factors are extracted from AFM measurements as shown in Table 1. As roughness factors are less than 1.5, Wenzel's relation is reasonable to apply in our case.⁴⁰ As our samples are hydrophilic, roughness makes them more hydrophilic following Wenzel's statement. For 400 cycles, the roughness increases with temperature lowering, which

Table 1 Surface roughness relation with contact angles is determined from AFM and tensiometer measurements

Temperature (°C)	Roughness, R_q (nm)	Real surface area (nm ²)	Projected surface area (nm ²)	Roughness factor, r	θ_A (deg)	θ_C (deg)
250	0.446	252 012	250 000	1.008	89.02	89.03
200	1.52	255 146	250 000	1.020	87.08	87.13
150	1.77	256 834	250 000	1.027	86.63	86.72

enhances the real surface area and surface energy. Therefore, the surface turns more hydrophilic. Table 1 summarizes the relation between temperature, roughness, roughness factor, and contact angles.

The dielectric properties of ZrO_2 are studied by capacitance–voltage and parallel conductance–voltage characteristics at 100 kHz. The ALD- ZrO_2 films were deposited on n-type Si wafers with the resistivity of 0.01–0.02 Ω cm. To evaluate the influence of the temperature on dielectric constant and interface traps, the oxide thicknesses were kept nearly identical such as 23.14, 21.17, and 22.3 nm for temperatures of 150, 200, and 250 °C respectively. The normalized C – V curves shown in Fig. 4a were obtained using a mercury probe. The capacitor area was 7.4×10^{-4} cm². The C – V curves have distinguishable accumulation, depletion, and inversion regions. Dielectric constants (k) estimated from the electrical measurements are 7.5 (150 °C), 10.85 (200 °C), and 11 (250 °C) respectively. Due to crystallinity at higher temperatures, the dielectric constants improved about 1.46 times. Our observation of k value is lower, but consistent with the expected value of k for ZrO_2 *i.e.* 10–25.⁴¹ For the device structures, the k -values were consistent with our reported dielectric constants. Ellipsometry is very sensitive to interfacial oxide, and we did not observe any signature of SiO_x growth in our ellipsometry data. All our mean-square-error (MSE) values were less than 5. The breakdown field of the ALD- ZrO_2 was ~ 1 MV cm^{−1}. We also examined the hysteresis behavior of the ALD- ZrO_2 dielectric in Fig. S4 (see ESI†). The CV curves show a small hysteresis. Low hysteresis means there exists a good quality of ALD- ZrO_2 dielectric/Si semiconductor interface. This low hysteresis is either due to the charge trapping in the ZrO_2 or defect in the channel layer. Interestingly, the optical band gap calculated from the ellipsometer was fixed approximately at 4.82 eV for all our samples irrespective of the deposition temperatures, number of cycles, and crystal structure.

The conductance–voltage (G_p/ω – V) characteristics of MOS capacitors are shown in Fig. 4b. Conductance curves can be utilized to calculate the interface state density using the Hill–Coleman method as following:⁴²

$$N_{ss} = \frac{2}{qA} \frac{\frac{G_{m,\max}}{\omega}}{\left(\frac{G_{m,\max}}{\omega C_{ox}}\right)^2 + \left(1 - \frac{C_m}{C_{ox}}\right)^2} \quad (4)$$

where A is capacitor area, $G_{m,\max}$ is the peak value of measured capacitance, C_m is the corresponding measured capacitance, and C_{ox} is the capacitance of insulation layer in the strong accumulation layer. The calculated interface trap densities are 9.23×10^{13} (150 °C), 6.15×10^{13} (200 °C), and 5.95×10^{13} (250

°C) eV^{−1} cm^{−2} respectively. The interface traps are highest at 150 °C because of the defects in the ZrO_2 films as the Zr precursor ligands did not remove completely, which is evident in the C – V curve flat-band shift. The interface traps at 200 and 250 °C are in the same order of magnitude reported for thermally evaporated hafnium oxide which was cured at 350 to 450 °C.⁴³ The traps in ZrO_2 can be reduced using doping or high temperature treatment after the deposition.^{44,45} Our goal is to use the ALD- ZrO_2 for printed electronics, so all our samples were as-deposited. To avoid high interface traps and growth saturation, subsequent depositions of ZrO_2 for device fabrication were carried out at 200 °C.

2.3 Device fabrication

The details of graphene ink preparation, optical absorption spectrum, and Raman spectra are discussed in the ESI (Fig. S5†). The reliability of a gate dielectric depends on its ability to modulate the drain current and provide low gate leakage. Fig. 5a and b show the schematic and microscopic image of the bottom gate coplanar transistor structure with ALD- ZrO_2 dielectric and inkjet printed graphene. The heavily doped n-type Si (100) wafer was used as the back-gate as well as the substrate. A ZrO_2 dielectric layer of 46.4 nm thick was deposited at 200 °C. The source (S) and drain (D) electrodes were printed using silver nanoparticle ink (Novacentrix, Metal-on® JS-B40G) followed by a thermal curing at 150 °C for 30 min. The printed silver developed a well-defined pattern on ZrO_2 which was confirmed from the microscopic and SEM images. The silver adhered to the ZrO_2 surface quite well as depicted in Fig. 5b. The width of the source and drain electrodes was 258.33 μm and the channel length was 113.33 μm . Multiple printing passes (12 times) of the graphene ink were performed to create a percolation cluster between source and drain terminals. For 12 printing passes, the average thickness of the printed graphene layers was approximately 53 nm. This satisfies the percolation threshold of printed graphene thickness of 25 nm for back-gated device.¹¹ The graphene ink was prepared using terpineol and cyclohexanone solvents which are polar solvents. Using polar solvents, it is difficult to print a regular pattern on a hydrophobic surface. In a hydrophobic surface, they either form small droplets in the defined region, or the pattern collapses during curing. Despite the nearly hydrophobic behavior of the surfaces, we printed and cured graphene on the ZrO_2 surface successfully. Fig. 5c shows the SEM image of the graphene percolating network. The projected area has good coverage with crumpling graphene flakes.

Fig. 5d depicts the output (I_d versus V_d) characteristics of the printed graphene transistor for several values of V_g . The gate



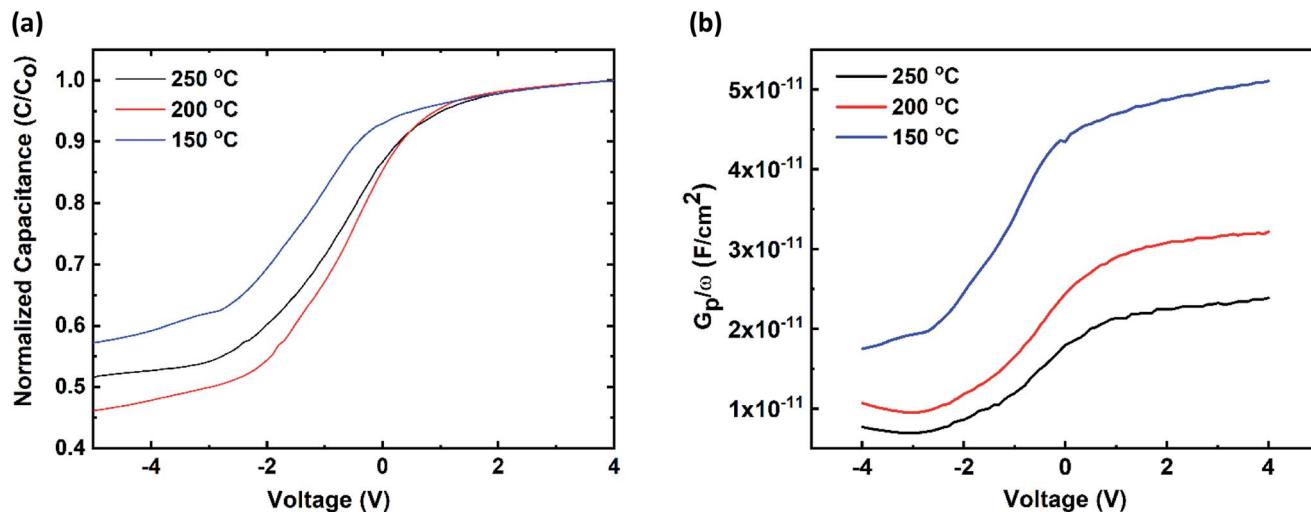


Fig. 4 (a) Capacitance–voltage behaviors of Hg/ZrO₂/Si-n (100) MOS capacitor, (b) G_p/ω curves at different voltages.

voltage was changed from 0.5 to -1.5 V with a decrement of -0.5 V. The drain voltage also varied from 0 to -2 V for each value of V_g . The drain characteristics are linear. The trace of $I_d - V_d$ goes higher as the gate bias changes from positive to more negative. As I_d increases with negative V_g , the transistor is of p-type. At $V_d = -2$ V, the drain current changes from -5.85 to -7.17 μ A for a V_g variation of 2 V. This implies that the field-effect behavior due to the application of voltage on a thin ZrO₂ layer is distinguishable from the output characteristics.

Transfer characteristics of printed graphene transistor is shown in Fig. S6 (see ESI†). Transfer characteristics were measured at the drain bias of -1 , -1.5 , and -2 V respectively. The gate–source leakage current (I_{sg}) was very small (less than 20 nA). The drain current I_d increases as the gate voltage goes from positive to negative. The charge neutrality (Dirac) point was outside of our measurement range. The unintentional doping may obscure the Dirac point in our measurement range. However, the gate modulation is well pronounced in the

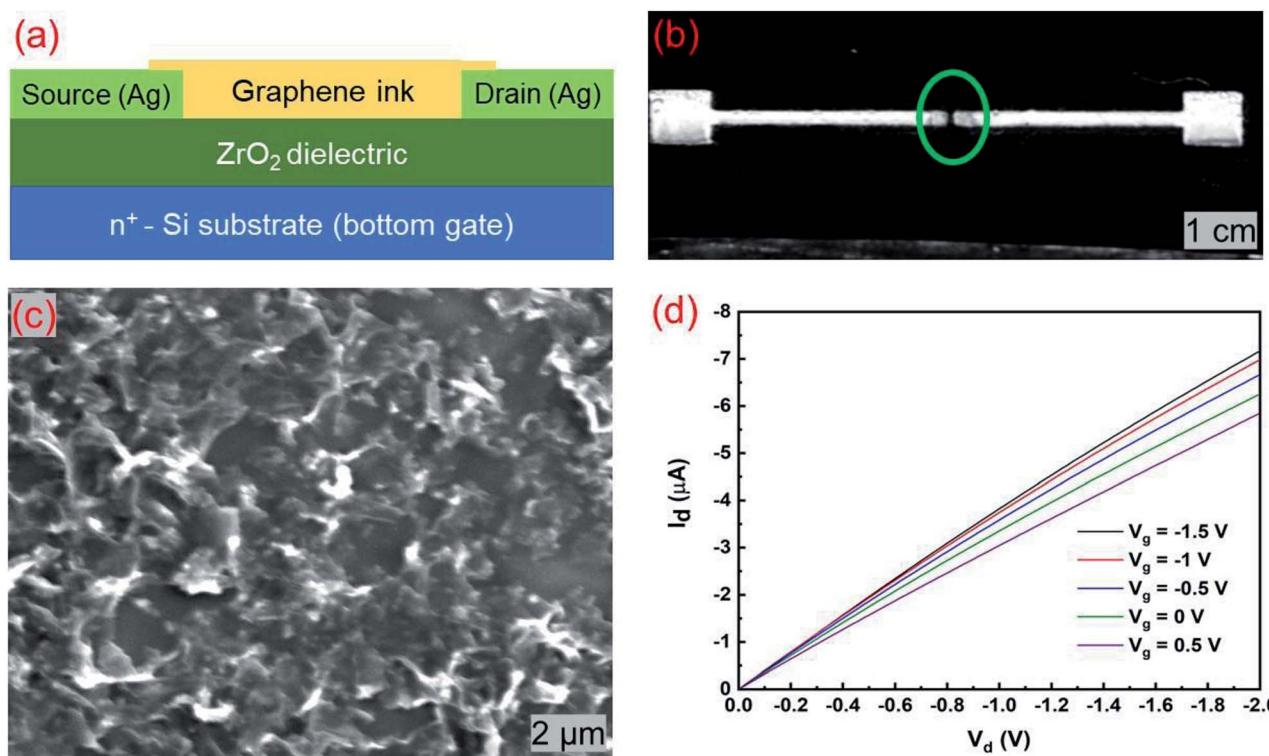


Fig. 5 (a) Schematic of bottom-gate coplanar transistor, (b) microscopic image of printed graphene transistor, (c) SEM image of printed graphene, and (d) output characteristics of an inkjet-printed graphene transistor.

transfer characteristics at different drain biases. At $V_d = -2$ V, a current ON/OFF ratio of 1.46 is obtained from Fig. S6 in the ESI.[†] It is well-known that graphene does not have a band gap (zero band gap) and its transistor never turns off. So, it is unlikely to get a perfect off state and ON/OFF switching behavior from a graphene transistor. Small ON/OFF ratio and non-saturation are problems with all inkjet printed graphene transistors, due to the absence of bandgap in graphene. The effective mobility μ can be derived from the slope of the transfer characteristics using $\mu = (L \times g_m / W \times C_{ox} \times V_d)$, where L (113.33 μm) and W (258.33 μm) are channel length and width, C_{ox} is the gate capacitance (≈ 200 nF cm^{-2}), and $g_m = dI_d/dV_g$ is the transconductance (0.887 μS). The estimated device mobility is ≈ 1 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. For our graphene transistor, the current ON/OFF ratio and mobility is lower than the printed graphene transistor reported in ref. 11 but higher than the one reported in ref. 10. However, our results are still comparable to other inkjet printed graphene transistors.⁴⁶ Therefore, the ALD grown thin oxide layers are suitable for low-voltage inkjet printed transistors.

3 Conclusion

A comprehensive study on growth kinetics and dielectric properties of the ALD-ZrO₂ is conducted from TDMAZr precursor. Low-temperature growth of ZrO₂ was achieved along with low roughness and high dielectric constant for different growth conditions. Linear relations of thickness and roughness were observed with growth cycles at different temperatures. The ALD temperature window for Zr(NMe₂)₄ precursor was determined from the growth saturation for 400 cycles at 250 °C. The crystallinity, the cubic phase, and the orientation in the (200) direction were observed at higher temperatures from the XRD patterns. The interface traps are due the defects in the ZrO₂ films. In general, all our oxide surfaces were hydrophilic as the contact angles were less than 90°. The trend of contact angle change with temperature change is contrary to the previous report, and therefore opens a new venue for research in this direction. Graphene thin films of given patterns were deposited through inkjet printing on ZrO₂ successfully. No significant differences of inkjet printed graphene on ZrO₂ were noticed from Raman spectra. Finally, the printing of graphene transistors was realized using the bottom-gate coplanar structure with ZrO₂ gate dielectric. A printed graphene transistor with a current on-off ratio of 1.46 at $V_d = -2$ V was achieved.

Conflicts of interest

The authors declare no conflict of interest.

Acknowledgements

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