RSC Advances

PAPER

View Article Online
View Journal | View Issue

Cite this: *RSC Adv.*, 2019, **9**, 592

Suppression of GeO_x interfacial layer and enhancement of the electrical performance of the high-*K* gate stack by the atomic-layer-deposited AlN buffer layer on Ge metal-oxide-semiconductor devices

Chin-I. Wang,[a] Teng-Jan Chang,[a] Chun-Yuan Wang,[a] Yu-Tung Yin,[a] Jing-Jong Shyue,[b] Hsin-Chih Lin[a] and Miin-Jang Chen*[a]

Received 14th September 2018
Accepted 3rd December 2018

DOI: 10.1039/c8ra07652a

rsc.li/rsc-advances

For high-performance nanoscale Ge-based transistors, one important point of focus is interfacial germanium oxide (GeO_x), which is thermodynamically unstable and easily desorbed. In this study, an atomic-layer-deposited AlN buffer layer was introduced between the crystalline ZrO_2 high-*K* gate dielectrics and epitaxial Ge, in order to reduce the formation of interfacial GeO_x. The results of X-ray photoelectron spectroscopy and high-resolution transmission electron microscopy demonstrate that the AlN buffer layer suppressed the formation of interfacial GeO_x. Hence, significant enhancement of the electrical characteristics of Ge metal-oxide-semiconductor (MOS) capacitors was achieved with a two-orders-of-magnitude reduction in the gate leakage current, a 34% enhancement of the MOS capacitance, and a lower interfacial state density. The results indicate that the AlN buffer layer is effective in providing a high-quality interface to improve the electrical performance of advanced Ge MOS devices.

1. Introduction

Over the last decade, it has become increasingly difficult to improve the performance of silicon (Si) metal-oxide-semiconductor (MOS) field-effect transistors (FETs) *via* conventional device scaling. Due to high carrier mobility, germanium (Ge) and III–V compound MOSFETs have been regarded as very promising candidates for the further improvement of device performance and scaling.[1–4] However, the lack of high-quality and thermodynamically stable gate dielectrics is a major problem in implementing Ge and III–V semiconductors as the channel materials.[5–10] For Ge, it is difficult to suppress the formation of a low-*K* germanium oxide (GeO_x) interfacial layer (IL) at the high-*K* and Ge interface, which limits the minimum achievable equivalent oxide thickness.[11,12] In contrast to the SiO_2/Si system, interfacial GeO_x has been reported to be thermodynamically unstable.[5] The smaller conduction band offset at the GeO_x/Ge interface also results in an increase in the gate leakage current.[13] Therefore, it is essential to prevent the formation of interfacial GeO_x in high-performance Ge-based MOSFETs.[13,14]

Many methods have been used to passivate the defects and achieve a stable high-*K*/Ge interface, such as the use of ultrathin Si, high-quality Ge oxides, and rare-earth oxides (Y_2O_3, $SmGeO_x$, *etc.*).[6,15–17] One of the most widely used methods is the insertion of an Al_2O_3 buffer layer between the high-*K* oxide and Ge because of the high bandgap and good thermal stability of Al_2O_3.[18,19] Besides, it has been reported that nitrogen incorporation into GeO_x yields an improvement in the thermal stability and the dielectric constant.[20,21] However, an unstable GeO_x is usually formed at the Al_2O_3/Ge and Ge-oxynitride/Ge interfaces. Furthermore, the use of germanium nitride (Ge_3N_4 or GeN_x) as the gate dielectric and the buffer layer has been demonstrated to exhibit well-behaved capacitance–voltage characteristics.[22–25] This improvement in the electrical performance may be the result of the suppression of interfacial GeO_x because the preparation of the nitride does not involve the use of oxygen.

AlN is a good material for gate dielectrics and buffer layers because it has a higher dielectric constant than GeO_x, good chemical stability, and a wide bandgap of ~6.2 eV.[26–28] AlN thin films are conventionally prepared by chemical vapor deposition (CVD) and sputtering.[29,30] However, the typical deposition temperature for AlN prepared using CVD is greater than 700 °C,[31] which is unfavorable for the integration of semiconductor processing. Besides, it is difficult to deposit high-quality nanoscale thin films using sputtering.[32] Recently, atomic layer deposition (ALD) has been reported for the preparation of high-quality nanoscale AlN thin films at low temperatures.[26,31] In this paper, remote plasma ALD (RP-ALD) was used to deposit a nanoscale AlN buffer layer between the

[a]*Department of Materials Science and Engineering, National Taiwan University, Taipei, Taiwan. E-mail: mjchen@ntu.edu.tw*

[b]*Research Center for Applied Science, Academia Sinica, Taipei, Taiwan*

crystalline ZrO_2 high-*K* gate dielectrics and Ge. The interfacial GeO_x was suppressed by the AlN buffer layer, so the capacitance equivalent thickness (CET), the interfacial state density (D_{it}) and the gate leakage current (J_g) of Ge MOS capacitors were significantly improved.

2. Experiments

The gate stacks in MOS capacitors are plotted schematically in Fig. 1. A Ge epitaxial layer was grown by remote plasma chemical vapor deposition using GeH_4 at 375 °C on a highly-doped (0.001–0.003 Ω cm) *n*-type Si substrate. After pre-cleaning, the samples were immersed in dilute HF (1 min) and then rinsed with de-ionized water (30 s) for several cycles, in order to remove the native oxide on the Ge. The gate stacks, which were composed of ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2, were then immediately deposited by RP-ALD (Fiji, Ultratech) at 250 °C. Tetrakis(dimethylamino)zirconium (TDMAZ), trimethylaluminum (TMA), O_2 plasma, and N_2/H_2 plasma were respectively used as the precursors and reactants for Zr, Al, O, and N. A platinum (Pt) top electrode with an area of 3×10^{-4} cm^2 was deposited by radio-frequency sputtering, and then an aluminum (Al) back contact was then produced by thermal evaporation. Finally, all samples were annealed in a furnace at 450 °C in N_2 ambient for 30 minutes.

The chemical bonding in the gate stacks was determined by X-ray photoelectron spectroscopy (XPS) using Al Kα radiation at 1486.6 eV. The cross-sectional images of the gate stacks were observed using high-resolution transmission electron microscopy (HRTEM, Philips Tecnai F20 G2 FEI-TEM, 200 kV). The crystalline phases of ZrO_2 were measured by grazing incident angle X-ray diffraction (GIXRD) using Cu Kα radiation at an incident angle of 0.5°. The capacitance density *versus* voltage (*C*–*V*), the leakage current density *versus* voltage (*I*–*V*), and the conductance density *versus* the frequency (*G*–*f*) curves of the gate stacks were characterized using an Agilent B1500A semiconductor device analyzer at room temperature.

3. Results and discussions

Fig. 2 shows the Ge 3d XPS spectra of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks with and without the annealing treatment, which reveals the oxidation states of Ge. The XPS spectra can be decomposed into the peaks corresponding to the binding energies at 29.4 eV (Ge), 31.7 eV (GeO), 33.6 eV (GeO_2), and 30.9 eV (Ge–N).[19] The XPS spectra of the samples without the annealing treatment are shown in Fig. 2(a)–(c). The presence of the GeO oxidation state in the ZrO_2 sample (Fig. 2(a)) is attributed to the supply of oxygen from ZrO_2. Fig. 2(b) reveals that the interfacial GeO was suppressed in the Al_2O_3/ZrO_2 gate stack compared to that in the ZrO_2 sample, which can be deduced from the lower Gibbs free energy of Al_2O_3 than that of ZrO_2.[33] It can be seen in Fig. 2(c) that the AlN buffer layer led to the formation of Ge–N bonds, and the GeO oxidation states were almost absent in the AlN/ZrO_2 sample because oxygen was not involved during AlN deposition. The result also suggests that the diffusion of oxygen from ZrO_2 toward the interface was effectively blocked by the AlN buffer layer, and so the formation of interfacial GeO_x was suppressed. Moreover, Fig. 2(d)–(f) are the XPS spectra of the samples treated with the annealing process. As compared with Fig. 2(a) and (b), the annealing treatment gave rise to an increase in the GeO signals and the formation of GeO_2 oxidation states in the ZrO_2 and Al_2O_3/ZrO_2 gate stacks:[34]

$$2GeO \rightarrow GeO_2 + Ge$$

The decomposition of GeO into GeO_2 and Ge is ascribed to the lower Gibbs free energy of GeO_2 than that of GeO.[34] The outcome indicates that the annealing process facilitated the formation of interfacial GeO_x. Notice that no obvious interfacial GeO_x appeared in the XPS spectrum of the AlN/ZrO_2 gate stack as shown in Fig. 2(f). The result confirms again that the AlN buffer layer could effectively restrain oxygen diffusion during the ZrO_2 deposition and annealing processes.

The Al 2p XPS spectra of the Al_2O_3/ZrO_2 and AlN/ZrO_2 gate stacks are shown in Fig. 3. The Al–O bond (75.6 eV) was present in the Al_2O_3/ZrO_2 sample due to the introduction of the Al_2O_3 buffer layer. The Al 2p peak of the AlN/ZrO_2 sample was located near 74.6 eV, which is associated with the Al–N bond because AlN was substituted for the Al_2O_3 buffer layer.[35] Depositing ZrO_2 on the AlN buffer layer results in a slight shift in the Al 2p peak (~75 eV) from the standard Al–N bond at 74.6 eV toward the Al–O bond at 75.6 eV, indicating the partial oxidation of AlN.

The HRTEM images of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks are shown in Fig. 4. It is seen that the total physical thickness of all the samples was approximately 7.5 nm. The ZrO_2 layer featured a crystalline lattice in the images for all of the samples, which demonstrates that ZrO_2 was crystallized

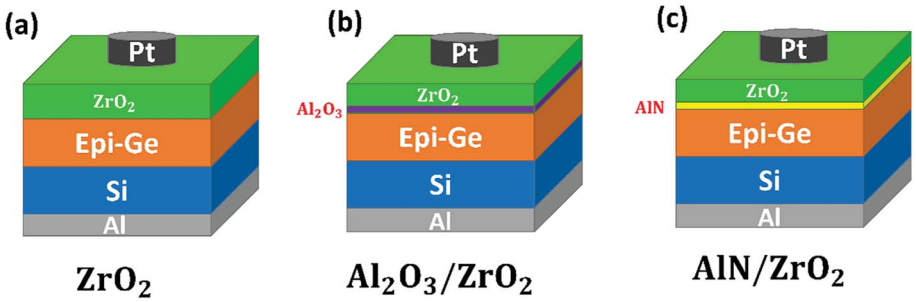

Fig. 1 Schematic of the (a) ZrO_2, (b) Al_2O_3/ZrO_2, and (c) AlN/ZrO_2 gate stacks.

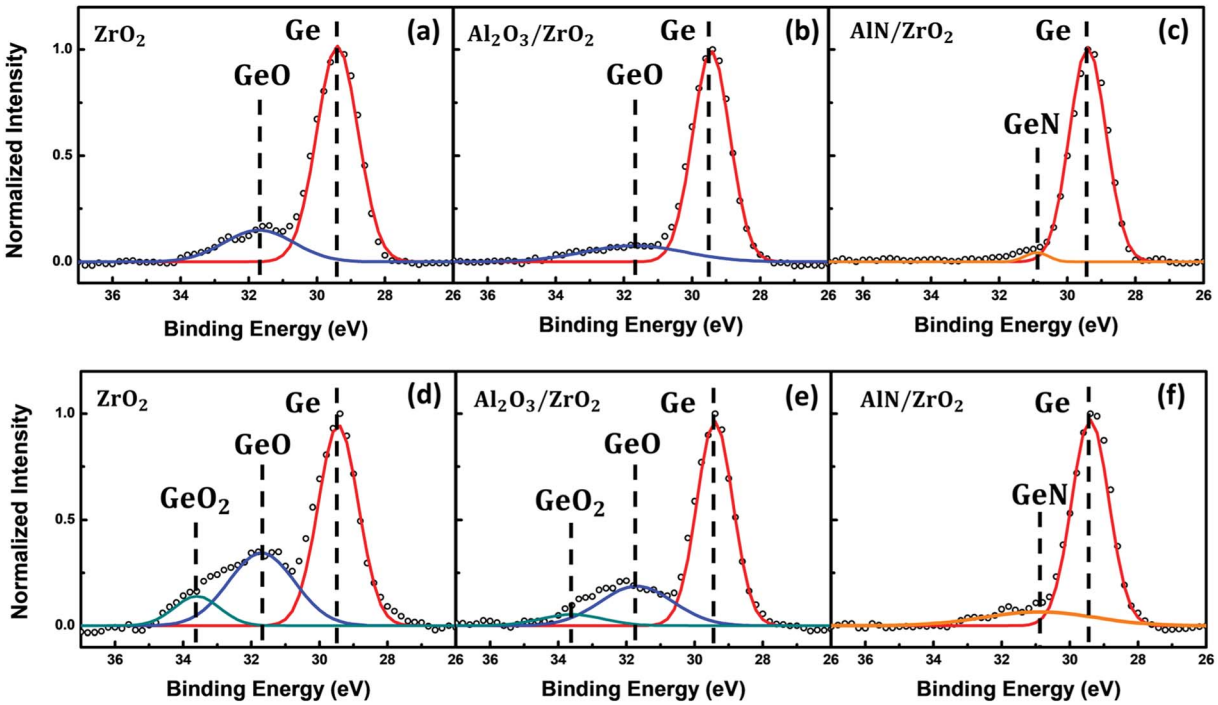

Fig. 2 The Ge 3d XPS spectra of the (a) ZrO_2, (b) Al_2O_3/ZrO_2, and (c) AlN/ZrO_2 gate stacks without the annealing treatment and the (d) ZrO_2, (e) Al_2O_3/ZrO_2, and (f) AlN/ZrO_2 gate stacks treated with the annealing process (in a furnace at 450 °C for 30 minutes in N_2 ambient). The intensity of the Ge peak of each sample was normalized to one. The annealing treatment facilitated the formation of interfacial GeO_x in the ZrO_2 and Al_2O_3/ZrO_2 gate stacks. The interfacial GeO_x was significantly suppressed in the AlN/ZrO_2 gate stack.

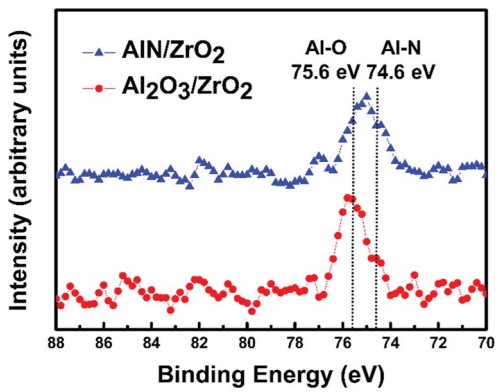

Fig. 3 Al 2p XPS spectra of the Al_2O_3/ZrO_2 and AlN/ZrO_2 gate stacks. The Al–O (75.6 eV) and Al–N (74.6 eV) bonds were present in the Al_2O_3/ZrO_2 and AlN/ZrO_2 samples.

during thermal annealing.[36] In Fig. 4(a), there is an obvious and rough interfacial GeO_x layer in the ZrO_2 sample. An Al_2O_3 buffer layer and interfacial GeO_x are observed in the Al_2O_3/ZrO_2 gate stack as shown in Fig. 4(b). Fig. 4(c) reveals a sharp interface without interfacial GeO_x between AlN and Ge, indicating that the AlN buffer layer was capable of suppressing interfacial GeO_x. The HRTEM results are in good agreement with the Ge 3d XPS spectra shown in Fig. 2.

The GIXRD patterns of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks are shown in Fig. 5. There is an obvious diffraction peak at $2\theta = 30.4^\circ$ in all of the samples, which corresponds to the tetragonal (101) phase (88-1007 JCPDS) or the cubic (111) phase (49-1642 JCPDS) of ZrO_2.[37] The tetragonal/cubic phase in ZrO_2 had a much higher dielectric constant than amorphous ZrO_2, which allows further CET scaling.[38] Although tetragonal/cubic ZrO_2 was thermodynamically stable at temperatures greater than 1170 °C,[39,40] the tetragonal/cubic phase had been observed in nanoscale ZrO_2 thin films.[41] The presence of tetragonal/cubic ZrO_2 in the nanoscale layers, as shown in Fig. 5, is consistent with the results of previous studies.[36,41]

The *C–V* curves of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks are shown in Fig. 6(a). The capacitance of the AlN/ZrO_2 sample was much greater than that of the ZrO_2 and Al_2O_3/ZrO_2 samples. Table 1 shows the CET and the effective dielectric constant (k_{eff}) of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks. These values were derived from the *C–V* curves. The CET and k_{eff} values of the ZrO_2 sample are 2.35 nm and 12.42 nm, respectively. The k_{eff} of the ZrO_2 sample is much lower than the dielectric constant of tetragonal/cubic ZrO_2,[42,43] which can be deduced from the presence of low-*K* interfacial GeO_x in the ZrO_2 sample, as shown in the XPS spectrum and the HRTEM image (Fig. 2(d) and 4(a)). Although the low-*K* interfacial GeO_x was suppressed by the Al_2O_3 buffer layer, as demonstrated by the XPS spectrum (Fig. 2(e)), the introduction of the Al_2O_3 buffer layer between ZrO_2 and Ge still caused a slight degradation of the CET (2.38 nm) and k_{eff} (12.29) of the Al_2O_3/ZrO_2 gate stack because Al_2O_3 has a lower dielectric constant than ZrO_2. The substitution of AlN for Al_2O_3 as the buffer layer led to a significant decrease in the CET (1.75 nm) and an increase in the k_{eff}

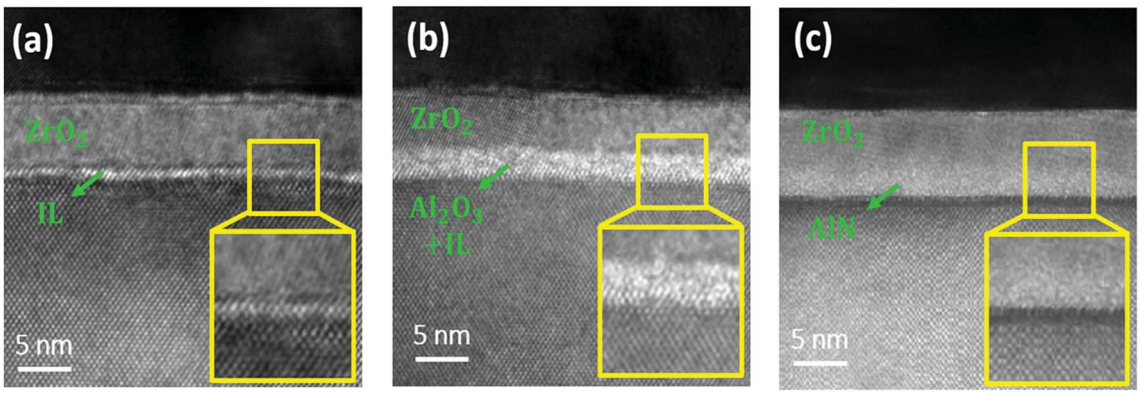

Fig. 4 Cross-sectional HRTEM images of the (a) ZrO_2, (b) Al_2O_3/ZrO_2, and (c) AlN/ZrO_2 gate stacks. There is a sharp interface between AlN and Ge in the AlN/ZrO_2 sample.

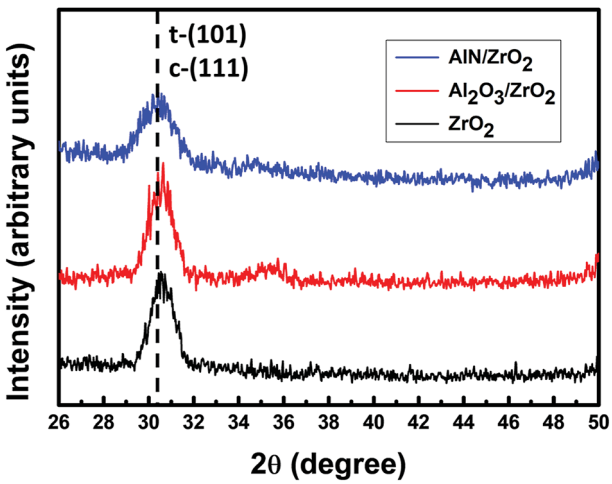

Fig. 5 GIXRD patterns of ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks. The obvious diffraction peak at $2\theta = 30.4°$ is associated with tetragonal/cubic ZrO_2.

(16.72) of the AlN/ZrO_2 sample, which is mainly attributed to the suppression of the interfacial GeO_x, as clearly shown in Fig. 2(f) and 4(c).

Fig. 6(b) and Table 1 show the I–V curves and the J_g of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks. The ZrO_2 sample had a high J_g value of 1.82×10^{-1} A cm^{-2} as a result of the leakage current path *via* the grain boundaries in crystalline ZrO_2. Due to the high bandgap of Al_2O_3, the presence of the Al_2O_3 buffer layer resulted in a decrease in the J_g (2.60×10^{-2} A cm^{-2}) of the Al_2O_3/ZrO_2 sample. There was a significant reduction in the J_g (1.12×10^{-3} A cm^{-2}) of the AlN/ZrO_2 gate stack, which is two orders of magnitude lower than that of the ZrO_2 sample because of the insertion of the AlN buffer layer. This can be understood from the suppressed growth of interfacial GeO_x, which has a low conduction band offset of only ~0.8 eV.[44]

The D_{it} value was measured by the conductance (Nicollian–Goetzberger) method.[45,46] Fig. 7(a) shows the equivalent parallel conductance over the angular frequency (G_P/ω) as a function of the frequency of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks. The value of D_{it} was estimated from the maximum value of G_P/ω as:[45]

$$D_{it} = \frac{2.5}{Aq}\left(\frac{G_P}{\omega}\right)_{max}$$

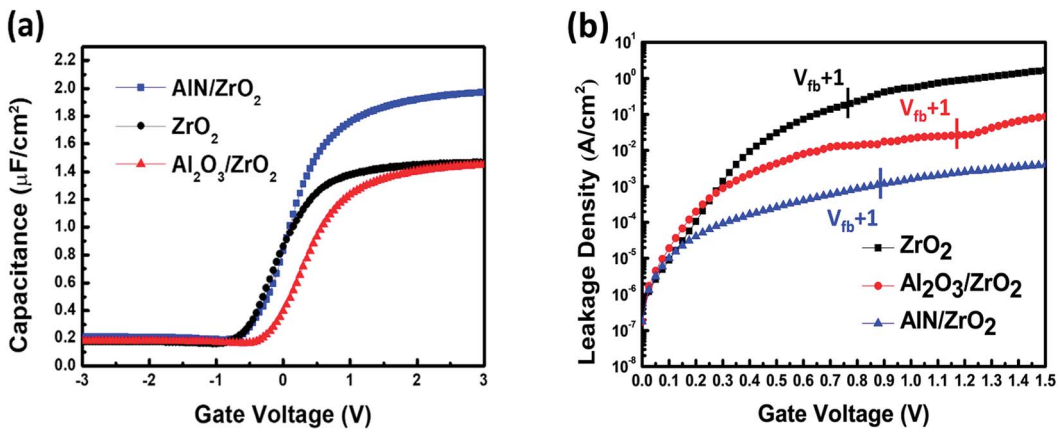

Fig. 6 (a) C–V and (b) I–V characteristics of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks. The AlN/ZrO_2 gate stack had a higher capacitance and a lower J_g than the ZrO_2 or Al_2O_3/ZrO_2 samples.

Table 1 The capacitance equivalent thickness (CET), the effective dielectric constant (k_{eff}), the gate leakage current (J_g), and the interfacial state density (D_{it}) of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks[a]

Sample	CET (nm)	k_{eff}	J_g (A cm^{-2})	D_{it} (cm^{-2} eV^{-1})
ZrO_2	2.35	12.42	1.82×10^{-1}	9.08×10^{12}
Al_2O_3/ZrO_2	2.38	12.29	2.60×10^{-2}	6.46×10^{12}
AlN/ZrO_2	1.75	16.72	1.12×10^{-3}	3.85×10^{12}

[a] These values were extracted from the *C–V*, *I–V*, and *G–f* curves as shown in Fig. 6 and 7. The leakage current density J_g was determined at V_{fb} (flat-band voltage) +1 V. The AlN/ZrO_2 gate stack exhibited a significant improvement in CET, k_{eff}, J_g, and D_{it} over the ZrO_2 and Al_2O_3/ZrO_2 samples.

where A is the area of the MOS capacitors. The D_{it} distributions in the bandgap of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks are shown in Fig. 7(b). Since the weak inversion response results in the overestimation of D_{it} for Ge at room temperature,[47] the minimum D_{it} values near the mid-gap were adopted to characterize the interfacial quality of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks.[48] As shown in Table 1, the minimum D_{it} of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 samples were 9.08×10^{12} cm^{-2} eV^{-1}, 6.46×10^{12} cm^{-2} eV^{-1}, and 3.85×10^{12} cm^{-2} eV^{-1}, respectively. Owing to the high thermal stability of the Al_2O_3 buffer layer and the reduced growth of interfacial GeO_x, the D_{it} of the Al_2O_3/ZrO_2 gate stack was lower than that of the ZrO_2 sample. The introduction of the AlN buffer layer caused a further decrease in D_{it} of the AlN/ZrO_2 gate stack, which is ascribed to the suppression of interfacial GeO_x by the AlN buffer layer. Because remote N_2/H_2 plasma was used as the reactant in the deposition of the AlN buffer layer, hydrogen passivation of the interfacial states also led to decrease in D_{it} of the AlN/ZrO_2 sample.[49]

The *C–V* curves of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks at various frequencies are shown in Fig. 8. In the frequency range from 1 kHz to 100 kHz, the frequency dispersion is 4.2%, 2.2%, and 1.4% for the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks at an accumulation bias of 2 V. The larger capacitance at a high frequency of 1 MHz was deduced from the parasitic inductance.[50] The relatively low-frequency dispersion in the AlN/ZrO_2 gate stack was correlated with the lower D_{it} as compared with the ZrO_2 and Al_2O_3/ZrO_2 samples.[51]

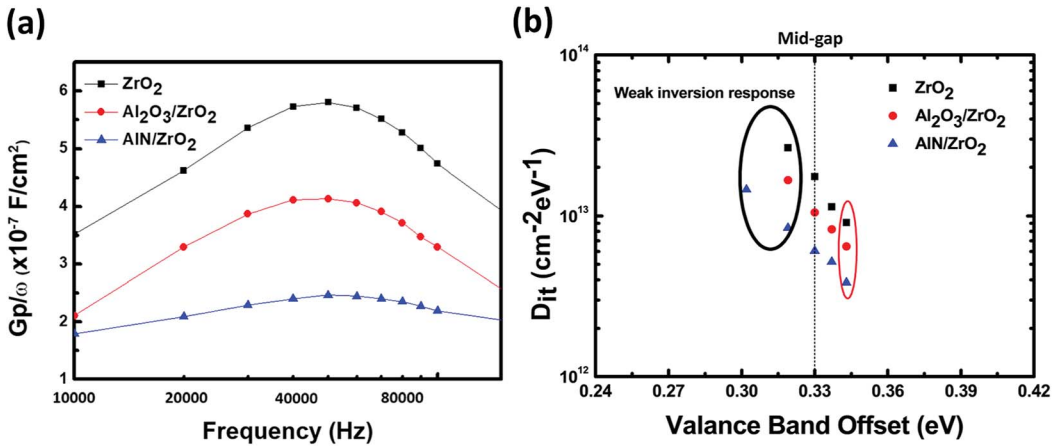

Fig. 7 (a) G_P/ω *versus* the frequency of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks. The AlN/ZrO_2 gate stack had the lowest value of $(G_P/\omega)_{max}$, and so the D_{it} of the AlN/ZrO_2 sample was lower than that of the ZrO_2 and Al_2O_3/ZrO_2 gate stacks. (b) D_{it} distributions *versus* bandgap energy, which were extracted from the conductance method, of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks.

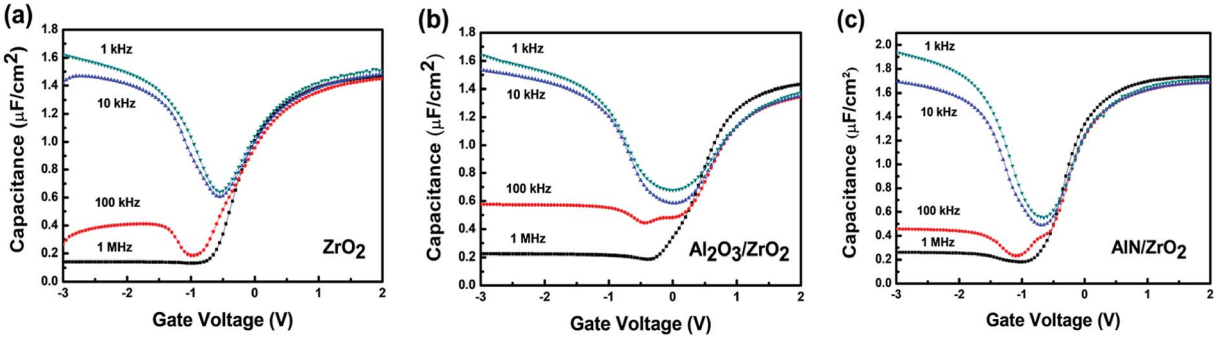

Fig. 8 The frequency dependence of the *C–V* curves of the (a) ZrO_2, (b) Al_2O_3/ZrO_2, and (c) AlN/ZrO_2 gate stacks. Low-frequency dispersion was observed in the AlN/ZrO_2 sample.

4. Conclusion

In this study, the electrical and structural characteristics of the ZrO_2, Al_2O_3/ZrO_2, and AlN/ZrO_2 gate stacks on Ge were investigated carefully. The introduction of an Al_2O_3 buffer layer between ZrO_2 and Ge resulted in a decrease of J_g value due to the high bandgap of Al_2O_3. However, it is difficult to prevent the growth of unstable, low-K interfacial GeO_x using an Al_2O_3 buffer layer because oxygen was involved during the deposition of Al_2O_3. The formation of interfacial GeO_x was significantly suppressed by an AlN buffer layer, as evidenced by the XPS and HRTEM characterizations. This produced a significant enhancement in the electrical characteristics, including the CET, k_{eff}, J_g, and D_{it} of the AlN/ZrO_2 gate stack. The results of this study show that an AlN buffer layer is an effective approach to high-quality interfacial engineering for high-performance high-K gate stacks in advanced Ge MOS transistors.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

The authors gratefully acknowledge the financial support of the Taiwan Semiconductor Manufacturing Company (TSMC) and the Ministry of Science and Technology (MOST 107-2622-8-002-018), Taiwan.

References

1 S. Takagi, *et al.*, *IEDM'03 Technical Digest*, IEEE International, 2003, pp. 3.3.1–3.3.4.
2 M. V. Fischetti and S. E. Laux, *J. Appl. Phys.*, 1996, **80**(4), 2234–2252.
3 K. Saraswat, C. O. Chui, T. Krishnamohan, D. Kim, A. Nayfeh and A. Pethe, *Mater. Sci. Eng., B*, 2006, **135**(3), 242–249.
4 S. Takagi, M. Noguchi, M. Kim, S.-H. Kim, C.-Y. Chang, M. Yokoyama, *et al.*, *Solid-State Electron.*, 2016, **125**, 82–102.
5 K. Prabhakaran, F. Maeda, Y. Watanabe and T. Ogino, *Appl. Phys. Lett.*, 2000, **76**(16), 2244–2246.
6 Y. Seo, T. I. Lee, C. M. Yoon, B.-E. Park, W. S. Hwang, H. Kim, *et al.*, *IEEE Trans. Electron Devices*, 2017, **64**(8), 3303–3307.
7 G. He, X. Chen and Z. Sun, *Surf. Sci. Rep.*, 2013, **68**(1), 68–107.
8 G. He, J. Gao, H. Chen, J. Cui, Z. Sun and X. Chen, *ACS Appl. Mater. Interfaces*, 2014, **6**(24), 22013–22025.
9 G. He, B. Deng, H. Chen, X. Chen, J. Lv, Y. Ma, *et al.*, *APL Mater.*, 2013, **1**(1), 012104.
10 G. He, J. Liu, H. Chen, Y. Liu, Z. Sun, X. Chen, *et al.*, *J. Mater. Chem. C*, 2014, **2**(27), 5299–5308.
11 Q. Xie, S. Deng, M. Schaekers, D. Lin, M. Caymax, A. Delabie, *et al.*, *Semicond. Sci. Technol.*, 2012, **27**(7), 074012.
12 J. Zhang, G. He, L. Zhou, H. Chen, X. Chen, X. Chen, *et al.*, *J. Alloys Compd.*, 2014, **611**, 253–259.
13 V. Afanas'ev and A. Stesmans, *Appl. Phys. Lett.*, 2004, **84**(13), 2319–2321.
14 Y. Fukuda, K. Kato, H. Toyota, T. Ono, Y. Nagasato and T. Ueno, *Jpn. J. Appl. Phys.*, 2006, **45**(9S), 7351.
15 R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka and S. Takagi, *Appl. Phys. Lett.*, 2011, **98**(11), 112902.
16 P. Zimmerman, *et al.*, *IEDM'06*, IEEE International, 2006, pp. 1–4.
17 C.-C. Lin, Y.-H. Wu, C.-Y. Wu and C.-W. Lee, *IEEE Electron Device Lett.*, 2014, **35**(3), 384–386.
18 S. Iwauchi and T. Tanaka, *Jpn. J. Appl. Phys.*, 1971, **10**(2), 260.
19 R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka and S. Takagi, *IEEE Trans. Electron Devices*, 2012, **59**(2), 335–341.
20 C. O. Chui, F. Ito and K. C. Saraswat, *IEEE Electron Device Lett.*, 2004, **25**(9), 613–615.
21 C. O. Chui, F. Ito and K. C. Saraswat, *IEEE Trans. Electron Devices*, 2006, **53**(7), 1501–1508.
22 T. Maeda, T. Yasuda, M. Nishizawa, N. Miyata, Y. Morita and S. Takagi, *Appl. Phys. Lett.*, 2004, **85**(15), 3181–3183.
23 T. Maeda, M. Nishizawa, Y. Morita and S. Takagi, *Appl. Phys. Lett.*, 2007, **90**(7), 072911.
24 Y. Otani, Y. Itayama, T. Tanaka, Y. Fukuda, H. Toyota, T. Ono, *et al.*, *Appl. Phys. Lett.*, 2007, **90**(14), 142114.
25 G. V. Rao, M. Kumar, T. Rajesh, D. R. K. Reddy, D. Anjaneyulu, B. Sainath, *et al.*, *Materials Today: Proceedings*, 2018, **5**(1), 650–656.
26 Y. J. Lee, *J. Cryst. Growth*, 2004, **266**(4), 568–572.
27 A. Ahmed, A. Rys, N. Singh, J. Edgar and Z. Yu, *J. Electrochem. Soc.*, 1992, **139**(4), 1146–1151.
28 M. Morita, S. Isogai, K. Tsubouchi and N. Mikoshiba, *Appl. Phys. Lett.*, 1981, **38**(1), 50–52.
29 X.-H. Xu, H.-S. Wu, C.-J. Zhang and Z.-H. Jin, *Thin Solid Films*, 2001, **388**(1–2), 62–67.
30 A. C. Jones, C. R. Whitehouse and J. S. Roberts, *Chem. Vap. Deposition*, 1995, **1**(3), 65–74.
31 D. Riihelä, M. Ritala, R. Matero, M. Leskelä, J. Jokinen and P. Haussalo, *Chem. Vap. Deposition*, 1996, **2**(6), 277–283.
32 P. Kelly and R. Arnell, *Vacuum*, 2000, **56**(3), 159–172.
33 G. Thompson, P. Skeldon, X. Zhou, K. Shimizu, H. Habazaki and C. Smith, *Aircr. Eng.*, 2003, **75**(4), 372–379.
34 S. Kai Wang, H.-G. Liu and A. Toriumi, *Appl. Phys. Lett.*, 2012, **101**(6), 061907.
35 P. Motamedi and K. Cadien, *Appl. Surf. Sci.*, 2014, **315**, 104–109.
36 J.-J. Huang, L.-T. Huang, M.-C. Tsai, M.-H. Lee and M.-J. Chen, *Appl. Surf. Sci.*, 2014, **305**, 214–220.
37 C. Zhao, S. Taylor, M. Werner, P. Chalker, R. Murray, J. Gaskell, *et al.*, *J. Appl. Phys.*, 2009, **105**(4), 044102.
38 D. Vanderbilt, X. Zhao and D. Ceresoli, *Thin Solid Films*, 2005, **486**(1–2), 125–128.
39 J. Robertson, *Rep. Prog. Phys.*, 2005, **69**(2), 327.
40 S. Bang, S. Lee, S. Jeon, S. Kwon, W. Jeong, S. Kim, *et al.*, *J. Electrochem. Soc.*, 2008, **155**(9), H633–H637.
41 C. Scanlan, M. Gajdardziska-Josifovska and C. Aita, *Appl. Phys. Lett.*, 1994, **64**(26), 3548–3550.
42 Y.-H. Wu, L.-L. Chen, R.-J. Lyu, M.-Y. Li and H.-C. Wu, *IEEE Electron Device Lett.*, 2010, **31**(9), 1014–1016.
43 R. Hegde, D. Triyoso, S. Samavedam and B. White Jr, *J. Appl. Phys.*, 2007, **101**(7), 074113.

44 J. Robertson and R. M. Wallace, *Mater. Sci. Eng., R*, 2015, **88**, 1–41.
45 R. Engel-Herbert, Y. Hwang and S. Stemmer, *J. Appl. Phys.*, 2010, **108**(12), 124101.
46 E. H. Nicollian, J. R. Brews and E. H. Nicollian, *MOS (metal oxide semiconductor) physics and technology*, Wiley, New York, 1982.
47 K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, *et al.*, *IEEE Trans. Electron Devices*, 2008, **55**(2), 547.
48 C.-C. Hsu, W.-C. Chi, Y.-H. Tsai, M.-L. Tsai, S.-Y. Wang, C.-H. Chou, *et al.*, *J. Vac. Sci. Technol., B*, 2018, **36**(5), 051204.
49 A. Nayfeh, C. O. Chui, K. C. Saraswat and T. Yonehara, *Appl. Phys. Lett.*, 2004, **85**(14), 2815–2817.
50 C.-M. Lin, H.-C. Chang, I.-H. Wong, S.-J. Luo, C. Liu and C. Hu, *Appl. Phys. Lett.*, 2013, **102**(23), 232906.
51 F. Ji, J. Xu, P. Lai, C. Li and J. Liu, *IEEE Electron Device Lett.*, 2011, **32**(2), 122–124.