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Graphene–Si CMOS oscillators†

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Graphene field-effect transistors (GFETs) offer a possibility of exploiting unique physical properties of graphene in realizing novel electronic circuits. However, graphene circuits often lack the voltage swing and switchability of Si complementary metal–oxide-semiconductor (CMOS) circuits, which are the main building block of modern electronics. Here we introduce graphene in Si CMOS circuits to exploit favorable electronic properties of both technologies and realize a new class of simple oscillators using only a GFET, Si CMOS D latch, and timing RC circuit. The operation of the two types of realized oscillators is based on the ambipolarity of graphene, *i.e.*, the symmetry of the transfer curve of GFETs around the Dirac point. The ambipolarity of graphene also allowed to turn the oscillators into pulse-width modulators (with a duty cycle ratio ~1 : 4) and voltage-controlled oscillators (with a frequency ratio ~1 : 8) without any circuit modifications. The oscillation frequency was in the range from 4 kHz to 4 MHz and limited only by the external circuit connections, rather than components themselves. The demonstrated graphene–Si CMOS hybrid circuits pave the way to the more widespread adoption of graphene in electronics.

1 Introduction

The development of graphene electronic circuits is mostly guided by the state-of-the-art circuit design of Si transistor technology. Such circuits try to exploit very large mobility[1] and saturation velocity[2] of charge carriers in graphene to match the performance of the corresponding Si circuits. However, this approach has not yielded satisfactory results so far because graphene does not have a bandgap[3–5] and therefore graphene field-effect transistors (GFETs) exhibit insufficient drain current saturation[6,7] and cannot be turned off. For instance, graphene ring oscillators[8] can indeed match the speed of the Si CMOS ring oscillators but only at the expense of considerable static power dissipation, which is unacceptable in highly-integrated digital circuits.[9] If graphene were to find applications in electronics, its unique properties, such as flexibility,[10] transparency,[11] and ambipolarity,[3] should be exploited to achieve either novel functionality or the same functionality with fewer transistors, rather than to mimic Si circuits. One of the truly unique electronic properties of graphene not exhibited by conventional semiconductors is ambipolarity. The ambipolarity of graphene has been used in the past to realize very simple logic gates[12] and frequency multipliers.[13] However, the logic gates suffered from large power dissipation and the mixers from large conversion loss, rendering both types of circuits unusable in realistic applications.

Here we demonstrate a novel class of graphene–Si CMOS circuits that exploit the ambipolarity of graphene to simplify the circuit and provide additional functionality. To illustrate the concept, we experimentally demonstrate two types of simple oscillators comprising just a GFET, a Si CMOS D latch, and a timing RC circuit. The D latch provides switching and large voltage swing for controlling the GFET, while the RC circuit is used to set the oscillation frequency (f_{osc}). The highest obtained oscillation frequency was f_{osc} = 4.2 MHz, limited only by the connections between the used discrete components. The ambipolarity of graphene allows realization of pulse-width modulators (PWMs) and voltage-controlled oscillators (VCOs) from the same oscillators, *i.e.*, without any circuit modifications. Oscillating signals with a duty cycle in the range from 20% to 80% and maximum-to-minimum frequency ratio of 7.7 were obtained in this way. The concept of exploiting favorable electronic properties of GFETs and Si CMOS is general and can be realized with any ambipolar material, although graphene is preferable for high-speed operation.

2 Results

Top-gated GFETs were fabricated from graphene grown by chemical vapor deposition[14,15] (CVD) and then transferred to

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SiO_2/Si substrates on which hBN[16] was previously exfoliated (Fig. 1(a)). The ambipolarity of graphene is reflected in the transfer curves of GFETs in which the same channel resistance (R_{ch}) is obtained at two different gate voltages (V_G). These gate voltages are symmetrically distributed around the Dirac point ($V_G = V_0$) at which $R_{ch}(V_G)$ reaches the maximum $R_{ch}(V_0)$, as illustrated in ESI Fig. S1.† When a GFET is connected to a power supply (V_{SS}) *via* a series resistor (R_S), as shown in Fig. 1(b), the output voltage of such a simple graphene circuit is $V_S = V_{SS}/(1 + R_S/R_{ch})$.[12] Therefore, the output voltage V_S has a maximum at the Dirac point for a positive supply ($V_{SS} > 0$) and minimum for a negative supply ($V_{SS} < 0$), as shown in Fig. S1.† Throughout this work, a negative supply was used ($V_{SS} = -2$ V) because it allowed to obtain more symmetric digital signals, as discussed in the Experimental section. The measured static voltage transfer characteristic of such graphene circuit is shown in Fig. 1(b).

To simplify the oscillator circuit, the supply V_{SS} of the graphene circuit was also used for the latch, hence the Si CMOS logic threshold was $V_{th} \approx V_{SS}/2 = -1$ V. Therefore, $V_{SS} = -2$ V defined the low logic level (Boolean 0), while ground (0 V) defined the high logic level (Boolean 1). The output voltage V_S of the graphene circuit was used to gate the Si CMOS logic, in this case a D latch. To be able to efficiently control, *i.e.*, change the state of the latch, the output voltage V_S had to symmetrically swing around the threshold V_{th}, as shown in Fig. 1(b). This was adjusted with the series resistor R_S, which had to be below $R_{ch}(V_0)$ to ensure $V_S(V_0) < V_{th}$. Under these conditions, the graphene circuit was able to trigger the latch in two operating points, denoted by B and C in Fig. 1(b), in which $V_S = V_{th}$.

Two types of oscillators were realized: parabolic (Fig. 1(c)) and bow tie (Fig. 1(e)), depending whether the Dirac point was a part of the oscillation cycle or not. In the first case, the operating point of the GFET oscillates between the points B and C moving through the Dirac point, as depicted in Fig. 1(d). In the case of the bow tie oscillator, the operating point oscillates outside of the operating range of the parabolic oscillator, *i.e.*, between the points A and B and between the points D and C in Fig. 1(f). In both cases, the D latch was operated in the toggle mode, *i.e.*, the latch changed its state whenever it was enabled, which was realized by connecting the complementary output ($\bar{Q}$) of the latch to its data input (D). The latch in the parabolic oscillator was enabled for $V_S > V_{th}$ and in the bow tie for $V_S < V_{th}$. The basic principle of operation of a D latch is briefly described in Fig. S2.†

In the parabolic oscillator, shown in Fig. 1(c), the high level at the output of the latch ($V_Q = 0$ V, *i.e.*, $Q = 1$) charges the capacitor C through the resistor R, *i.e.*, the gate voltage V_G (equal to the capacitor voltage) increases. As V_G increases, the output voltage V_S of the GFET first decreases (for $V_B < V_G < V_0$) and then increases (for $V_0 < V_G < V_C$), as shown in Fig. 1(d). When V_G reaches V_C (the voltage in the operating point C), the output voltage of the graphene circuit reaches the threshold voltage V_{th} enabling the latch. This changes the state of the latch, *i.e.*, the output switches to the low state ($V_Q = V_{SS} = -2$ V,

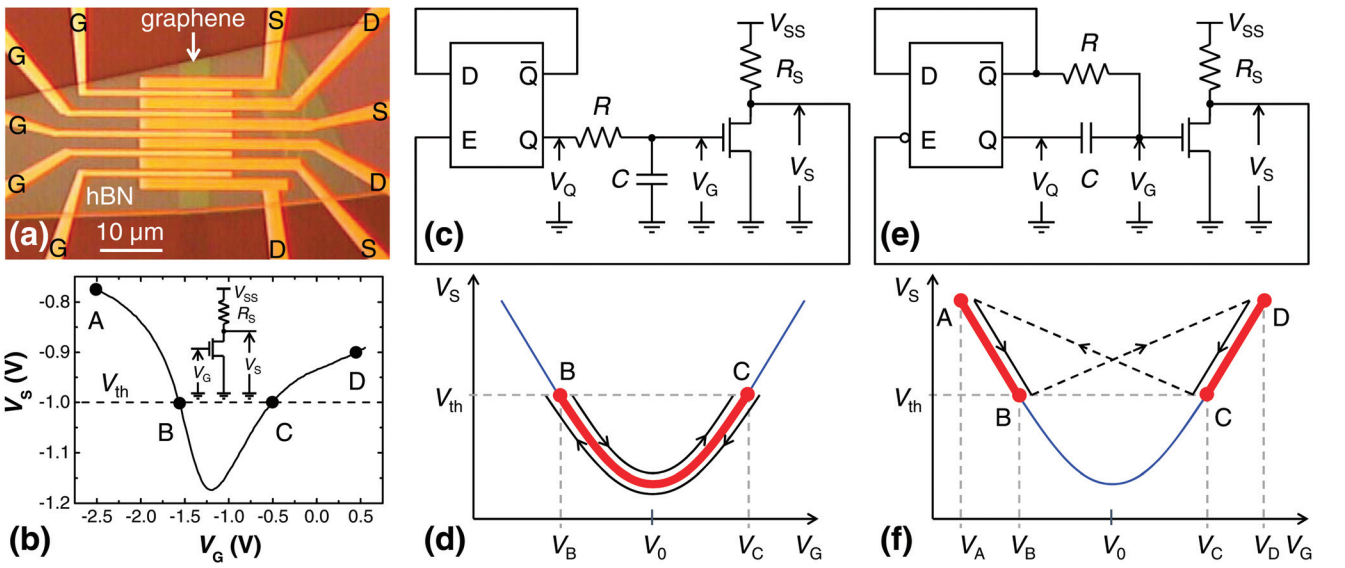

Fig. 1 Graphene–Si CMOS oscillators. (a) Optical image of 5 top-gated GFETs fabricated on an hBN flake. The source (S) and drain (D) contacts were made of Au while the gate (G) stack was made of Al/AlO_x. (b) The measured static voltage transfer characteristic of a circuit comprising a GFET connected to a supply $V_{SS} = -2$ V *via* load $R_S = 1.26$ kΩ (the circuit is shown in the inset). The load is realized as one of the neighboring GFETs in (a) with a floating (*i.e.*, not connected) gate. The output voltage V_S equals the threshold of the Si CMOS logic $V_{th} \approx V_{SS}/2$ at the operating points B and C. (c) The schematic of a parabolic oscillator comprising the graphene circuit in (b), a Si CMOS D latch, and a timing RC circuit. The latch is enabled for $V_S > V_{th}$. (d) In the parabolic oscillator, the operating point oscillates between the operating points B and C (and therefore passes through the Dirac point). (e) The schematic of a bow tie oscillator comprising the same elements as the parabolic oscillator but with a latch which is enabled for $V_S < V_{th}$. (f) In the bow tie oscillator, the operating point oscillates along the segments AB and DC (and therefore does not pass through the Dirac point).

i.e., $Q = 0$) and the capacitor starts discharging through the same resistor. As V_G decreases, V_S decreases below the threshold V_{th} disabling the latch. With the further decrease of V_G, V_S first decreases (for $V_0 < V_G < V_C$) and then increases (for $V_B < V_G < V_0$), finally reaching the threshold voltage V_{th} in the operating point B. This enables the latch again, which switches to the high state ($Q = 1$) and starts charging the capacitor. As V_S decreases, the latch disables and the entire cycle repeats again. In this way, the present relaxation oscillator keeps oscillating between the operating points B and C.

In the bow tie oscillator, shown in Fig. 1(e), when the latch is in the low state ($V_Q = V_{SS} = -2$ V, *i.e.*, $Q = 0$), the high state at the complementary output ($\bar{Q} = 1$) charges the capacitor C through the resistor R, and the gate voltage increases to V_B, as shown in Fig. 1(f). As V_G increases, the output voltage V_S of the graphene circuit decreases and when it reaches the threshold V_{th} in the operating point B, the latch is enabled and switches to the high state ($V_Q = 0$ V, *i.e.*, $Q = 1$). The sudden increase of V_Q by $|V_{SS}|$ is transferred to the gate voltage V_G because the capacitor voltage is a continuous function of time. As a consequence, the oscillator switches to the operating point D in which $V_D = V_B + |V_{SS}|$. This disables the latch and the low state at the complementary output ($\bar{Q} = 0$) starts discharging the capacitor and therefore decreasing V_G. Consequently, V_S decreases from V_D to V_C, enabling the latch at the operating point C in which $V_S = V_{th}$. The latch switches to the low state again, instantly decreasing V_G by $|V_{SS}|$. The oscillator therefore switches to the operating point A in which $V_A = V_C - |V_{SS}|$ initiating the same cycle again.

The measured signals in the oscillators are shown in Fig. 2, in which they were tuned to audio frequencies ($f_{osc} < 20$ kHz) for clarity. The highest measured oscillation frequency was $f_{osc} = 4.2$ MHz (Fig. S3†), limited by the off-chip connections between the graphene and Si CMOS chips. This limitation could be overcome by integrating both technologies in a single chip.[17,18] The oscillation frequency was set by the timing RC circuit, *i.e.*, by the charging and discharging times of the capacitor. In the parabolic oscillator, the durations of the high state ($Q = 1$) and low state ($Q = 0$) are $t_1 = RC\ln(V_B/V_C)$ and $t_0 = RC\ln((V_C - V_{SS})/(V_B - V_{SS}))$, respectively, which can easily be obtained from the transient response of a simple RC circuit.[19] In the bow tie oscillator, they are $t_1 = RC\ln((V_B - 2V_{SS})/(V_C - V_{SS}))$ and $t_0 = RC\ln((V_C + V_{SS})/V_B)$. This gives for the oscillation frequency $f_{osc} = 1/T \propto 1/(RC)$, where $T = t_1 + t_0$ is the period.

The gate voltage levels V_B and V_C, at which $V_S = V_{th}$, mainly influence the duty cycle ($D = t_1/T$) of the signals. The advantage of the oscillators is that the symmetric signals ($D = 50\%$) are obtained for $V_{SS} = V_B + V_C$, regardless of the asymmetry of the transfer curve of the GFET around the Dirac point (Fig. 1(b)). In this case, the output voltage V_S of the GFET has the fundamental frequency of $2f_{osc}$, *i.e.*, the oscillators are capable of generating the signals at frequencies f_{osc} and $2f_{osc}$ at the same time. The asymmetry of the transfer curve of the GFET only causes the asymmetry of V_S in Fig. 2, which is observable due to the large signal operation of the circuit.

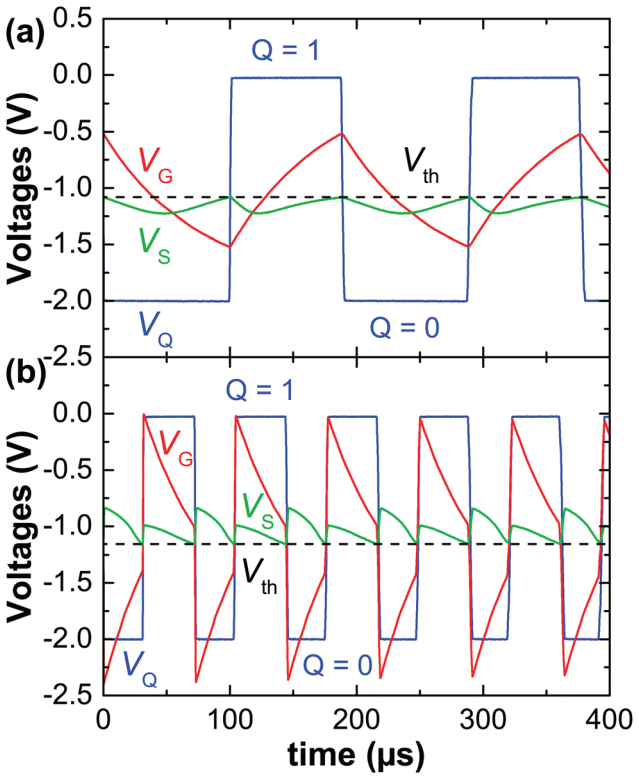

Fig. 2 The measured waveforms in the oscillators in air ambient for $V_{SS} = -2$ V, $R_S = 1.26$ kΩ, and $C = 1$ nF. (a) The waveforms in the parabolic oscillator with $R = 85$ kΩ resulting in the oscillation frequency $f_{osc} = 5.3$ kHz and duty cycle $D = 46\%$. (b) The waveforms in the bow tie oscillator with $R = 57$ kΩ, $f_{osc} = 13.8$ kHz, and $D = 55\%$.

The gate voltage levels V_B and V_C and therefore the duty cycle D can be controlled by the GFET back-gate voltage, thus turning the oscillators into the PWMs without any circuit modifications. PWMs are typically used to digitally control the power supplies in electronic circuits.[20] Fig. 3(a) shows the static voltage transfer characteristic $V_S(V_G)$ at different back-gate voltages (V_{BG}). As the back-gate voltage is increased, a smaller top-gate voltage was required to reach the same carrier density in the channel, *i.e.*, the transfer characteristic was shifted towards smaller voltages, as shown in Fig. 3(a). This decreased both V_B and V_C as V_{BG} increased (Fig. S4†). In the parabolic oscillator, this increased t_0 (Fig. S4†) and therefore decreased the duty cycle, as shown in Fig. 3(b). The measured duty cycle changed from 20% to 78% in one of the parabolic oscillators. In the bow tie oscillator, the duty cycle increased with V_{BG}, as the capacitor was charged in the low state (Fig. S4†) rather than in the high state as with the parabolic oscillator.

The graphene chip was fully integrated, *i.e.*, the fixed load resistor R_S was integrated with the GFET as the channel of another GFET with a floating gate (Fig. 1(a)). However, the channel resistance R_S could also be changed by connecting this gate to a voltage source V_{GG}, as shown in Fig. 4(a). The increase of V_{GG} decreased R_S and therefore shifted the static

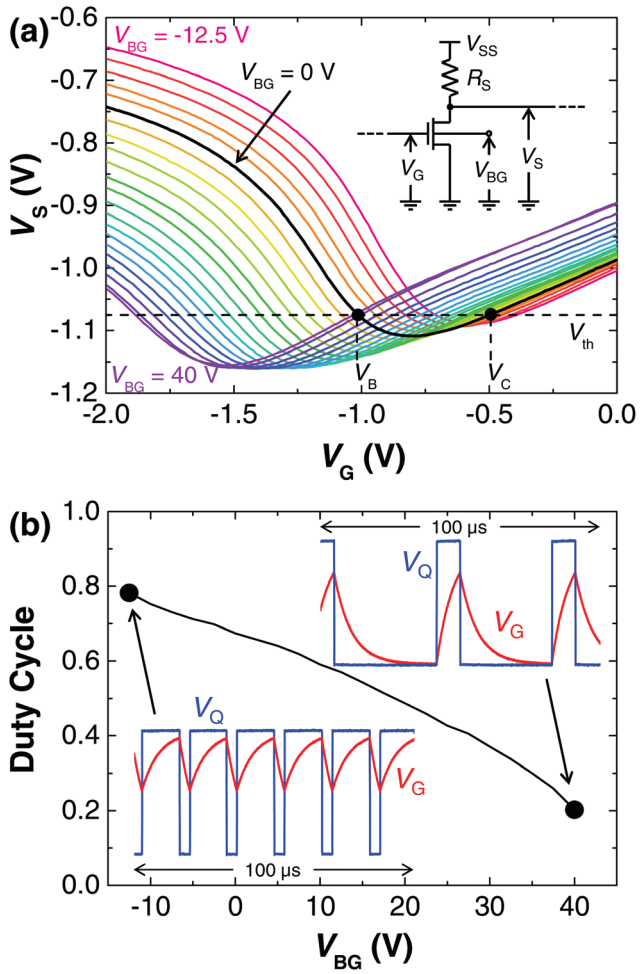

Fig. 3 PWM functionality obtained by controlling the duty cycle with a back-gate voltage at V_{SS} = −2 V and R_S = 708 Ω. (a) The static voltage transfer characteristics $V_S(V_G)$ of the graphene circuit shown in the inset, at the back-gate voltages V_{BG} ranging from −12.5 V to 40 V in steps of 2.5 V. The intersections between a characteristic and the CMOS threshold V_{th} (which are at $V_G = V_B$ and $V_G = V_C$) can be controlled by V_{BG}. For V_{BG} = 0 V, the intersections are at $V_B \approx -1$ V and $V_C \approx -0.5$ V. (b) The measured duty cycle D as a function of the applied back-gate voltage V_{BG}. The insets show the measured waveforms with the largest (D = 78%) and smallest (D = 20%) measured duty cycle. The time range of the waveforms is 100 µs and the voltage range is from −2 V to 0 V. In all measurements R = 17.78 kΩ and C = 0.5 nF.

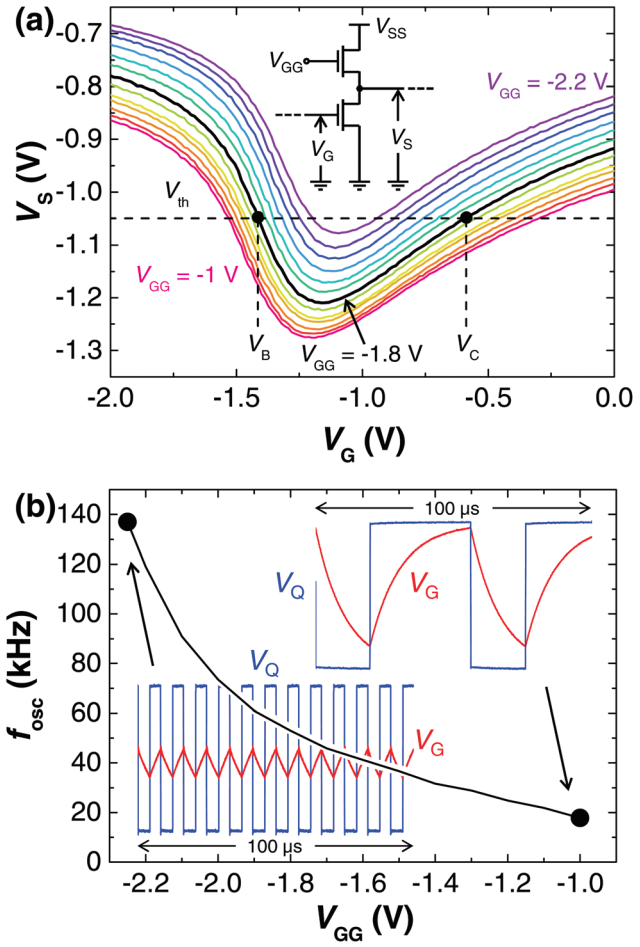

Fig. 4 VCO functionality obtained by controlling the oscillation frequency with a gate voltage at V_{SS} = −2 V. (a) The static voltage transfer characteristics $V_S(V_G)$ of the graphene circuit shown in the inset for different gate voltages V_{GG} of a load GFET which replaces the series resistor R_S. V_{GG} ranges from −2.2 V to −1 V in steps of 0.1 V. V_{GG} controls the GFET resistance R_S and consequently the vertical shift of the transfer characteristics. The intersections between a characteristic and the CMOS threshold V_{th} (which are at $V_G = V_B$ and $V_G = V_C$) are therefore controlled by V_{GG}. For V_{GG} = −1.8 V, the intersections are at $V_B \approx -1.4$ V and $V_C \approx -0.6$ V. (b) The measured oscillation frequency f_{osc} as a function of the gate voltage V_{GG}. The insets show the measured waveforms with the highest (f_{osc} = 137 kHz) and lowest (f_{osc} = 18 kHz) measured oscillation frequency. The time range of the waveforms is 100 µs and the voltage range is from −2 V to 0 V. In all measurements R = 10 kΩ and C = 1 nF.

voltage transfer characteristic $V_S(V_G)$ to smaller output voltages V_S, as shown in the same figure. This decreased V_B and increased V_C (Fig. S5†) and therefore increased both t_1 and t_0 in the parabolic oscillators, decreasing their oscillation frequency f_{osc}. In this way, the gate voltage V_{GG} was used to control f_{osc} realizing the functionality of a VCO, one of the most used electronic circuits in communications systems.[21] By increasing V_{GG}, the measured oscillation frequency decreased from 137 to 18 kHz in one of the parabolic oscillators, as shown in Fig. 4(b). In contrast, the increase of V_{GG} decreased t_1 and t_0 (Fig. S5†) and therefore increased the oscillation frequency in the bow tie oscillators.

3 Discussion

For the same circuit components, the oscillation frequency of the bow tie oscillator is higher than that of the parabolic oscillator because the operating point of the bow tie oscillator stays only on one side of the Dirac point during each half period. Assuming a duty cycle of 50% in both oscillators, *i.e.*, $V_{SS} = V_B + V_C$, the bow tie oscillator oscillates at twice the frequency of the parabolic oscillator if $V_B = 0.742V_{SS}$ and $V_C = 0.258V_{SS}$. The disadvantage of the bow tie oscillator is that its gate voltage can overshoot the supply voltage rails at the signal

edges, *e.g.*, $|V_G| > |V_{SS}|$ at the falling edge of Q in Fig. 2(b). This could be dangerous for other components in the circuit, primarily the GFET which has the gate voltage breakdown of ~2.9 V. In a bow tie PWM, the largest overshoots are at the two extremes of the duty cycle.

The present oscillators can be fabricated on a large scale because they do not require exfoliated hBN or a global back gate. The exfoliated hBN was used only because of the large doping of the GFETs on SiO_2 in the used batch. Similarly, the global backgate was used in PWMs only for demonstration; in realistic devices this can easily be replaced by a local back gate so that each PWM is individually gated. Control voltages in PWMs and VCOs are typically obtained from the output of other circuits rather than separate power supplies. For example, a VCO is driven by a phase detector in a phase-locked loop (PLL).[21]

The demonstrated principle of operation is general, *i.e.*, the other ambipolar materials, *e.g.*, amorphous Si,[22] Si nanowires[23] or semiconducting carbon nanotubes,[24] could also be used. Although their ambipolarity has been exploited in applications[25,26] similar to that of graphene,[12] they have not been combined with Si CMOS logic so far. In contrast to other ambipolar materials, graphene has much larger carrier mobility[1] and saturation velocity[2] allowing much faster operation. The symmetric band structure of graphene[27] (*i.e.*, almost identical electron and hole mobilities) also leads to symmetric digital signals, which cannot easily be obtained in materials with different electron and hole mobilities.

In terms of the component count, the present oscillators are similar to the simplest Si field-effect transistor (FET) oscillators, because they were made of only 5 components. However, it should be noted that a gated D latch[28] is usually made of 10 FETs, resulting in 14 components in the oscillator. The commercial discrete D latches usually comprise more than 10 FETs because they also provide three-state outputs (which were not used here). For comparison, the simplest conventional astable multivibrators with vertical signal edges[19] have only 2 FETs, but also 10 other components, bringing the total component count to 12. The simplest Si CMOS ring oscillators[29] have 6 FETs but their oscillation frequency is determined by internal gate delays[8,9] rather than a timing RC circuit. Finally, the simplest Schmitt trigger inverter oscillators[30] have 8 components. Despite similar component count, the present oscillators provide additional functionalities of the PWMs and VCOs. Compared to graphene ring oscillators,[8,9] which have a limited output voltage swing, the output voltage swing in the present oscillators is determined by the Si CMOS part of the circuit providing rail-to-rail operation.

Although the oscillators use a GFET which cannot be turned off, the static power dissipation is not a critical factor because the relaxation oscillators do not spend any time in the idle state and dissipate the dynamic power continuously. This could also be understood from the ratio between the static power dissipation of the graphene circuit $P_s \sim {V_{SS}}^2/(2R_s)$ and dynamic (switching) power dissipation $P_d \sim f_{osc}C{V_{SS}}^2/2$ of the timing RC circuit. Here it was assumed for simplicity that the voltage on the capacitor oscillates between $0.25V_{SS}$ and $0.75V_{SS}$ (as in Fig. 2(a)) and that the power dissipation of the D latch is negligible. The ratio $P_s/P_d \sim R/R_s$, because $f_{osc} \sim 1/(RC)$, meaning that for large f_{osc} (*i.e.*, $R < R_s$), $P_s < P_d$. For example, $R/R_s \sim 50$ in the low-frequency oscillators shown in Fig. 2, but $R/R_s \sim 0.25$ in the high-frequency oscillator shown in Fig. S3.†

The realized oscillators could be used to provide high-frequency reference required for the signal up/down conversion in high frequency transmitters/receivers. The D latch is not expected to limit the bandwidth of the fully integrated oscillators because high-speed Si CMOS technology is capable of operating at very high serial data rates (up to 120 Gb s^{-1}).[31]

The realized oscillators could also be used to generate clock signals for digital data processing which requires the exact clock duty cycle of 50%. In microprocessors, this is typically achieved by running a VCO (inside the PLL) at twice the clock frequency and then dividing the frequency by two.[32,33] However, such realizations significantly increase the dynamic power dissipation and are not practical at very high frequencies. Our oscillators offer an alternative solution because both PWM (duty cycle tuning) and VCO (frequency tuning) are integrated in the same circuit.

The integration of graphene with Si CMOS technology should be considered in the context of 3D monolithic integrated circuits (ICs). Such ICs cannot be easily made in Si CMOS technology due to high temperatures required for the fabrication of each Si CMOS layer in a 3D stack. This problem can be overcome by stacking other transistor technologies, which do not require high-temperature fabrication, on top of Si CMOS.[34] Alternative transistor technologies also allow realization of additional functionalities which cannot be obtained with Si CMOS alone.[34,35] Graphene is a good candidate for the integration with Si CMOS in 3D monolithic ICs because it can be transferred to a target substrate at room temperature.

4 Conclusions

We exploited the symmetry of the transfer characteristics of GFETs to realize a new class of very simple electronic relaxation oscillators comprising a GFET, Si CMOS latch, and RC timing circuit. The difference between the two types of the realized oscillators was in the movement of the operating point, oscillating through the Dirac point in the first type and jumping over the Dirac point in the second type. The simplicity of the oscillators and additional PWM and VCO functionalities, obtained without any circuit modifications, stemmed from the ambipolarity of graphene. The switching and large voltage swing of generated waveforms were provided by Si CMOS logic. The introduction of graphene in Si CMOS logic may prove to be a feasible approach in simplifying it and providing additional functionality while at the same time overcoming barriers to entry of graphene in electronics.

5 Experimental

hBN was exfoliated on highly p-doped (>10^{19} cm^{-3}) Si substrates with a 300 nm thick top layer of SiO_2. The back of the Si substrates was metallized and used as a global back-gate, if needed. Monocrystalline monolayer graphene was grown by CVD on Cu from the CH_4 precursor and then transferred (by a wet process) to the same substrates on which hBN was previously exfoliated. The GFETs were patterned by electron-beam (e-beam) lithography using poly(methyl methacrylate) resist. The GFET channels (the channel width W = 5 μm) were defined by etching graphene in O_2 plasma both in parts of the substrates covered and uncovered by hBN flakes. This allowed fabrication of a large number of GFETs on hBN (the only selection criteria were the lateral size >5 μm and thickness <50 nm of the hBN flakes) and control GFETs on SiO_2 in the same chips.

The rest of the fabrication process was the same in both cases. Top-gates were patterned first by e-beam lithography followed by e-beam evaporation of 100 nm of Al. Al oxidized after a few days in air ambient creating a thin (~4 nm) native layer of AlO_x on all surfaces of Al, including the interface with graphene.[36–40] This formed an AlO_x/Al gate stack with a top-gate oxide capacitance[8,40] C_{ox} = 1.37 μF cm^{-2}. Source and drain Au contacts (100 nm) were finally fabricated by e-beam lithography and e-beam evaporation. The gate length was L = 1 μm, source-to-drain distance L_{SD} = 1.2 μm (*i.e.*, the access length from both sides of the gate was 100 nm), and length of the source and drain contacts was 2 μm.

The oscillators worked both with a positive and negative power supply. However, we found that a negative supply allowed more symmetric digital signals at $|V_{SS}| \sim 2$ V, *i.e.*, the signals with a duty cycle closer to 50%. This is because the unbiased GFETs on hBN had the Dirac voltage $V_0 \approx -0.5$ V, which changed to $\approx V_0 + V_{SS}/4$ when V_{SS} was applied (because $R_{ch} \approx R_S$ at the Dirac point). The signal symmetry requires $V_H - V_C = V_B - V_L$, *i.e.*, that the Dirac voltage is approximately half way between the voltage rails. This means $V_0 + V_{SS}/4 \approx V_{SS}/2$, *i.e.*, $V_{SS} \approx 4V_0$, which is the reason the supply $V_{SS} = -2$ V was used. The series resistance R_S was realized as either an external discrete resistor or another GFET with a floating gate. The output voltage swing of the graphene circuit depends on R_S, *e.g.*, the highest swing in the parabolic oscillator is obtained for $R_S = \sqrt{R_{ch}(V_0)R_{ch}(V_B)}$.

The GFETs were made on hBN substrate because the lower $|V_0|$ allowed the use of lower supply voltages $|V_{SS}|$, as described above. We also found that GFETs on hBN had much better long-term stability than GFETs on SiO_2. The same GFETs on hBN were repeatedly measured in the oscillators for months without any apparent degradation of their electrical properties.

The Si CMOS part of the oscillator circuit (including the timing RC circuit) was built on a breadboard (in low-frequency oscillators) or printed circuit board (in high-frequency oscillators) and connected to the GFET *via* a FormFactor probe station. The Si CMOS gated D latch was 74HC375AP or 74AC573P. The dc characteristics were measured by Keithley 2611A source measure units, while the waveforms were measured by Keysight Infiniium DSO9404A oscilloscope and Keysight N2795A and 1158A active probes.

Conflicts of interest

There are no conflicts to declare.

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