



Cite this: *Nanoscale Adv.*, 2019, **1**, 1130

Growth of graphene with large single-crystal domains by Ni foam-assisted structure and its high-gain field-effect transistors†

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High-quality graphene materials and high-performance graphene transistors have attracted much attention in recent years. To obtain high-performance graphene transistors, large single-crystal graphene is needed. The synthesis of large-domain-sized single-crystal graphene requires low nucleation density; this can lead to a lower growth rate. In this study, a Ni-foam assisted structure was developed to control the nucleation density and growth rate of graphene by tuning the flow dynamics. Lower nucleation density and high growth rate ($\sim 50 \mu\text{m min}^{-1}$) were achieved with a 4 mm-gap Ni foam. With the graphene transistor fabrication process, a pre-deposited Au film as the protective layer was used during the graphene transfer. Graphene transistors showed good current saturation with drain differential conductance as low as 0.04 S mm^{-1} in the strong saturation region. For the devices with gate length of $2 \mu\text{m}$, the intrinsic cut-off frequency f_T and maximum oscillation frequency f_{\max} were 8.4 and 16.3 GHz, respectively, with $f_{\max}/f_T = 1.9$ and power gain of up to 6.4 dB at 1 GHz. The electron velocity saturation induced by the surface optical phonons of SiO_2 substrates was analyzed. Electron velocity saturation and ultra-thin Al_2O_3 gate dielectrics were thought to be the reasons for the good current saturation and high power gain of the graphene transistors.

Received 11th September 2018

Accepted 12th December 2018

DOI: 10.1039/c8na00203g

rsc.li/nanoscale-advances

Introduction

Graphene as the two-dimensional structure of graphite exhibits numerous extraordinary physical, chemical, optical, biological and electronic properties.^{1,2} The high carrier mobility of graphene results in its promising application in high-speed field-effect transistors (FETs). The performance of graphene FETs depends on the quality of the graphene channel. In this aspect of graphene growth, a larger single-crystal domain indicates reduced boundary in the graphene channel, and it tends to maintain high electronic characteristics in graphene FETs.³ Therefore, the growth of large single-crystal graphene is imperative. Low cost and large area are obtained using the Cu-catalysed chemical vapor deposition (CVD) method, which is a promising approach to achieve large single-crystal graphene growth.⁴

The key to the growth of larger single-crystal graphene is to maintain low nucleation density in the CVD process.⁵ There are several approaches such as controlling the nucleation density on Cu foils, smoothening the surface of Cu foil, growth of Cu

oxide, substantially reducing the CH_4 percentage, and controlling the channel structure or tube shape.^{5–9} The above methods can effectively increase the size of single-crystal graphene. However, the low nucleation density also leads to a lower growth rate; most growth rates are in the range of $1\text{--}10 \mu\text{m min}^{-1}$, due to which a longer time is required for larger single-crystal graphene growth.^{5,9–12}

For graphene transistors used in wireless communication circuits, high gain values still hinder the application due to lack of current saturation.^{13–16} The way to obtain current saturation is to open a bandgap by nanopatterning of monolayer graphene (MLG)¹⁷ or by applying vertical electric displacement on Bernal-stacked bilayer graphene (BLG).^{18,19} These methods have their respective drawbacks for practical application. Thinning the gate dielectric is thought to be another efficient way to obtain current saturation.²⁰

In this study, we design a simple Ni foam-assisted structure to control the graphene growth on a Cu foil. With the Ni foam, the nucleation density and growth kinetics of graphene are controlled. The state of the precursors on the top surface of the Cu foil is controlled by regulating the gap of the Ni foam and Cu foil. With the Ni foam-assisted graphene growth, the nucleation density is lowered to $1/\text{mm}^2$, and the growth rate can be higher than $50 \mu\text{m min}^{-1}$. A Au film was pre-deposited on the graphene surface as a protective layer to avoid the contamination of graphene during the transfer and FET fabrication process. By

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† Electronic supplementary information (ESI) available. See DOI: 10.1039/c8na00203g



thinning the gate dielectric Al_2O_3 down to 5 nm, graphene FETs with gate length of 2 μm show good current saturation and power gain up to 6.4 dB at 1 GHz.

Experimental

Growth and characterization of graphene

Cu foil (98%, 25 μm , Alfa Aesar) was oxidized at 200 $^{\circ}\text{C}$ for 20 min on a hot plate. The growth of graphene was conducted in a vertical-type chemical vapor deposition furnace. The Cu foil was loaded onto the heater, and the pressure was controlled at 25 mbar. Ar gas with a flow of 1000 sccm was used to remove the air, and the temperature was kept at 1000 $^{\circ}\text{C}$ for 10 min. Then, graphene was grown at 1000 $^{\circ}\text{C}$ with a methane flow of 2 sccm and H_2 flow of 60 sccm. The size and nucleation density of graphene were measured by optical microscopy (OM). The Cu foil with graphene was oxidized at 160 $^{\circ}\text{C}$ for 10 min on a hot plate to increase the contrast for OM observation. Micro-Raman scattering experiments were performed at RT with a spectrometer (514 nm).

Graphene transfer

After the growth of graphene on the Cu foil, 30 nm of Au film was immediately deposited onto the graphene surface on the top side of the Cu foil. The graphene on the bottom side of Cu foil was removed by O_2 plasma. Cu foil was etched by FeCl_3 aqueous solution and then, the Au/graphene film was rinsed in deionized water three times. Au/graphene was transferred onto an SiO_2/Si wafer; the thickness of SiO_2 was 90 nm. Au/graphene/ SiO_2/Si was dried at 90 $^{\circ}\text{C}$ for 20 min.

Device fabrication

Graphene FETs were fabricated by a self-aligned process following the method reported in our previous study.²¹ Optical lithography was adopted to define the channel regions, followed by electrical isolation by exposing the graphene surface to oxygen plasma after removal of the Au film outside the channel. We deposited Ti 20 nm/Pt 50 nm/Au 150 nm to form the electrode pads. Gates of 2 μm were patterned by optical lithography. Subsequently, the Au layer under the gates was wet-etched to form a self-aligned source and drain ohmic contacts automatically. Next, 1.7 nm-thick Al was deposited by e-beam evaporation, which was then oxidised in air for 1 day at room temperature to form an Al_2O_3 dielectric. The thickness of the alumina was $t_{\text{Al}_2\text{O}_3} \approx 5$ nm. Finally, a 150 nm-thick Al metal film was evaporated to form the gate electrodes.

Results and discussion

Ni foam is used to assist the graphene growth by controlling the precursor flow dynamics. Fig. 1(a) shows the schematic of Ni foam-assisted graphene growth. The distance between the Ni foam and Cu substrate is 4 mm. The flow rate of the precursors decreases due to the Ni foam on the top of the Cu substrate; the decreased flow rate can lead to lower nucleation density and a higher growth rate, as shown in Fig. 1(c), with a growth time of

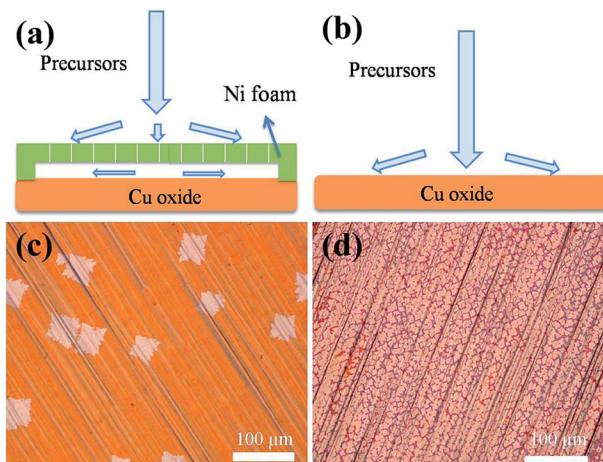


Fig. 1 (a) Schematic image and (c) OM image of Ni foam-assisted graphene growth with a growth time of 15 min; (b) schematic image and (d) OM image of conventional graphene growth on Cu foil with a growth time of 10 min.

15 min. The schematic without Ni foam-assisted graphene growth is shown in Fig. 1(b). Fig. 1(d) shows the results without Ni foam-assisted growth. The growth time is 10 min. Fig. 1(d) shows very high nucleation density and slower growth rate compared with Fig. 1(c), demonstrating that we can decrease the nucleation density and increase the growth rate with the Ni foam-assisted graphene growth process.

The mechanism of the influence of Ni foam in the graphene growth process was studied. The Cu foil was oxidized before insertion into the tube, and we used EDX to study the oxygen coverage on the Cu foil. SEM and EDX images are shown in Fig. S1.[†] After heating to 1030 $^{\circ}\text{C}$ under Ar gas for 10 min, the oxygen coverage of the Cu foil surface with the Ni foam structure was significantly higher than that without the Ni foam-assisted structure. With the Ni foam structure, the surface oxygen coverage was at 4.62%, and without the Ni foam structure, the surface oxygen coverage was at 1.28%. The higher oxygen content can suppress the nucleation and improve the graphene growth rate.²²

To study the effect of the precursor flow rate, graphene growth under different gaps between the Ni foam and Cu substrate is studied. The gaps are set as 3 mm, 4 mm, and 5 mm. The growth times of graphene with and without Ni foam are 15 min and 10 min, respectively. Fig. 2(a), (b) and (c) show the graphene growth with 3 mm, 4 mm, and 5 mm gaps, respectively. It can be found that the nucleation density increases as the gap increases. Fig. 2(d) shows the graphene grown without Ni foam; the nucleation density is very high ($\sim 1.2 \times 10^4/\text{mm}^2$) and the graphene size is very small. Fig. 2(e) shows the corresponding nucleation density of the Ni foam-assisted graphene growth with different gaps. As the Ni foam gap increases, the precursor flow rate increases, resulting in higher nucleation density. Fig. 2(f) shows the average growth rate of graphene with different gaps. The rate of graphene growth is the highest in the 4 mm Ni foam gap. Without Ni foam, the graphene growth has very high precursor flow rate but



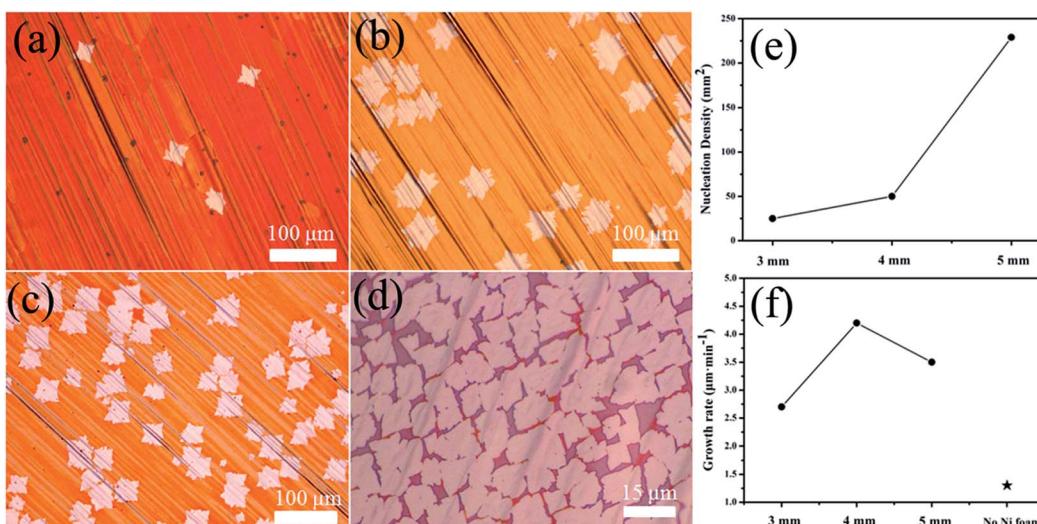


Fig. 2 Graphene growth under different gaps between the Ni foam and Cu substrate. Gap size: (a) 3 mm, (b) 4 mm, and (c) 5 mm. (d) Graphene growth without the Ni foam. (e) Nucleation density. (f) Growth rate of graphene with different Ni foam gaps.

a lower growth rate. The above results show that 4 mm Ni foam gap is appropriate for assisted graphene growth; it can maintain a higher growth rate and a relatively lower nucleation density.

Fig. 3 shows the images of graphene growth with Ni foam (4 mm gap) and without Ni foam at 1060 °C. For graphene with Ni foam grown at 1060 °C for 10 min, the grain size of graphene is about 512 μm, as shown in Fig. 3(a). The nucleation density is $\sim 1/\text{mm}^2$ and growth rate is $\sim 51.2 \mu\text{m min}^{-1}$. With prolonged growth time, the grain size of graphene reaches millimeter scale. Fig. 3(b) shows graphene grown for 1 min without Ni foam at 1060 °C. The nucleation density shows no decrease as the growth temperature increases to 1060 °C. Fig. 3(c) and (d)

show the OM images of the transferred graphene onto SiO_2/Si substrates. Fig. 3(c) shows the image of graphene growth with Ni foam. The surface of graphene in optical microscopy view is very clear. There are many adlayers for graphene grown without Ni foam, as shown in Fig. 3(d). This is mainly due to the large number of boundaries between the small grains. Precursors go through to the boundary, forming many adlayers. Fig. 3(e) and (f) show the Raman shift of transferred graphene on the SiO_2/Si substrates. As shown in Fig. 3(e), for graphene grown with Ni foam, the intensity ratio of the 2D/G peak is 3.4 with no clear D peak, demonstrating a single-layer graphene of high-quality.²³ For graphene grown without Ni foam, the Raman shifts of the single-

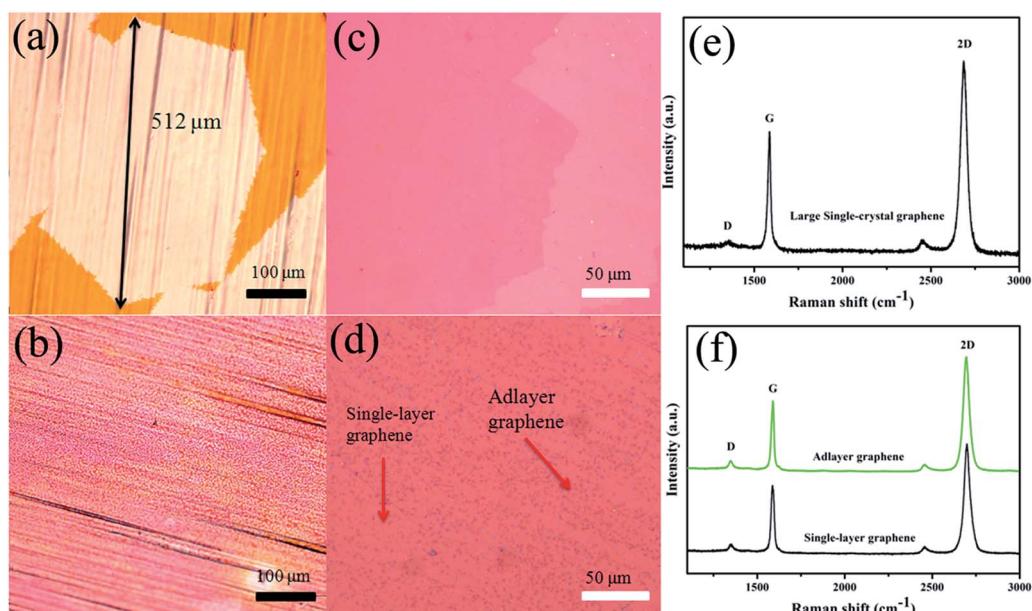


Fig. 3 OM images of graphene growth on Cu foil (a) with Ni foam (4 mm gap) and (b) without Ni foam at 1060 °C. OM images and Raman pattern of graphene transferred to the SiO_2/Si substrates: (c, e) with Ni foam (4 mm gap) and (d, f) without Ni foam.

layer and adlayers (in Fig. 3(d)) are given in Fig. 3(f). The intensity ratio of the 2D/G peak is 3.5 for the adlayer graphene, demonstrating that adlayers do not exhibit an AB stacking structure.²⁴ The relative intensity of the D/G peak in Fig. 3(f) is higher than that in Fig. 3(e), demonstrating that the quality of graphene grown with Ni foam is higher than that without Ni foam.²³

The relationship between the growth rate and material quality was studied. We set up five sets of experiments. The first experiment involved the fabrication of a Cu foil without a Ni foam-assisted structure with growth temperature of 1000 °C; the other experiments involved the fabrication of Cu foils with 4 mm-gap Ni foam with growth temperatures of 1000 °C, 1020 °C, 1040 °C and 1060 °C. The graphene growth rates in these five samples are found to be $\sim 1 \mu\text{m min}^{-1}$, $\sim 4 \mu\text{m min}^{-1}$, $\sim 12 \mu\text{m min}^{-1}$, $\sim 23 \mu\text{m min}^{-1}$ and $\sim 50 \mu\text{m min}^{-1}$. The Raman shifts of these five graphene samples were also studied. The Raman results are shown in Fig. S2.† The FWHM values of the 2D peaks of the five samples are 38 cm⁻¹, 37 cm⁻¹, 39 cm⁻¹, 38 cm⁻¹ and 43 cm⁻¹, showing that the samples are all monolayer graphene. It was also found that the I_D/I_G ratios decrease as the growth rates increase. The I_D/I_G ratios of the five samples are 0.05, 0.03, 0.03, 0.02 and 0.02. The larger I_D/I_G ratio of the graphene sample with a growth rate of $\sim 1 \mu\text{m min}^{-1}$ may be mainly due to the small single-crystal size and numerous grain boundaries.

The fabrication schedule and OM image of graphene FETs fabricated by a self-aligned process are shown in Fig. S3.† Dual-gate graphene transistors with gate length of 2 μm and gate width of 100 $\mu\text{m} \times 2$ were fabricated. The field-effect mobility values of the graphene transistors were $2450 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (hole) and $3307 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (electron), respectively (Fig. 4(d)), indicating the high quality of the graphene material and less contamination in the device fabrication process.

Fig. 4 shows the DC electrical transport characteristics of graphene FETs. The DC electrical transport measurements were obtained using a Semiconductor Parameter Analyser (SPA). As shown in Fig. 4(a), the drain current (I_{ds}) shows strong saturation with maximum scaled on-current I_{ds} reaching 0.54 A mm⁻¹. The sample shows n-type doping with the Dirac point at $V_{\text{gs}} = -0.85 \text{ V}$ and the maximum transconductance (g_m) is measured at $V_{\text{ds}} = -2 \text{ V}$ is 0.2 S mm^{-1} , as shown in Fig. 4(b). Due to the strong drain current saturation, the drain differential conductance (g_{ds}) is small, as shown in Fig. 4(c). The g_{ds} value is as low as 0.04 S mm^{-1} in the strong saturation region ($-2 \text{ V} \leq V_{\text{ds}} \leq -3 \text{ V}$).

High-frequency scattering parameters (S -parameters) of the transistors were measured up to 10 GHz using standard GSG probes. Fig. 5(a)–(c) show the as-measured, de-embedded, and intrinsic short-circuit current gain ($|H_{21}|^2$), maximum stable/available gain (MSG/MAG), and Mason's unilateral power gain (U) extracted from S -parameters for the graphene transistor with $L_g = 2 \mu\text{m}$ and $W_g = 100 \mu\text{m} \times 2$. As a result, the intrinsic cut-off frequency f_T and maximum oscillation frequency f_{max} were determined to be 8.4 and 16.3 GHz for the device. The calculated f_{max} values from the maximum stable/available gain (MSG/MAG) and Mason's unilateral power gain (U) showed good consistency with each other, indicating the veracity of the derivation process.

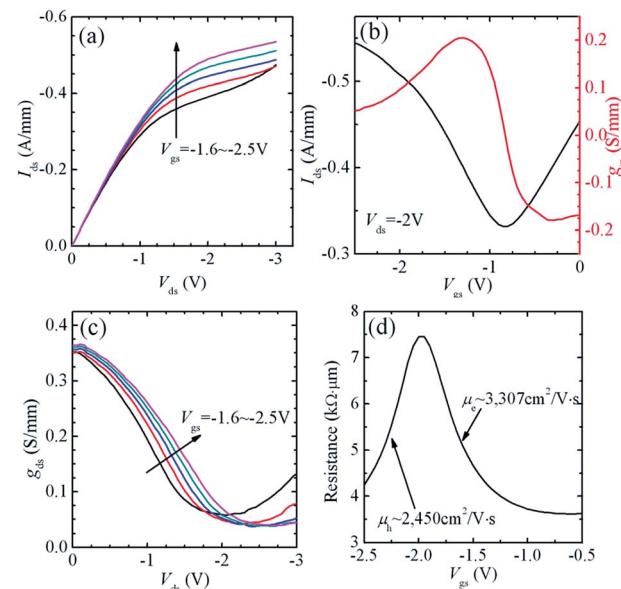


Fig. 4 DC characteristics of the graphene transistors. (a) The current–voltage characteristics at gate voltages ranging from -1.6 V to -2.5 V . (b) Transfer characteristics at $V_{\text{ds}} = -2 \text{ V}$ with $-2.5 \text{ V} \leq V_{\text{gs}} \leq 0 \text{ V}$. (c) Drain differential conductance g_{ds} . (d) Scaled resistance of a graphene transistor versus gate voltage at $V_{\text{ds}} = -0.1 \text{ V}$.

Fig. 5(d) shows forward power gain $|S_{21}|$ and the AC open-circuit voltage gain Z_{21}/Z_{11} as a function of frequency for the graphene transistor. The AC open-circuit voltage gain reaches 15 dB

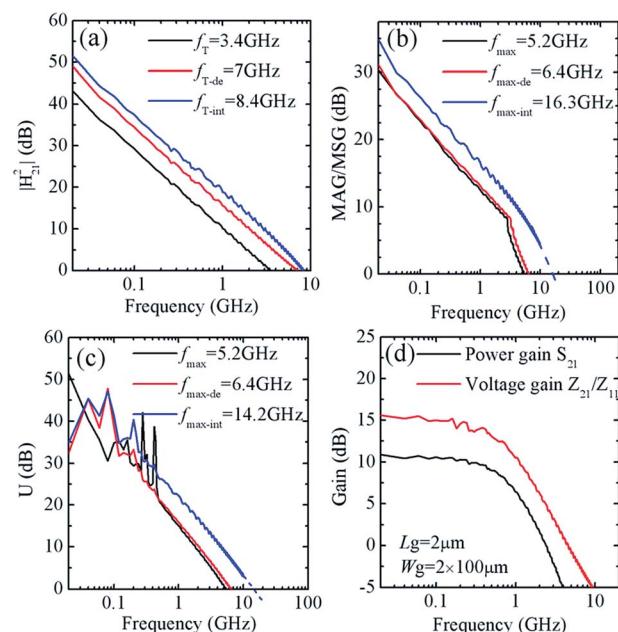


Fig. 5 High-frequency characteristics of the GFET with a gate length of $2 \mu\text{m}$ and a gate width of $100 \mu\text{m} \times 2$. (a) Measured, de-embedded, and intrinsic $|H_{21}|^2$; (b) measured, de-embedded, and intrinsic maximum stable/available gain (MSG/MAG); (c) measured, de-embedded, and intrinsic Mason's unilateral power gain (U); and (d) measured frequency response of AC open-circuit voltage gain (Z_{21}/Z_{11}) and forward power gain ($|S_{21}|$).



Table 1 Component parameters of the graphene transistor with gate length of 2 μm and gate width of 100 $\mu\text{m} \times 2$

| C_{gd} (fF) | C_{gs} (fF) | C_{ds} (fF) | g_{ds} (mS) | g_{m} (mS) | R_{i} (Ω) | R_{g} (Ω) | R_{s} (Ω) | R_{d} (Ω) |
|----------------------|----------------------|----------------------|----------------------|---------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 341 | 1407 | 785 | 17 | 96 | 3.2 | 5 | 6.5 | 6.5 |

for the measured frequency range. Power gain $|S_{21}|$, which reflects the real power amplification of a two-port network, is around 6.4 dB at 1 GHz for the device, which is among the highest reported values for CVD graphene transistors.^{25,26} The graphene FETs show very high power gain, which is a result of the strong drain current saturation-induced low drain differential conductance (g_{ds}).

There are two possible reasons for the strong drain current saturation. One is the electron velocity saturation induced by the surface optical phonons of SiO_2 substrates.^{27,28} In the case of graphene with mobility limited by impurity scattering, the high field behavior is determined by the emission of surface optical phonons in the SiO_2 substrate.²⁹ The energy of the surface optical phonons of SiO_2 is $\varepsilon_{\text{SO}} \approx 59$ meV. From ε_{SO} , the saturated electron velocity v_{sat} can be estimated via emission of the surface optical phonons, which is denoted as follows:^{30,31}

$$v_{\text{sat}} = \frac{2}{\hbar} \frac{\varepsilon_{\text{SO}}}{\pi \sqrt{\pi n_s}} \sqrt{1 - \frac{\varepsilon_{\text{SO}}^2}{4\pi n_s(\hbar v_f)^2}} \frac{1}{N_{\text{OP}} + 1} \quad (1)$$

here, N_{OP} is the phonon occupation number. In the high carrier density limit, the above relation may be reduced to

$$v_{\text{sat}} = \frac{2\varepsilon_{\text{SO}}}{\hbar\pi\sqrt{\pi n_s}} \quad (2)$$

Table 1 shows the small signal model parameters of GFET.³²⁻³⁴ The extracted gate capacitance $C_g = C_{\text{gs}} + C_{\text{gd}}$ is 1748 fF. The sheet density of the graphene channel can be estimated by $n_s = V_{\text{Dirac}} \times C_g/e$.³⁵ The sample shows n-type doping with the Dirac point at $V_{\text{gs}} = -0.85$ V, and the calculated graphene channel (n_s) is $2.3 \times 10^{12} \text{ cm}^{-2}$. From eqn (2), one can expect saturated electron velocity of $1.5 \times 10^7 \text{ cm s}^{-1}$ with $n_s = 2.3 \times 10^{12} \text{ cm}^{-2}$ in the graphene on Si/SiO_2 substrates. The intrinsic cut-off frequency f_{T} in an FET can be estimated as follows:

$$f_{\text{T}} = \frac{v_{\text{sat}}}{2\pi L_g}$$

For a graphene transistor with gate length L_g of 2 μm , the estimated intrinsic cut-off frequency f_{T} is 12 GHz for n_{sh} of $2.3 \times 10^{12} \text{ cm}^{-2}$. The measured intrinsic f_{T} of our device is 8.4 GHz, which is slightly lower than the estimated one, indicating that the electron velocity can achieve saturation. The ultra-thin self-oxidized AlO_x gate dielectric should also be helpful in drain current saturation. Han *et al.* have shown that the low-density state (DOS) of graphene can help obtain drain current saturated characteristics in thin dielectric devices.²⁰ They demonstrated that by employing a very thin gate dielectric (equivalent oxide thickness (EOT) less than 2 nm), full drain current saturation can be obtained for graphene FETs with short channels. EOT of graphene FETs in this study is approximately 2 nm, which will be beneficial for current saturation.

Conclusions

With a Ni foam-assisted structure to control the graphene growth on a Cu foil, graphene with grain size of millimeters was prepared. A pre-deposited Au film as a protective layer to avoid the pollution of graphene was used during the transfer and graphene FET fabrication process. Graphene FETs with gate length of 2 μm show good current saturation and power gain up to 6.4 dB at 1 GHz. Electron velocity saturation induced by surface optical phonons of SiO_2 substrates and ultra-thin gate dielectric were thought to be the reasons for good current saturation and high power gain. Graphene transistors with short gate length will be developed in the next study to push frequency and power gain.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (61674131 and 61306006) and Basic Research Program of Hebei (18961020D).

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