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Gate-tuned conductance of graphene-ribbon junctions with nanoscale width variations†

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To utilize graphene as interconnection electrodes in high-density nanoelectronic structures, the electrical stability of graphene should be guaranteed under nanometer-scale deviations. Graphene-ribbon (GR) junctions with accessible dimensions (*i.e.*, sub-micrometer widths) are used in diverse interconnection electrode applications and should be characterized properly if they are to be applied in high-density nanoelectronics. Analyzing the effects of nanoscale GR width variations on the conductance of the entire graphene electrode is necessary for their proper characterization. Here, we diagnose the conductance and thermal effect of graphene electrode junctions constructed from GRs of various widths and directions under gate-tuned voltages. On applying partial gate voltages, we identify the effect of local potential variance on the entire graphene electrode junction. As a result, we were able to perceive precise and minute conductance variations for the entire graphene electrode, arising mainly from different sub-micrometer-scale widths of the GRs, which could not be distinguished using conventional global gating methods.

Introduction

Two-dimensional (2D) crystals such as graphene or transition metal dichalcogenides (TMDCs) have been favored for atomically thin electronic applications demanding high charge-carrier mobility, large on–off ratios, and the capability of overcoming short-channel effects.[1–12] In particular, graphene is suitable for use in interconnections and waveguide electrodes between atomically thin electrical and optical devices in flexible, transparent, high-performance circuits.[10–19] To achieve high performance from 2D semiconductor field-effect transistors (FETs), we should overcome the tremendous contact resistance of the 2D semiconductor channel with conventional metal electrodes, which degrades the carrier-transport performance. Graphene has been employed as an electrode for decreasing contact resistance, because the Fermi levels of the 2D crystal channel and the graphene electrode are close.[8,10–15] Moreover, when graphene with atomic thickness and high conductivity is used as an optical waveguide electrode on flexible and transparent devices, the conductivity of the graphene waveguide reflects the shape of the guided optical wave and its efficiency.[16–19] Thus, the conductivity of graphene electrodes depends on variations in dimensions such as width and is an important factor for nanometer-scale applications in electrical and optical devices. There have been several reports on the theoretical and experimental characterization of variations in the conductance of individual graphene ribbons (GRs) without width variations, on the application of an electrically global gating condition.[20–26] However, these studies have focused mainly on ultra-narrow (∼ a few nanometers wide) graphene nanoribbon structures with quantized conductance variations ascribed to localized state effects. For the application of graphene in interconnections of 2D crystal FET arrays, the adaptable dimensions (∼ sub-micrometer width) of the GRs used in the electrodes should be confirmed with predictable conductance variations. Therefore, direct measurement of the partially nanoscale width-difference-dependent conductance variation of the entire GR junction electrode is necessary. A scanning probe microscope (SPM) can be used to perform nanoscale graphene surface characterization.[27,28] In particular, upon applying an electric gate on desired nanoscale GR areas *via* a conductive SPM probe, we can investigate the direct effect of individual GR widths on the entire GR junction electrode conductance, which is not revealed by applying a global gating avenue.

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In this work, to diagnose the effect of sub-micrometer variations in GRs on conductance, we demonstrate junction structures composed of GRs with various widths. We investigate the conductance variation as a function of width by applying electrical biases and gate voltages. As a result, while conductance variations generally expected for GR junctions with a sub-micrometer width range, on the application of a global gating voltage through the SiO_2 substrate, are from 40% to 69%, we could detect precise and minute conductance variations (ranging from 0.3% to 3.0%) over the GR junction, which were contributed by individual GRs on applying a partial gating voltage with a conductive SPM probe.

Results and discussion

To investigate width-dependent conductance variations in graphene electrodes, we employed GR junctions with different widths (Fig. 1(a)). The GR junctions were prepared using polymethyl methacrylate (PMMA) e-beam resist as an etch mask in an oxygen plasma etching process, which removed the unprotected graphene (for more details see the Experimental section and ESI, Fig. S1 and S2†). The widths of GR ranged from 100 to 500 nm, targeting sub-micrometer scale interconnection electrodes. For the interconnection applications of graphene electrodes in high-density device arrays, there should be sub-micrometer scale variations in the width and direction. Therefore, we employed various GR junction devices with widths ranging from ~95 to ~470 nm, lengths ranging from 4.0 to 5.5 μm, and directions differing between types (I), (II), and (III) (Fig. 1(a)). The GR junctions were terminated with a gradually widening graphene area in contact with Cr/Au electrodes. On applying a global back-gate voltage V_{BG} (Fig. 1(b)), the observed transport characteristics of the type (I) GR junction (Fig. 1(a)) exhibited slightly p-doped behavior with a charge-neutral position V_{CNP} = 18.5 V (Fig. 1(c)). Here, the carrier density ($\bar{n} = 2.61 \times 10^{12}$ cm^{-2}) induced in graphene by the charged impurities was extracted by correlating the currents obtained through experiments and simulations of the entire GR junction under the biased voltage V_{DS} (for more details of the calculation of $\bar{n}$, see the Experimental section and ESI†). We also calculated similar $\bar{n}$ = 2.64×10^{12} cm^{-2} and 2.48×10^{12} cm^{-2} for type (II) and (III) GRs with V_{CNP} = 12.5 V and 13.7 V, respectively (see ESI, Fig. S3 and S4†). As a result, the initial Fermi level (E_0) in the proposed schematic diagram in the inset of Fig. 1(c) could be calculated as $E_0 = \hbar\nu_F(\bar{n}\pi)^{1/2}$ = 188 meV for the graphene in type (I). Similarly, E_0 for types (II) and (III) was estimated as 190 meV and 184 meV, respectively. Here, $\hbar$ and $\nu_F = 1 \times 10^6$ m s^{-1} are the Planck's constant and Fermi velocity of graphene, respectively. As the transport curve in Fig. 1(c) was measured by applying V_{BG} through 280 nm thick SiO_2 dielectric layers, $\bar{n}$ was the averaged initial carrier density of the entire GR junction structure. Therefore, we can employ this transport curve as a reference for the conductance variation by applying a gate voltage. A more precise inspection, such as that using SPM, can be employed for confirming the conductance variation for the entire GR junction, caused by individual GRs with different widths, on the application of a gate electric field (Fig. 1(b)).

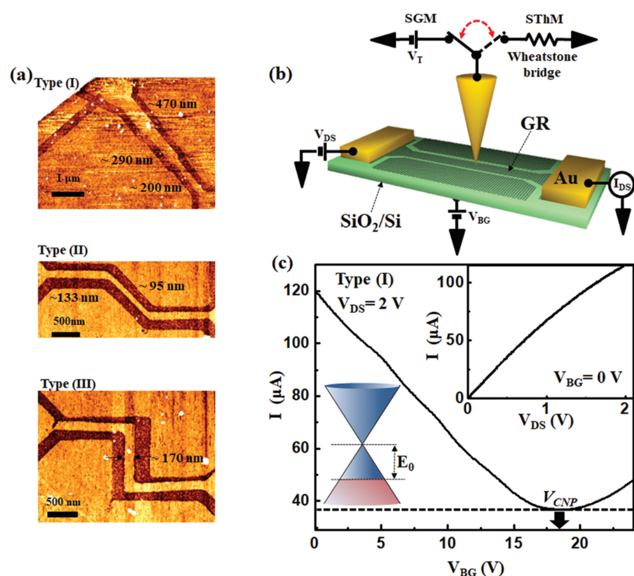

Fig. 1 (a) GR junction structures. Type (I): Straight GR junctions with widths of ~470, 290, and 200 nm. Type (II): a 45° path-changed GR junction with ~133 nm wide sides and a ~95 nm wide center. Type (III): a 90° path-changed GR junction with ~170 nm wide sides and a ~170 nm wide center. The lengths of the GRs in each type of sample are approximately 1 μm. (b) Schematic diagram of a GR FET on SiO_2/Si and its conductance, SGM, and SThM measurements. (c) Current variation of the GR junction of (a) type (I) as a function of global back-gate voltage (V_{BG}). Here, there is a level marker (dashed line and arrow) for checking the charge neutral position (V_{CNP}). Inset: Current variation of the GR junction as a function of bias voltage (V_{DS}) and schematic diagram of graphene energy potential exhibiting slightly p-doped behavior with E_0.

Fig. 2(a) shows an electric field microscopy (EFM, V_{EFM}) image of a GR junction with V_{DS} = 0.5 V. Here, the represented GR junction is type (I), as shown in Fig. 1(a), constructed with 470, 290, and 200 nm widths and ~1 μm length for the individual GRs. In the EFM image exhibiting the conductance of the graphene area (Fig. 2(a)), the electrical isolation of the GR junctions from the initially exfoliated graphene flakes corresponding to the AFM image of type (I) (Fig. 1(a)) is guaranteed and a gradually sloping electric potential is observed between the ends of the GR junction marked with A and B (Fig. 2(a)), owing to the application of a bias voltage V_{DS} = 0.5 V. Here, we can observe that the variation of the potential is the largest in the widest part of the GR due to a larger electric field, exhibiting greater slope for GR with 470 nm width than for GR with 290 and 200 nm widths (see ESI, Fig. S5†). Although the width-dependent Joule self-heating temperature difference (ΔT = 5 to 15 K for 470 to 200 nm width with V_{DS} = 2 V) in the GR junction was not large, the ΔT variation agreed well with the conductance of the GR junctions, as a function of width and V_{BG} (Fig. 2(b) and (c), respectively; see also ESI, Fig. S3 and S4†).

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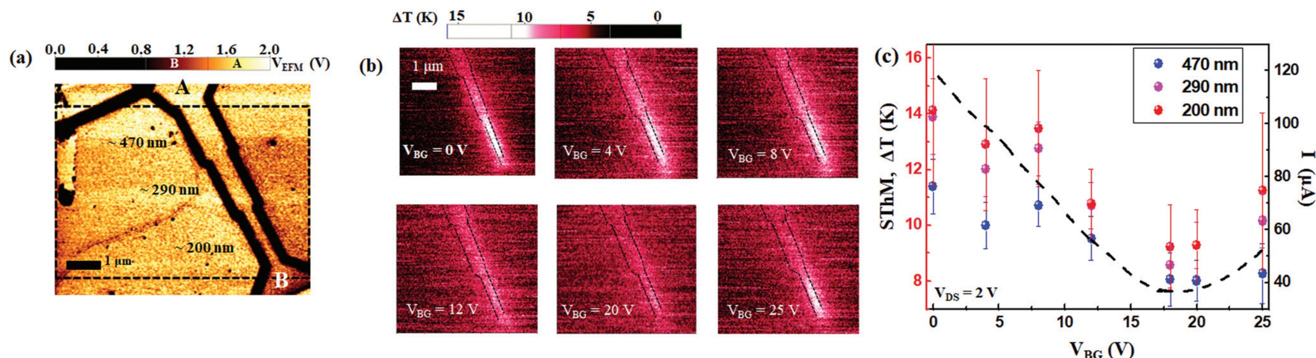

Fig. 2 (a) EFM image of applying V_{DS} = 0.5 V for the type (I) GR junction shown in Fig. 1. Here, the points marked A and B in the color scale bar correspond to $\Delta V_{EFM} \sim 0.5$ V for positions marked by A and B on the EFM image of the GR junction and the dashed box indicates the same area of (b) SThM and (Fig. 3) SGM images. (b) Temperature distribution images of a Joule self-heated type (I) GR junction for applied V_{DS} = 2 V and V_{BG} = 0–25 V. (c) Temperature variation at GR widths of 200 nm (red dots), 290 nm (purple dots) and 470 nm (blue dots), as a function of V_{BG}. Temperature values were extracted from (b) SThM images as a function of V_{BG}. The current variation (dashed line) of the GR junction as a function of V_{BG} is the same as that in Fig. 1(c).

This indicates that the width-dependent conductance of GR is dominant among the electrical and thermal properties of a GR junction.

For the direct measurement of the gate voltage contribution to the individual conductance of the GR in the junction structure constructed with different widths or directions, we employed scanning gate microscopy (SGM) (Fig. 1(b)).[27–31] By applying a partial gate voltage to each different strip width area, the conductance variation of the GR junction contributed by the ribbon structure could be investigated, as shown in Fig. 3(a–c). From the SGM measurements, by applying a partial gate voltage $V_T = \pm 8$ V using a conductive SGM probe at a constant height of 100 nm, we deduce the Fermi level of the GR junction tuned in the hole-doping region to be $E_0 \pm \Delta E_T = \hbar \nu_F[(\bar{n} \pm \Delta n)\pi]^{1/2}$ = 169–206 meV by roughly estimating $\Delta n = C_{Air} \cdot V_T / e = \pm 0.5 \times 10^{12}$ cm^{-2}, as proposed in the schematic diagrams in the inset of Fig. 3(a) and (b), where Δn and C_{Air} are the charge-carrier density induced by applying a gate voltage (V_T or V_{BG}) and capacitance of air with 100 nm distance between the SGM probe and GR, respectively. Based on this charge-carrier density variation of graphene, induced by V_T, the SGM images of the GR junctions (Fig. 3(a) and (b)) exhibited a width dependency leading to conductance variations around $(I - I_0)/I_0$ = 0.29% to 0.94% for widths between 470 and 200 nm (see Fig. 3(c)). Here, I and I_0 are the current values of the entire GR junction, with and without a gating voltage applied over individual GR areas, respectively. The $(I - I_0)/I_0$ values used in this work were absolute values for comparing the variations as a function of the width and gate voltage.

GR junction structures of various widths and paths have been fabricated and characterized (Fig. 1(a) and Fig. S2†), and we confirmed that the width variation was significantly more dominant than the path change for our specimens. Namely, although type (II) and (III) GR junctions with a ribbon of 1 μm length had path changes of 45° and 90°, respectively, variations were not observed in the transport characteristics

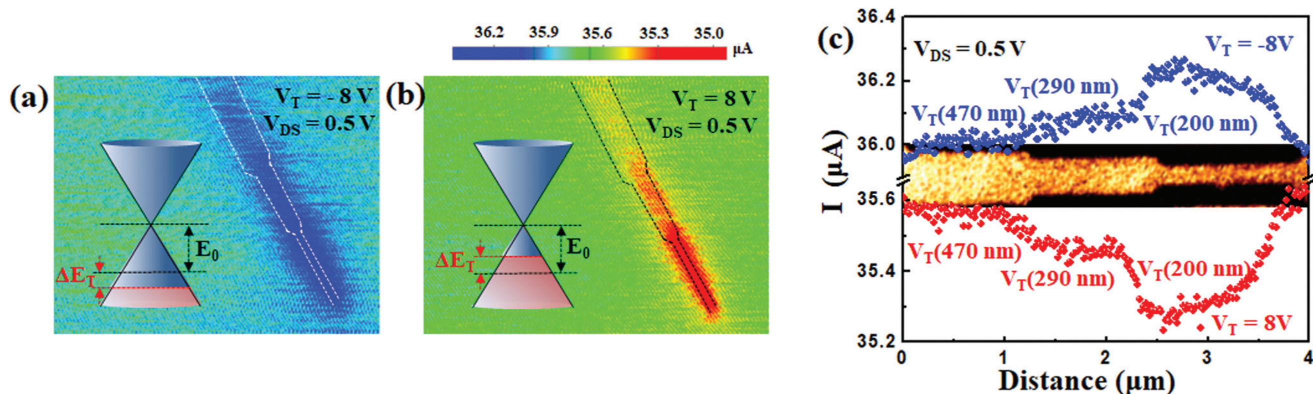

Fig. 3 (a) and (b) SGM images for $V_T = \pm 8$ V for the type (I) GR junction biased by V_{DS} = 0.5 V. Inset: Schematic diagrams of graphene energy potential exhibiting doping change with $E_0 \pm \Delta E_T$. (c) Conductance profiles of (a) and (b) SGM images along the GR junction. Here, the V_T (470 nm), V_T (290 nm), and V_T (200 nm) marks indicate the partial gating by V_T on individual GRs with widths of ~470 nm, ~290 nm, and ~200 nm, respectively. The cropped EFM image of Fig. 2(a) is shown at the center of the plots for correlating current variations with GR features.

owing to a short mean free path in graphene on SiO_2 (see ESI, Fig. S3 and S4†).[13,32–35] Note that, upon employing the ballistic conditions for suspended graphene or graphene on a hexagonal boron nitride (hBN) substrate, which can suppress charge impurities and improve carrier mobility above 500 000 $cm^2 V^{-1} s^{-1}$, the mean free path can be increased to micrometer scales.[32–35] However, our GR junctions on SiO_2 possessing a few hundred nanometers width and few micrometers length, exhibited a carrier mobility of approximately several thousand $cm^2 V^{-1} s^{-1}$ (*i.e.*, 2000 to 4000 $cm^2 V^{-1} s^{-1}$ for 2.61×10^{12} cm^{-2} of the hole carrier density region for our specimens) because of the electron–hole puddles created by the SiO_2 substrate. Therefore, the mean free path should have been smaller than 1 µm. Conventional dielectric substrates such as SiO_2 lead to short mean free paths and do not allow path-dependent transport variations in graphene. On the other hand, because we observed substantial width-dependent conductance variations (see also ESI, Fig. S3 and S4†), we focused our analysis on the width-dependent conductance variations of GR junctions on the application of gate voltages.

For comparing the electric-field effect on the GR/SiO_2 structure by gating either V_T or V_{BG} (Fig. 4(a)), we numerically calculated electric potential distributions, reflecting notably different electric potential distributions between the GR and the dielectric areas under gating of either V_T or V_{BG} in Fig. 4(b) or (c), respectively (for details of the calculations, see the Experimental section and ESI, Fig. S6–S8†). Applying V_T = 8 V *via* the SGM probe at a distance of 100 nm from the GR surface created an electric potential at the exact desired position of the GR, with almost invariant electric potential of the SiO_2 substrate (see Fig. 4(b)). The global gating voltage V_{BG} = 8 V applied through the 280 nm thick SiO_2 substrate caused a doping change in the entire GR in both SiO_2 and air (see Fig. 4(c)). As a result, the global gating voltage V_{BG} produced a carrier-density change over the entire GR area, as shown by the large carrier density $\Delta n \sim 1.54 \times 10^{12}$ cm^{-2} at the center of the GR (x = 0) (Fig. 4(d–f)). On the other hand, the application of V_T by the SGM probe induced a carrier density change in graphene, which could be exactly ascribed to the SGM probe position ($x = y = 0$ nm), as well as its rapid suppression on increasing $|y|$ (red line in Fig. 4(e)), while Δn by V_{BG} was invariant along the length direction (blue line in Fig. 4(e)). Furthermore, we found that Δn under both V_{BG} and V_T was enhanced at the edge of the GR owing to the geometry, the state of the graphene edge, and the electric field strength.[26] The Δn for V_T was slightly smaller than that for V_{BG}, albeit the SGM probe was applied at the GR edge (see also ESI, Fig. S7†). Here, although the GR with 100 nm width is representatively exhibi-

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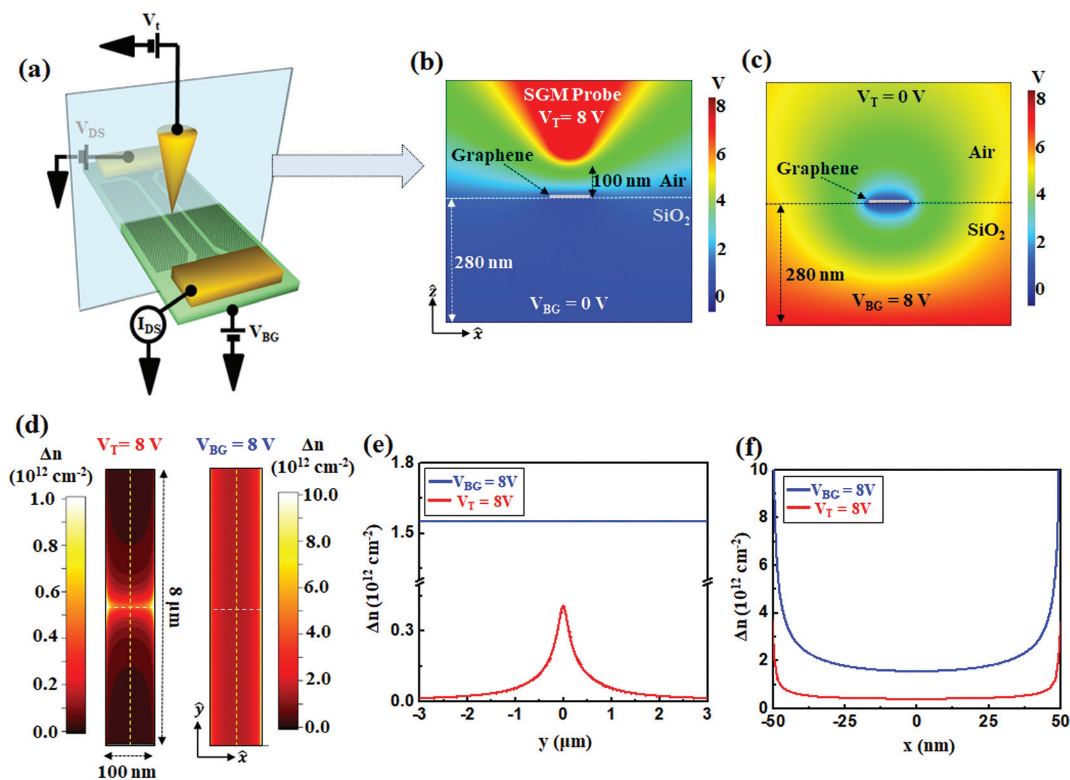

Fig. 4 (a) Schematic diagram of SGM measurements of GR and the marked vertical cross-section area between the SGM probe and GR. (b) and (c) Simulation of the electric potential distribution (for the marked vertical cross-section area in (a)) between the SGM probe and the represented GR with 100 nm width on a SiO_2 substrate by applying either (b) V_T or (c) V_{BG}. (d) Simulation of the spatial distribution of the induced carrier density (Δn) for GR with 100 nm width by applying either (b) V_T or (c) V_{BG}. (e) Simulated cross-section profiles of Δn along GR length direction (marked by dashed lines along the y-direction in (d)) by applying either V_T (red line) or V_{BG} (blue line). (f) Simulated cross-section profiles of Δn along the GR width direction (marked by dashed lines along the x-direction in (d)) by applying either V_T (red line) or V_{BG} (blue line).

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ted in Fig. 4, we calculated and employed Δn for all width conditions from 500 nm to 100 nm, with the aim of extracting the conductivities of the GR junctions (see ESI, Fig. S8†).

Since the global gate-induced large Δn derived the conductivity of graphene $\sigma_{GR\text{-}BG}$, $(I - I_0)/I_0 = (\sigma_{GR\text{-}BG} - \sigma_{GR0})/\sigma_{GR0}$ as a function of width (W) for the GR under global gating V_{BG} = 8 V was assumed to vary from ∼40% for W = 500 nm to ∼69% for W = 100 nm, owing to the large electric field over the entire GR area through both air and the SiO_2 substrate by global gating, where $\sigma_{GR\text{-}BG}$ and σ_{GR0} are the conductivities of GR under V_{BG} = 8 V and 0 V, respectively (see the inset of Fig. 5(a) and ESI, Fig. S9†). Under the global gating of V_{BG} (*i.e.*, when applying an electric field to the entire graphene nanoribbon structure), the behavior of conductance variation of the narrowest nanoribbon part (< several tens of nanometers) was dominant. Therefore, the previously reported research concept was employed for focusing the analysis of conductivity on the narrowest target graphene nanoribbon area alone.[22–25] However, for graphene electrodes constructed with subtle differences in width (∼ several hundreds of nanometers) of the GR junctions, since each partial width difference dominantly contributed to the conductance variation of the entire GR junction, global gating was unsuitable for the inspection of each partial width-difference-dependent conductivity of the entire GR electrode junction. Based on the gate-tuned Δn in Fig. 4, which employed enough length of Δy to reflect almost the entire induced carrier density over the GR length, the conductivities $\sigma_{GR\text{-}T}$ of GR could be extracted as a function of W on the application of V_T (Fig. 5(a), for more details see the Experimental section and ESI, Fig. S9 and S10†). The $\sigma_{GR\text{-}T}$ and σ_{GR0} under V_T = 8 V and 0 V exhibited suppression and invariance, respectively, as a function of W (Fig. 5(a)), which led to a conductance variation from 1.7% for W = 500 nm to 4.1% for W = 100 nm, according to the relationship $(I - I_0)/I_0 = (\sigma_{GR\text{-}T} - \sigma_{GR0})/\sigma_{GR0}$ (see the solid line in Fig. 5(b)). Here, the $\sigma_{GR\text{-}T}$ for V_T = 8 V and σ_{GR0} for V_T = 0 V was acquired by applying the averaged value of the induced carrier density $\bar{n}$ from type (I), (II), and (III) GRs (see ESI, Fig. S10†). Although similar to the suppression behavior of $(I - I_0)/I_0$ for increasing W, an offset was observed, when compared with the experimental results (black, red, and blue dots with a conductance variation from 0.29% for W = 470 nm to 2.8% for W = 95 nm). During SGM probe gating on the target GR, since the extra resistance (R_{ext}) included in other GR junctions under V_T = 0 was still connected, the total current in all GR junctions could be expressed as $I = V_{DS}/(R_{GR\text{-}T} + R_{ext})$, where $R_{GR\text{-}T} = L/(W \cdot \sigma_{GR\text{-}T})$ (for more details see the Experimental section and the section on the simulation of the conductance variation and electric potential of GR junctions in ESI, Fig. S9 and S10†). Upon employing theoretical fitting (dashed lines and the gray area in Fig. 5(b)) with the parameter R_{ext} = 7 to 13 kΩ, we confirmed the range of gradual escalation of $(I - I_0)/I_0$, depending on W for type (I) (blue dots), (II) (red dots), and (III) (black dots) GR junctions (Fig. 5(b)). In particular, because the $(I - I_0)/I_0$ of W ∼ 170 nm (black dots in Fig. 5(b)) for the type (III) GR junction, which included the cracked area leading to a few tens of nanometers width during fabrication (see ESI, Fig. S4†), corresponded well with the value of $(I - I_0)/I_0$ between ∼133 nm and ∼200 nm widths for type (I) and (II) of GR junctions, respectively, we can assume that the resistance of the crack area in the type (III) GR junction was within the range of 7 to 13 kΩ. This indicates that we can expect the conductance behaviors of the entire GR junctions with $(I - I_0)/I_0$ to be a function of the target GR width under various R_{ext} and V_T (see ESI, Fig. S11†). Consequently, although there is extra-GR with large resistance connected to the target GR, the analysis of the conductance contribution of the target GR to the entire GR junction is guaranteed by SGM characterization, while global gating methods such as those reported previously[20–26] are limited to the measurement of the width-dependent conductance for individual GRs constructed with invariant width.

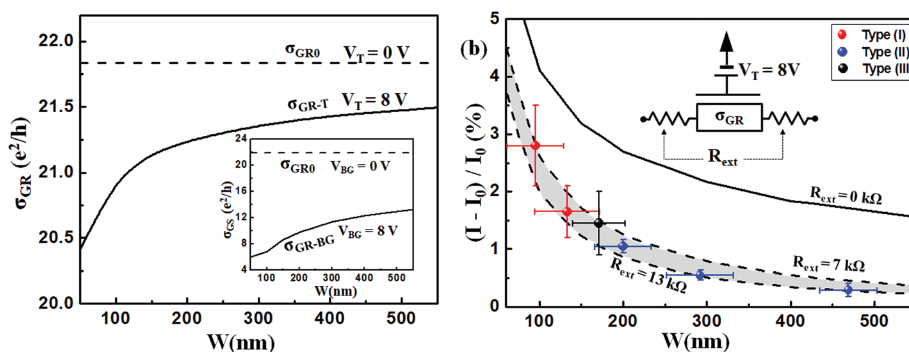

Fig. 5 (a) Conductivities of the GR (σ_{GR}) as a function of width (W) on the application of either V_T = 0 V (dashed line) or 8 V (solid line) marked with σ_{GR0} or $\sigma_{GR\text{-}T}$, respectively. Inset: σ_{GR} as a function of W on the application of either V_{BG} = 0 V (dashed line) or 8 V (solid line) marked with σ_{GR0} or $\sigma_{GR\text{-}BG}$, respectively. (b) Current variation around $(I - I_0)/I_0$ as a function of the GR width from ∼95 nm to ∼470 nm and its theoretically fitted results on the application of V_T = 8 V (dashed line). Here, $(I - I_0)/I_0$ for each width was extracted from the AFM and SGM images of GR type (I) (blue dots), type (II) (red dots), and type (III) (black dots) shown in Fig. 1, 2 and Fig. S3, S4.† Here, the calculated lines were extracted for the GR junction structure (dashed lines and the gray area) or the individual GR structure (solid line) with the parameters of R_{ext} = 7 to 13 kΩ or 0 kΩ, respectively. Inset: Schematic diagram of the GR connected with the R_{ext} structure on the application of V_T.

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Conclusions

We studied the conductance variations in GR junctions under different widths and directions, and the Joule heating conditions under the application of different biases and gate voltages. While there were no effects observed due to the direction, the conductance and thermal variations of the GR junction varied between 2.8% and 0.29% and 24 K and 5 K, respectively; these values are minute for widths of 95 nm to 470 nm. Furthermore, we confirmed that the width dependency of the GR contributed directly to the conductance variation of the entire GR junction. This gate-tuned conductance variation of GR with sub-micrometer widths allows us to obtain a predictable and precise characterization of graphene electrodes for nanoscale interconnection applications in high-density array electronics.

Experimental methods

Fabrication of GR FETs

To prepare the GR junction structure, single-layer graphene FETs were fabricated by mechanical exfoliation of Si wafers covered with ~280 nm thick SiO_2. Then Cr/Au electrodes (0.5 nm/40 nm thickness) were made to come into contact by standard e-beam lithography. For defining the dimensions of the GR junctions, we employed an e-beam resist of PMMA. By etching away the unprotected graphene area between the PMMA etch mask using oxygen plasma, we could isolate the GR junction area from the graphene flakes (see ESI, Fig. S1†). The GR junction devices were annealed at 320 °C to 360 °C in a hydrogen/argon gas mixture for two hours to remove the PMMA residue on the graphene surface. This manufacturing process allowed us to prepare various GR junction devices with widths ranging from ~95 to ~470 nm and lengths ranging from 4.0 to 5.5 μm (see also ESI, Fig. S2†).

Scanning probe microscopy characterization

To elucidate the spatial formation tendencies of graphene, SPM measurements were performed using a commercial atomic force microscope (XE-100, Park Systems Corp.) in air at room temperature. While observing EFM data, we applied an AC voltage of amplitude ~0.5 V, a DC voltage of 1 to 2 V, and a frequency of 17 kHz to a Cr/Au coated probe. The EFM images were obtained by a two-way scan method to avoid topographic artifacts. The first scan was for topography in the noncontact mode with a dithering resonant frequency of ~120 to 170 kHz, and the second scan was for an EFM image using the ~100 nm constant height mode. For observing the SGM image, we applied a gate voltage V_T *via* a metal-coated SPM probe at a constant height of ~100 nm.[27,28] Upon applying V_T on individual GR areas, the conductance of the entire GR junction structure was observed by the normal 2-probe measurement between the electrodes at each end of the entire GR junction. Scanning thermal microscopy (SThM) experiments were carried out by monitoring the resistance variation of a high-resolution thermistor on the SPM tip connected to a Wheatstone bridge circuit. The resistance of the SThM probe was calibrated on an absolute-temperature scale by employing Raman spectroscopy of graphene that included the temperature of the G-mode phonon.[28,36] First, we measured the SThM signal induced by the off-balance of the Wheatstone bridge signal under a graphene applied bias voltage. Then, the temperatures of the G-mode phonons (T_G) of the graphene applied bias voltage were obtained from the ratio of the anti-Stokes and Stokes signals through the relationship $I_{aS}/I_S = C\exp(-\hbar\omega_G/k_BT_G)$, where $\hbar\omega_G$ is the G-phonon energy (~195 meV), k_B is the Boltzmann constant, and C is a previously determined numerical factor.[36] Finally, by comparing the SThM signal and the T_G of graphene under the same bias voltage, we calibrated the resistance unit of the SThM signal with the absolute-temperature unit.[28]

Conductivity model for graphene

We employed the following description of the conductivity of graphene in this work:

$$\sigma \approx \begin{cases} 20\dfrac{e^2}{h}\dfrac{(\Delta n+\bar{n})}{n_i} & \text{for } \Delta n+\bar{n} > n^* \\ 20\dfrac{e^2}{h}\dfrac{n^*}{n_i} & \text{for } \Delta n+\bar{n} < n^* \end{cases},$$

where Δn, $\bar{n}$, n_i, and n^* are the gating (V_T or V_{BG})-induced carrier density (externally induced), carrier density induced in graphene by the charged impurity (internal characteristic of graphene), charged impurity concentration, and self-consistent residual carrier density considering electron and hole puddle formation by the charged impurities, respectively.[37,38] For a given n_i, $\bar{n}$ and n^* were determined by the relationship:

$$\frac{n^*}{n_i} = 2{r_s}^2 C_0^{\mathrm{RPA}}(r_s, a = 4d\sqrt{\pi n^*}), \quad \bar{n} = \frac{{n_i}^2}{4n^*},$$

where $C_0^{\mathrm{RPA}}(r_s,a) = -1 + 4E_1(a)/(2+\pi r_s)^2 + 2e^{-a}r_s/(1+2r_s) + (1+2r_sa)e^{2r_sa}(E_1[2r_sa] - E_1[a(1+2r_s)])$ and $E_1(z) = \int_z^\infty t^{-1}e^{-t}\mathrm{d}t$ (the exponential integral function). The effects of both dangling bonds on SiO_2 and the undesired residues on the graphene surface leading to the doping of graphene were reflected in the variables $r_s \approx 0.8$ (graphene on a SiO_2 substrate) and $d \approx 1$ nm (distance between graphene and a plane where charged impurities lie).[33,34] The above graphene conductivity description was established under the assumption of zero temperature. However, our graphene sample's Fermi level was approximately 188 meV for type (I) GR, which translated to a Fermi temperature of $T_F = E_F/k_B = 2187$ K. Type (II) and (III) GRs also exhibited similar conditions. This was approximately seven times higher than room temperature (300 K). Therefore, the conductivity model described above was applicable to our study constructed under room temperature.[37]

Simulation of the gate (V_T or V_{BG})-tuned conductance of GR

To simulate the GR with tip or back gating, we solved the Maxwell equations for electric potential under the electrostatic situation. We regarded graphene and Si substrate as a conduc-

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tor and put the metallic tip above the GR (see ESI, Fig. S6†). By applying a gate voltage to the metallic tip surface or the Si substrate, the surface charges on graphene were acquired by differentiating the electric potential near the graphene surface. The calculated charges were regarded as additional carriers in graphene; thus, the conductivity of graphene formed a spatial distribution. The effective conductivity (averaged conductivity) of the GR could be expressed as follows:[22]

$$\sigma_{\text{eff}} = \left(\iint \frac{1}{\sigma_{\text{local}}} \mathrm{d}A\right)^{-1},$$

where σ_{local} is the conductivity on the local area of graphene. Since our GR specimens were gate tuned, we marked the effective graphene conductivity as $\sigma_{\text{GR-T}}$, $\sigma_{\text{GR-BG}}$, and σ_{GR0} for the applied gate voltages of V_{T} (tip-gating), V_{BG} (back-gating), and 0, respectively. The current was $I = V_{\text{DS}}/(R_{\text{GR}} + R_{\text{ext}})$ and $R_{\text{GR}} = L/(W{\cdot}\sigma_{\text{GR}})$, we could extract the conductance of the GR and conductance variation as $1/R_{\text{GR}}$ and $(I - I_0)/I_0 = [\{1/(W{\cdot}\sigma_{\text{GR0}}) + L{\cdot}R_{\text{ext}}\}/\{1/(W{\cdot}\sigma_{\text{GR-G}}) + L{\cdot}R_{\text{ext}}\}] - 1$, where L and W are the length and width of the GR, respectively.

Conflicts of interest

There are no conflicts to declare.

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