RSC Advances

PAPER

View Article Online
View Journal | View Issue

Cite this: *RSC Adv.*, 2018, **8**, 13917

Polymer–carbon dot hybrid structure for a self-rectifying memory device by energy level offset and doping

Hang Lu, Yingying Chen, Qing Chang, Shuai Cheng, Yamei Ding, Jie Chen, Fei Xiu, Xiangjing Wang, Chaoyi Ban, Zhengdong Liu, Juqing Liu* and Wei Huang*

Received 5th March 2018
Accepted 31st March 2018

DOI: 10.1039/c8ra01928b

rsc.li/rsc-advances

A strategy for self-rectifying memory diodes based on a polymer–carbon dot hybrid structure, with a configuration of rGO/PEDOT : PSS/carbon dots/MEH-PPV/Al, has been proposed. The fabricated device exhibits a rectification of 10^3 in the rectification model and an ON/OFF current ratio of 121 in the memory model. The rectifying behavior was attributed to an energy level offset between the electrodes and the bilayer polymers and the memory effect was induced by carrier trapping of carbon dots within the polymers.

Polymer-based resistive switching memory devices, as ideal candidates for future emerging memory devices, have attracted a great deal of attention due to their simple structure, tunable properties, high-density integration, low-power consumption, facile fabrication process, and low-cost potential.[1–4] Generally, a cross-bar architecture in memory arrays has been designed to achieve high-density data storage.[5–8] However, the sneaking current issue, which is caused by a cross-talk effect in the cross-bar array, results in a misreading of a cell in a high resistance state (HRS) when the neighboring cells are in a low resistance state (LRS).[9–13] To alleviate the sneaking current issue, great effort has therefore been devoted to the search for a memory device with a rectifying effect. For example, the architecture of one diode-one resistor (1D1R) or one transistor-one resistor (1T1R) can improve reading accessibility in an integrated memory array structure.[11,12,14,15] However, they still suffer from limitations of complex device structure, fabrication process, low yield and high energy consumption,[16] which could be circumvented by creating a self-rectifying memory device with a simple sandwich architecture and solution process fabrication.

Self-rectifying memory devices with metal/insulator/metal structure have risen as an important class of memory technology in high density data storage. Numerous transition metal oxide materials, *e.g.*, Cr-doped $SrTiO_3$,[16] $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO),[17] ZrO_2,[18] TiO_2,[19] HfO_{2-X},[20,21] and TaO_X,[22] and Si-based materials, *e.g.*, a-Si[23,24] and Si_3N_4,[25] can serve as the insulator layer and exhibit excellent self-rectifying memory features such as short switching time, large resistance ratio, and good retention ability. Unfortunately, most devices are fabricated by traditional film plating technology such as pulsed laser deposition, electron beam deposition, sputtering deposition and thermal evaporation, leading to very complicated process. Nowadays, polymer rectifying devices by energy level offset[26,27] and memory devices by doping method[28,29] have been widely fabricated, with the merit of solution process. Therefore, combining energy level offset and doping technique in solution processed polymer diodes are anticipated to achieve self-rectifying memory performance.

In this letter, we reported a solution processed polymer–carbon dots hybrid structure for self-rectifying memory device by energy level offset and doping method, with a configuration of reduced graphene oxide (rGO)/poly(3,4-ethylenedioxythiophene) : poly(styrenesulfonate) (PEDOT : PSS)/carbon dots/poly(2-methoxy-5(2′-ethyl)hexyloxy-phenylenevinylene) (MEH-PPV)/Al. Bilayer PEDOT : PSS and MEH-PPV are used as the rectifying active layers due to their energy level offset with electrodes. Carbon dots are doped as the memory active layer due to their carrier trapping behavior within polymers. rGO film as bottom electrode and Al as top electrode are fabricated by thermal annealing and thermal evaporation, respectively. The fabricated device in a 6 × 6 cross-bar array exhibits rectifying function with a rectifying ratio of 10^3, and also possesses stable memory effect with a minimum ON/OFF current ratio of 121. Our strategy is promising for preparation of other polymer–nanoparticle hybrid structures for self-rectifying memory devices.

The self-rectifying memory devices were fabricated basing on a facial solution-based process as shown in Fig. 1. The patterned rGO electrodes with a square resistance of 1 kΩ sq^{-1} were fabricated from solution-processed GO films *via* an oxygen-plasma etching approach.[30,31] A 30 nm-thick PEDOT : PSS layer was spin-coated on rGO electrode surface, then treated

Key Laboratory of Flexible Electronics (KLOFE), Institute of Advanced Materials (IAM), Jiangsu National Synergistic Innovation Center for Advanced Materials (SICAM), Nanjing Tech University (NanjingTech), 30 South Puzhu Road, Nanjing 211816, P. R. China. E-mail: iamjqliu@njtech.edu.cn; iamwhuang@njtech.edu.cn

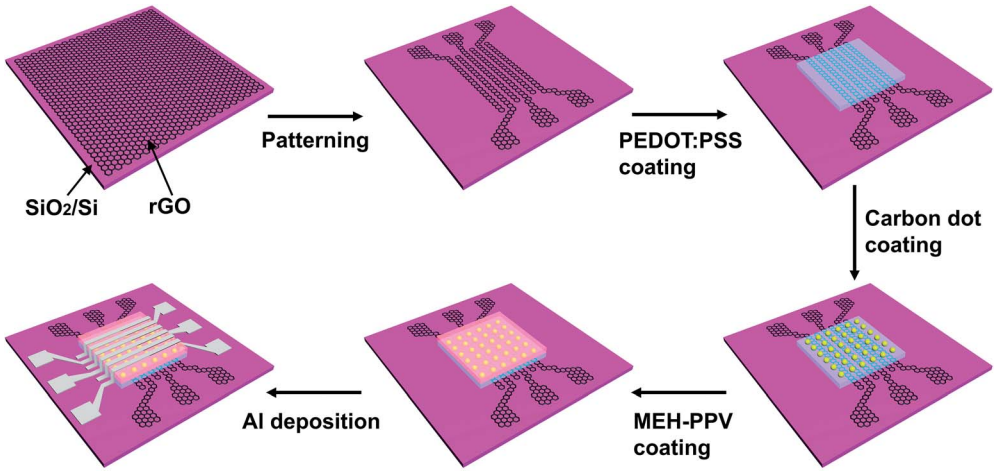

Fig. 1 Schematic diagrams of the fabrication process for rGO/PEDOT : PSS/carbon dots/MEH-PPV/Al self-rectifying memory devices.

with 20 W oxygen-plasma for 20 s, followed by thermal annealing in air at 120 °C for 20 min. The carbon dots aqueous with a concentration of 3 mg ml^{-1} was spin-coated onto PEDOT : PSS layer at 3000 rpm and subsequently annealed at 100 °C for 20 min. Subsequently, a 30 nm-thick MEH-PPV layer was spin-coated and then annealed in a N_2 gas environment at 70 °C for 30 min. Finally, 6 Al lines of 500 μm in width were deposited perpendicularly to rGO lines, through a shadow mask *via* thermal evaporation. Electrical properties of the as-fabricated devices were investigated using a semiconductor parameter analyzer (Keithley 4200) in the ambient environment.

To illuminate that the memory effect is caused by the carrier trapping effect of carbon dots, the rectifying device without carbon dots was fabricated and characterized (Fig. 2(a)). The current–voltage (*I*–*V*) characteristics of the rectifying diode device are shown in Fig. 2(b). Basing on optimal fabrication conditions, the rectifying diode device with the optimized structure exhibited a maximum rectification ratio (RR) of ~10^3 following RR = $|I_{forward}/I_{reverse}$ (here – $I(V-)/I(V+)$)|.[32] This rectifying effect is attributed to the Schottky barrier between Al electrode and MEH-PPV layer when a negative bias is applied to the rGO electrode. As is shown in the energy band diagram (Fig. 2(c)), the work function of rGO and Al is 4.8 eV and 4.3 eV, respectively. The highest occupied molecular orbital (HOMO) of PEDOT : PSS and MEH-PPV occurs at 5.2 and 5.1 eV, respectively. In this case, during the positive voltage sweep, holes from the rGO electrode can be efficiently injected into the HOMO of PEDOT : PSS layer with a 0.4 eV barrier height. On the other hand, when applying a negative voltage, it's difficult to realize the injection of holes from Al electrode to the LUMO of MEH-PPV layer due to a large barrier height up to 0.8 eV.

To obtain the self-rectifying memory effect, carbon dots are introduced as the memory active layer due to their carrier trapping behavior within polymers (Fig. 2(d)). Carbon dots were prepared by pyrolyzing citric acid as described elsewhere.[33] The

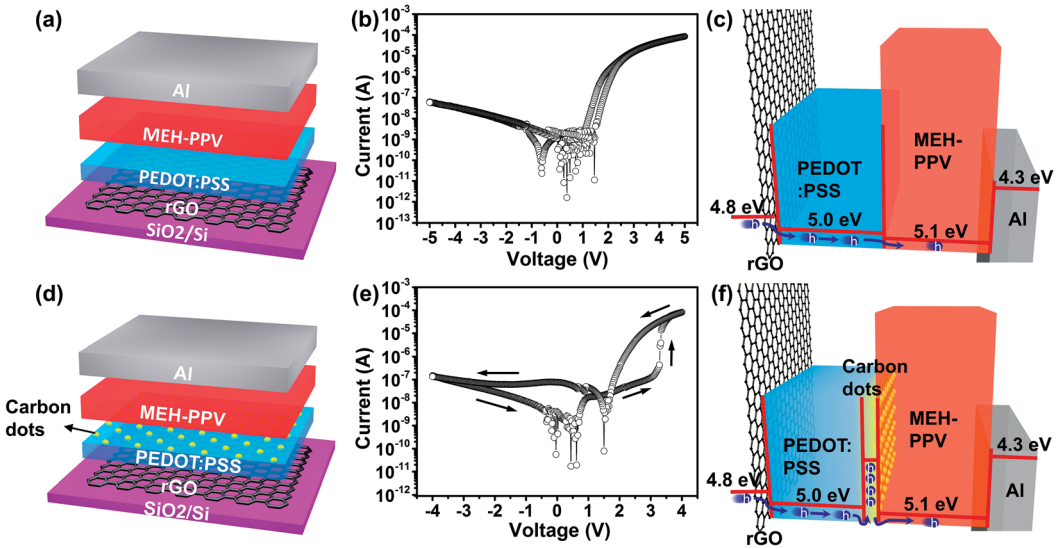

Fig. 2 (a) Schematic structure, (b) typical *I*–*V* characteristics and (c) energy band diagram of the rectifying device. (d) Schematic structure, (e) typical *I*–*V* characteristics (the arrows represent the sweep directions) and (f) energy band diagram of the rectifying memory device.

UV-vis absorption and PL spectra of carbon dot are demonstrated in Fig. 3(a), from which an apparent UV-vis absorption band centered at 335 nm is observed and the maximum PL emission occurs at a wavelength of 445 nm, suggesting their semiconductor properties. High quality TEM image shows that carbon dots have a diameter of ~4 nm (Fig. 3(b)), suggesting their strong ability to capture charges. Moreover, current–voltage (*I*–*V*) characteristics of the self-rectifying memory device are investigated and demonstrated in Fig. 2(e). When a negative bias was initially applied to the rGO bottom electrode, the device exhibited a high resistance state (HRS, namely OFF state). By applying a low positive voltage, the holes injected from rGO electrode were captured by carbon dots, the carbon dots served as trap centers due to the boundary and quantum confinement effect.[34] With the increase of sweep voltage, the injected carriers increase rapidly and the traps were nearly filled. When the power supply approaches the threshold voltage, the traps were filled completely, the device underwent a resistive switching from HRS to low resistance state (LRS, namely ON state). The device maintained a LRS with trap filling when the voltage swept from 4 to 0 V. The device exhibits rectifying effect at LRS due to the Schottky effect coming from the bilayer's energy level offset with electrodes. When the power was turned off, the captured charges might be released from the trap centers due to the shallow traps of carbon dots and the device returned to HRS.

The performance of the self-rectifying memory devices was evaluated under ambient conditions. Fig. 4(a) shows the typical *I*–*V* characteristics of the self-rectifying memory device under positive voltage sweep. The device could not maintain in the ON state steadily and it relaxed to the OFF state as once the power was removed, suggesting its volatile property. Fig. 4(b) shows the statistical distribution of ON-/OFF-state current (measured at 3 V) of the operative memory cells. The distribution of OFF- and ON-state current values lays within two orders of magnitude, the maximum currents at ON state and OFF state are about 10^{-4} and 10^{-7} A, respectively, with a ON/OFF current ratio of 10^2 to 10^3 : 1, reducing the misreading probability during the operation process. We also measured 40 randomly selected memory cells to evaluate the uniform distribution of switching threshold voltages, as shown in Fig. 2(c). The memory cells demonstrate an average value nearly 3 V of switching voltage. The retention time of the ON and OFF state with a continuous 3 V is measured in Fig. 4(d). The ON state can be maintained by applying a refreshing pulse of 4 V every 5 s, a slightly

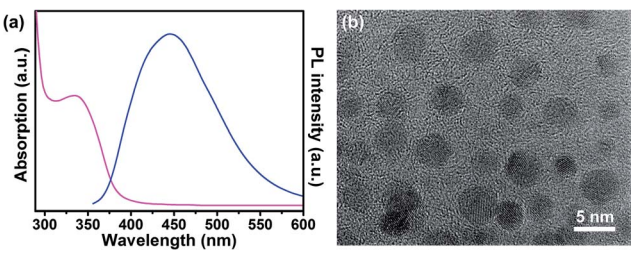

Fig. 3 (a) UV-vis absorption and PL spectra of the carbon dots. (b) TEM image of the carbon dots.

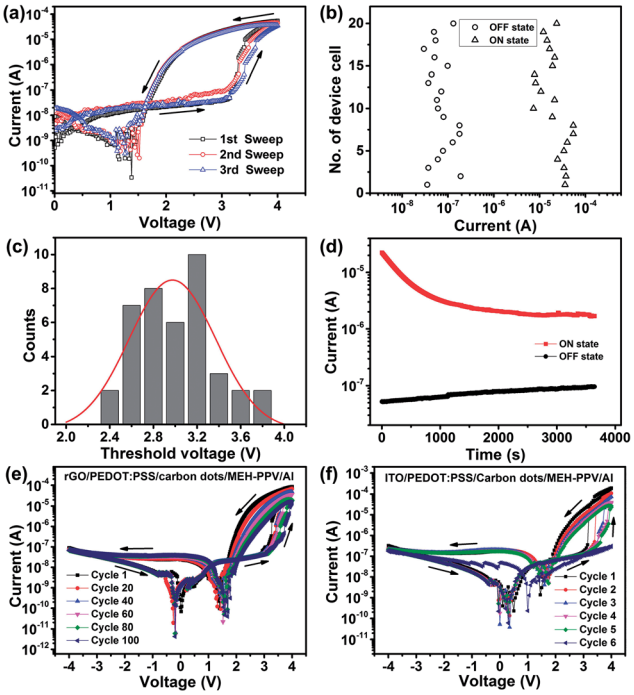

Fig. 4 (a) Typical *I*–*V* curves of the rGO/PEDOT : PSS/carbon dots/MEH-PPV/Al device. (b) Statistical distribution of the ON-/OFF-state currents measured at 3 V. (c) Statistics histograms of switching voltages of the rGO/PEDOT : PSS/carbon dots/MEH-PPV/Al devices from 40 memory cells. (d) Retention time for the rGO/PEDOT : PSS/carbon dots/MEH-PPV/Al device under a continuous positive bias stress. (e) Cycle endurance test of the rGO/PEDOT : PSS/carbon dots/MEH-PPV/Al device. (f) Cycle endurance test of the ITO/PEDOT : PSS/carbon dots/MEH-PPV/Al device. The arrows represent the sweep directions.

degradation was observed at the beginning and underwent stable with an ON/OFF current ratio of 30. The curves of first sweep in Fig. 4(e) and (f) indicated that both devices with the same structure basing on rGO electrode and ITO electrode can realize the self-rectifying memory effect, even though the former one exhibits higher endurance stability. After 100 consecutive voltage sweeps, the rectifying ratio of rGO/PEDOT : PSS/carbon dots/MEH-PPV/Al device still maintains 10^2 (Fig. 4(e)). Simultaneously, the ON/OFF ratio of the device at 3 V remained approximately 36. In contrast, the phenomenon of rectifier and memory gradually disappeared after six consecutive voltage sweeps for ITO based devices (Fig. 4(f)). This performance degradation was caused by the unstable property of the ITO/PEDOT : PSS interface in ambient environment. The acidic PEODT : PSS solution can etch ITO during the polymer spin-coating process, and hydrolysis of deposited PEDOT : PSS *via* moisture absorption can also etch ITO.[35] On the contrary, rGO electrodes are physically, chemically and electrically stable in ambient environment, guaranteeing a higher endurance stability of self-rectifying memory devices with rGO electrode.

In summary, a self-rectifying polymer memory device with the configuration of rGO/PEDOT : PSS/carbon dots/MEH-PPV/Al has been designed and fabricated through solution process. The memory effect of the as-fabricated device is attributed to the carrier trapping effect of carbon dots within

polymers and the corresponding rectifying characteristic comes from the bilayer's energy level offset with electrodes. The self-rectifying memory device exhibits a maximum rectification of 10^3 in rectify model and a minimum ON/OFF current ratio of 121 in memory model. Moreover, the devices show high endurance stability of self-rectifying memory effect with rGO electrode compared to that with ITO electrode. Importantly, the solution process fabrication make this device extremely simple. Because of the self-rectifying memory feature, the simple devices have great potential application in cross-bar structure memory for high-density data storage.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

We thank primary financial supports by the National Key R&D Program of China (2017YFB1002900), the National Natural Science Foundation of China (61622402, 61376088, and 51302134), the Natural Science Foundation of Jiangsu (BK20150955), and the Jiangsu Specially-Appointed Professor programme, the Six Talent Plan (2015XCL015).

Notes and references

1 A. Asamitsu, Y. Tomioka, H. Kuwahara and Y. Tokura, *Nature*, 1997, **388**, 50–52.
2 R. Waser and M. Aono, *Nat. Mater.*, 2007, **6**, 833–840.
3 M. J. Lee, Y. Park, D. S. Suh, E. H. Lee, S. Seo, D. C. Kim, R. Jung, B. S. Kang, S. E. Ahn, C. B. Lee, D. H. Seo, Y. K. Cha, I. K. Yoo, J. S. Kim and B. H. Park, *Adv. Mater.*, 2007, **19**, 3919–3923.
4 C. Moreno, C. Munuera, S. Valencia, F. Kronast, X. Obradors and C. Ocal, *Nano Lett.*, 2010, **10**, 3828–3835.
5 J. C. Scott, *Science*, 2004, **304**, 62–63.
6 M. J. Lee, S. Seo, D. C. Kim, S. E. Ahn, D. H. Seo, I. K. Yoo, I. G. Baek, D. S. Kim, I. S. Byun, S. H. Kim, I. R. Hwang, J. S. Kim, S. H. Jeon and B. H. Park, *Adv. Mater.*, 2007, **19**, 73–76.
7 J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart and R. S. Williams, *Nat. Nanotechnol.*, 2008, **3**, 429–433.
8 S. H. Jo, K. H. Kim and W. Lu, *Nano Lett.*, 2009, **9**, 870–874.
9 E. Linn, R. Rosezin, C. Kugeler and R. Waser, *Nat. Mater.*, 2010, **9**, 403–406.
10 D. Tu, M. Liu, L. Shang, X. Liu and C. Xie, *Appl. Phys. Lett.*, 2008, **92**, 123302.
11 G. H. Kim, K. M. Kim, J. Y. Seok, H. J. Lee, D. Y. Cho, J. H. Han and C. S. Hwang, *Nanotechnology*, 2010, **21**, 385202.
12 B. Cho, T. W. Kim, S. Song, Y. Ji, M. Jo, H. Hwang, G. Y. Jung and T. Lee, *Adv. Mater.*, 2010, **22**, 1228–1232.
13 X. Yan, H. Hao, Y. Chen, S. Shi, E. Zhang, J. Lou and B. Liu, *Nanoscale Res. Lett.*, 2014, **9**, 548–553.
14 K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki and Y. Sugiyama, *Appl. Phys. Lett.*, 2008, **93**, 033506.
15 W. Y. Park, G. H. Kim, J. Y. Seok, K. M. Kim, S. J. Song, M. H. Lee and C. S. Hwang, *Nanotechnology*, 2010, **21**, 195201.
16 M. Y. Song, Y. Seo, Y. S. Kim, H. D. Kim, H.-M. An, B. H. Park, Y. M. Sung and T. G. Kim, *Appl. Phys. Express*, 2012, **5**, 091202.
17 S.-L. Li, D. S. Shang, J. Li, J. L. Gang and D. N. Zheng, *J. Appl. Phys.*, 2009, **105**, 033710.
18 Q. Zuo, S. Long, S. Yang, Q. Liu, L. Shao, Q. Wang, S. Zhang, Y. Li, Y. Wang and M. Liu, *IEEE Electron Device Lett.*, 2010, **31**, 344–346.
19 K. P. Biju, X. Liu, E. M. Bourim, I. Kim, S. Jung, M. Siddik, J. Lee and H. Hwang, *J. Phys. D: Appl. Phys.*, 2010, **43**, 495104.
20 J. H. Yoon, S. J. Song, I.-H. Yoo, J. Y. Seok, K. J. Yoon, D. E. Kwon, T. H. Park and C. S. Hwang, *Adv. Funct. Mater.*, 2014, **24**, 5086–5095.
21 J. H. Yoon, K. M. Kim, S. J. Song, J. Y. Seok, K. J. Yoon, D. E. Kwon, T. H. Park, Y. J. Kwon, X. Shao and C. S. Hwang, *Adv. Mater.*, 2015, **27**, 3811–3816.
22 S. Gao, F. Zeng, F. Li, M. Wang, H. Mao, G. Wang, C. Song and F. Pan, *Nanoscale*, 2015, **7**, 6031–6038.
23 S. H. Jo and W. Lu, *Nano Lett.*, 2008, **8**, 392–397.
24 H. Lv, Y. Li, Q. Liu, S. Long, L. Li and M. Liu, *IEEE Electron Device Lett.*, 2013, **34**, 229–231.
25 H.-D. Kim, M. Yun and S. Kim, *J. Alloys Compd.*, 2015, **651**, 340–343.
26 L. S. Roman, M. Berggren and O. Inganäs, *Appl. Phys. Lett.*, 1999, **75**, 3557–3559.
27 J. Robertson, *J. Vac. Sci. Technol., A*, 2013, **31**, 050821.
28 J. Liu, Z. Yin, X. Cao, F. Zhao, A. Lin, L. Xie, Q. Fan, F. Boey, H. Zhang and W. Huang, *ACS Nano*, 2010, **4**, 3987–3992.
29 J. Liu, Z. Zeng, X. Cao, G. Lu, L. H. Wang, Q. L. Fan, W. Huang and H. Zhang, *Small*, 2012, **8**, 3517–3522.
30 J. Liu, Z. Yin, X. Cao, F. Zhao, L. Wang, W. Huang and H. Zhang, *Adv. Mater.*, 2013, **25**, 233–238.
31 S. Pang, H. N. Tsao, X. Feng and K. Müllen, *Adv. Mater.*, 2009, **21**, 3488–3491.
32 C. Guo, K. Wang, E. Zerah-Harush, J. Hamill, B. Wang, Y. Dubi and B. Xu, *Nat. Chem.*, 2016, **8**, 484–490.
33 Y. Dong, J. Shao, C. Chen, H. Li, R. Wang, Y. Chi, X. Lin and G. Chen, *Carbon*, 2012, **50**, 4738–4743.
34 P. C. Ooi, M. M. R. Wee, C. F. Dee, C. C. Yap, M. M. Salleh and B. Y. Majlis, *Thin Solid Films*, 2018, **645**, 45–50.
35 T. L. Truong, D.-O. Kim, Y. Lee, T.-W. Lee, J. J. Park, L. Pu and J.-D. Nam, *Thin Solid Films*, 2008, **516**, 6020–6027.

