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Correction: Lithographically fabricated gold nanowire waveguides for plasmonic routers and logic gates

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Correction for 'Lithographically fabricated gold nanowire waveguides for plasmonic routers and logic gates' by Long Gao *et al.*, *Nanoscale*, 2018, **10**, 11923–11929.

The authors have noticed an error in Fig. 6 in the published paper, in which Fig. 6b and Fig. 5c are identical due to an error that occurred in the production stage of the paper. The correct version of Fig. 6 is shown below, and the caption of the figure remains the same. This error does not affect the conclusions of the paper.

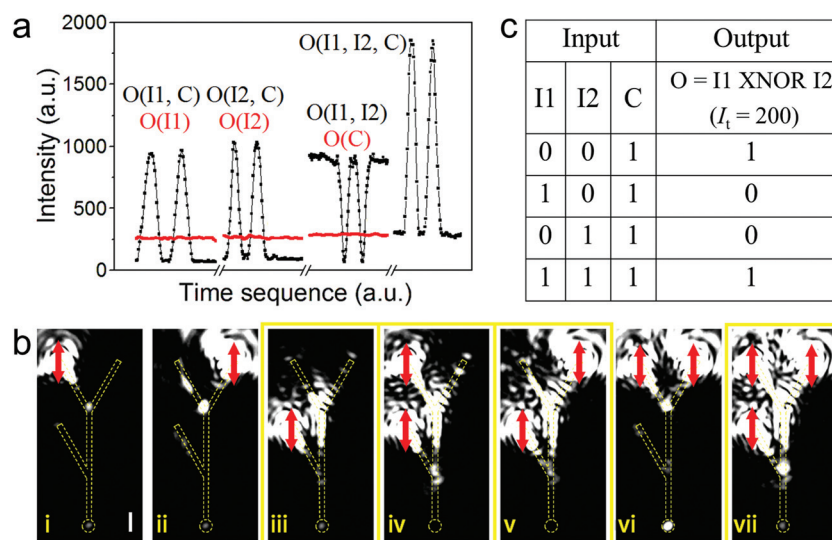


Fig. 6 Interference of SPs in a gold NW network with three inputs for the XNOR gate. (a) Output intensity for single inputs (red) and multiple inputs (black) with the phase difference changing over time. The plateaus on the sides of the oscillating curves correspond to the minimum or maximum output intensity for fixed phases. (b) (i–iii) Scattering images for single inputs. (iv–vii) Scattering images for two or three inputs. The scattering images outlined by yellow boxes show the working states corresponding to the XNOR operations. The red arrows indicate the polarization of incident light. The scale bar is 1 μm . (c) Inputs and outputs of the XNOR logic gate.

The Royal Society of Chemistry apologises for this error and any consequent inconvenience to authors and readers.

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