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Optimized single-layer MoS_2 field-effect transistors by non-covalent functionalisation†

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Field-effect transistors (FETs) with non-covalently functionalised molybdenum disulfide (MoS_2) channels grown by chemical vapour deposition (CVD) on SiO_2 are reported. The dangling-bond-free surface of MoS_2 was functionalised with a perylene bisimide derivative to allow for the deposition of Al_2O_3 dielectric. This allowed the fabrication of top-gated, fully encapsulated MoS_2 FETs. Furthermore, by the definition of vertical contacts on MoS_2, devices, in which the channel area was never exposed to polymers, were fabricated. The MoS_2 FETs showed some of the highest mobilities for transistors fabricated on SiO_2 with Al_2O_3 as the top-gate dielectric reported so far. Thus, gate-stack engineering using innovative chemistry is a promising approach for the fabrication of reliable electronic devices based on 2D materials.

Introduction

Following the advent of graphene,[1] two-dimensional (2D) materials have been extensively examined as promising materials for nanoelectronics.[2–5] Unlike graphene, in which the absent bandgap limits its applications,[6–9] 2D semiconducting transition-metal dichalcogenides (TMDs), such as MoS_2, are considered as promising materials for future nanoelectronic devices.[10–14] To date, several methods have been introduced to obtain TMDs, each with benefits and drawbacks: mechanical exfoliation delivers high-quality flakes[10,15] but suffers from scalability, while liquid-phase exfoliated materials have limited device performance.[16–19] Additionally, exfoliation leads to dispersed layer thicknesses, which give rise to varying properties.[15,20–22] Thermally assisted conversion (TAC) of pre-deposited metals or metal oxides yields a variety of large-scale TMD films with a controllable thickness, however they are typically polycrystalline and defective.[23–25] Chemical vapour deposition (CVD) produces high-quality TMD crystals of predominantly monolayer thickness, however the growth of continuous, large-area films remains a challenge.[26–28] Given the associated advantages, CVD growth is the most suitable method for scalable fabrication of industry-relevant electronic devices.

Besides the challenges in synthesis, one of the major issues in the fabrication of reliable devices with monolayer TMDs is the control over the surface chemistry. Due to their monolayer nature, the properties of 2D materials depend strongly on the environment. Adsorbates lead to doping *via* charge transfer, resulting in significant changes in the electrical properties. This effect is exploited in chemiresistors or ChemFETs for chemical sensing.[29,30] Furthermore, most monolayer TMDs are unstable and degrade under ambient conditions due to oxidation by water and/or oxygen.[31,32] This leads to a deteriorated performance of FETs due to hysteresis and undefined doping. Therefore, it is important to passivate the 2D channels of devices for their stable operation. High-κ materials are considered to be excellent passivation layers and gate insulators. In general, they are suitable for low leakage and low power logic devices due to the high dielectric constant.[33] Furthermore, high-κ materials improve the carrier mobility by reducing Coulomb scattering for nanostructures[34] or increasing the effective gate electric field.[35] Al_2O_3 is one of the most commonly used high-κ materials, often deposited using trimethylaluminum (TMA, $Al(CH_3)_3$) and an oxidation agent, water or ozone, by atomic layer deposition (ALD). However, the basal planes of 2D nanosheets, such as graphene or MoS_2, do not react with TMA due to the lack of dangling bonds or surface hydroxyl groups.[36–39] Thus, the formation of a seeding layer is required to perform ALD on the clean surface of 2D van der Waals crystals. We have shown that when perylene bisimides are deposited from the liquid phase onto graphene,

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they form self-assembled monolayers (SAMs).[40,41] Specifically, –COOH and –OH units of the molecule react with TMA and promote the nucleation.[33,42,43] The same non-covalent functionalisation route was adopted for TMD layers,[44] wherein the perylene bisimide functional layer served as a stable seeding layer for Al_2O_3 deposition *via* ALD.

In this study we fabricated top-gated FETs with functionalised CVD-grown MoS_2. The perylene bisimide functional layer is used as a seeding layer for Al_2O_3 deposition, fabricating fully encapsulated MoS_2 FETs. We compared the devices fabricated by two different process flows. In both cases the electrical integrity of the TMD is maintained. Furthermore, the influence of the polymer residue on the device performance could be quantified.

Methods

MoS_2 growth

MoS_2 samples were grown in a micro-cavity in a two-zone CVD furnace at 700 °C as described previously.[26] The samples were grown directly on SiO_2/Si (300 nm thick SiO_2, highly p-doped Si) substrates with MoO_3 and sulfur as solid precursors.

Device fabrication

Back-gated MoS_2 FETs. The source/drain electrodes on MoS_2 flakes were patterned by electron beam lithography (EBL), with an electron beam resist (PMMA – A4, MicroChem) which was spin-coated onto the sample. EBL was performed using a Zeiss Supra 40 with a Raith EBL kit. After baking at 180 °C and developing with a MIBK : IPA (1 : 3) solution, the metal electrodes (Ti/Au, 5 nm/50 nm) were deposited by sputtering using a Gatan Precision Etching and Coating System (PECS).

Top-gated MoS_2 FETs type 1. Directly after the MoS_2 growth, perylene bisimide dissolved in aqueous buffer solution was deposited on the sample. Source/drain electrodes were defined by EBL as described above. The metal electrodes (Ti/Au, 5 nm/50 nm) were deposited by using an electron beam evaporator (Temescal FC-2000). After lift-off, a 34 nm thick Al_2O_3 layer was then deposited on the MoS_2 channel region which was defined by EBL, using ALD (TP01, ATV Technology) with TMA and H_2O precursors at 80 °C. The Al_2O_3 thickness was measured by atomic force microscopy (AFM) as shown in Fig. S1(a).† Finally, the top-gate metal electrode (Ti/Au, 5 nm/50 nm), patterned by EBL, was sputtered (Gatan Precision Etching and Coating System).

Top-gated MoS_2 FETs type 2. Directly after the MoS_2 growth, perylene bisimide dissolved in aqueous buffer solution was deposited on the MoS_2. Subsequently, a 16 nm thick Al_2O_3 layer was deposited onto the samples by ALD at 80 °C with TMA and H_2O as precursors. The height profile of the first ALD-grown Al_2O_3 layer measured by AFM is shown in Fig. S1(b).† PMMA (A4, MicroChem) was then spin-coated on the Al_2O_3 layer and source/drain electrodes were defined by EBL. After development, the exposed Al_2O_3 layer was removed with 2.38% tetramethylammonium hydroxide (TMAH) solution in H_2O at 55 °C, creating a vertical contact hole (VIA). Then metal electrodes (Ti/Au, 5 nm/50 nm) were deposited by electron beam evaporation, followed by lift-off. In order to prevent the possible leakage of the gate dielectrics during electrical measurements, an additional 24 nm thick Al_2O_3 was deposited onto the gate region. The AFM height profile of the second ALD Al_2O_3 thickness is shown in Fig. S1(c).† In a subsequent step, the top gate electrode was defined by EBL and the gate metal electrode (Ti/Au, 5 nm/50 nm) was sputtered, followed by lift-off.

Raman spectroscopy was performed using LabRam ARAMIS IR2 (HORIBA JOBIN YVON) and a WITec Alpha 300R with a 532 nm laser as the excitation source. The thicknesses of Al_2O_3 and MoS_2 were measured using AFM (MFP-3D, Asylum Research). The topographic images of the MoS_2 surface were obtained by AFM (Park Systems Park XE100). Scanning electron microscopy (SEM) imaging was done using a MIRA3 (TESCAN). Electrical measurements were conducted on a JANIS probe station connected to a Keithley 2612A source meter unit under vacuum (top-gated FETs: ~3.7 Torr, back-gated FETs: ~2.3×10^{-4} Torr) at room temperature. The substrate was connected to the ground during the electrical measurement of the top-gated FETs.

Results

The CVD growth yields randomly distributed, monolayer MoS_2 regions, *e.g.* flakes, which are mostly triangular in shape and extend over several micrometers. In Fig. 1 typical results of CVD-grown MoS_2 on SiO_2 are presented. In Fig. 1(a) a SEM image of the triangular shaped MoS_2 is shown. AFM measurements confirmed the monolayer nature of the triangular regions, as shown in Fig. 1(b) and (c). A Raman spectrum of an as-grown MoS_2 flake is shown in Fig. 1(d), the in-plane (E′) and out-of-plane (A'_1) peaks occur at 383 and 403 cm^{-1}, respectively, which is consistent with monolayered MoS_2. Some bilayer and/or multilayer formation also can take place in the seeding regions of the flakes as shown in the inset of Fig. 2(a) (line region of the optical image).

To reveal the electrical properties of the CVD-grown MoS_2, flakes were brought into contact with EBL-defined electrodes as shown in Fig. S2(a).† Using the substrate as the back gate, a FET with an MoS_2 channel was defined as schematically shown in the inset of Fig. S2(a).† The FET shows on/off ratios on the order of 10^3, and the average field-effect mobility of the device is 0.66 $cm^2\ V^{-1}\ s^{-1}$ for forward sweep and 0.79 $cm^2\ V^{-1}\ s^{-1}$ for reverse sweep. These relatively low mobility values can be attributed to the scattering of carriers at the surface and the SiO_2 substrate.[45] In order to improve the performance, FETs in which the MoS_2 channel is encapsulated and the channel has a top-gate electrode, separated by a high-κ oxide for effective modulation, can be fabricated. The gate dielectric deposition is ideally realised in a non-destructive and scalable manner by ALD. However, generally ALD on clean 2D van der Waals materials is challenging, due to the

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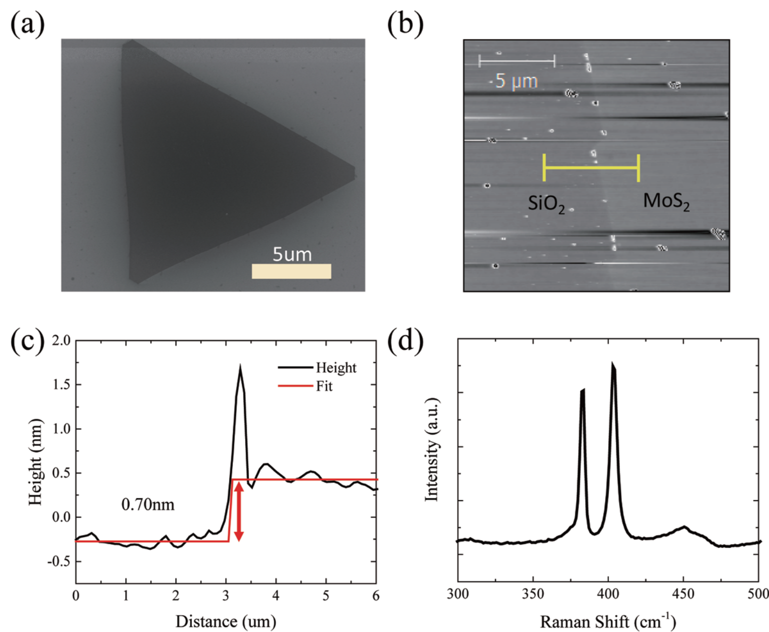

Fig. 1 (a) SEM image of CVD-grown MoS_2. (b) AFM topography of CVD-grown MoS_2. (c) Average line profile along the marked line in (b). The step height between the flake and substrate is ∼0.7 nm, confirming the monolayer nature of the triangular regions. (d) Raman spectrum of monolayer CVD-grown MoS_2.

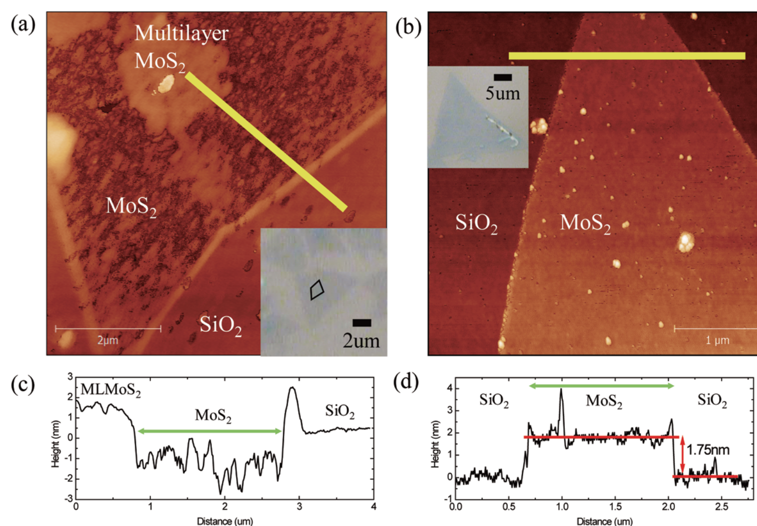

Fig. 2 (a) AFM topography of pristine MoS_2 after Al_2O_3 deposition by ALD. A very rough surface due to Al_2O_3 islands can be seen on the MoS_2 regions. Inset: Optical image of the investigated region. (b) AFM topography of MoS_2 functionalized with perylene bisimide after Al_2O_3 deposition by ALD. Inset: Optical image of the investigated region. (c) Line profile along the marked line in (a). The MoS_2 lies on average lower than that in the SiO_2 substrate. (d) Line profile along the marked line in (b). The MoS_2 lies higher than that in the SiO_2 substrate.

absence of seeding sites such as hydroxyl or carbonyl oxides.[39,46–48]

AFM measurements were carried out to investigate the Al_2O_3 deposition on MoS_2. As also shown in Fig. 2 the triangular MoS_2 flakes consist of monolayers. There is some double and multilayer formation in the seeding region at the centre of the grain as shown in the inset of Fig. 2(a) (line region). Fig. 2(a) shows an AFM topography image of an ALD-Al_2O_3 layer deposited on a MoS_2 flake with 45 cycles of TMA/H_2O at 80 °C. Fig. 2(c) shows the line profile of the yellow line in Fig. 2(a). The step height between the monolayer and substrate is approximately 0.34 nm. The MoS_2 lies on average lower than the SiO_2 substrate, and the monolayer surface is very rough. This is attributed to the inhomogeneous and imperfect deposition of Al_2O_3 on the monolayer. Evidently, on the monolayer MoS_2 some Al_2O_3 island growth has taken place, but no con-

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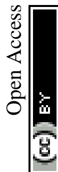

tinuous, complete coverage is reached. The step height between the multilayer and substrate is approximately 1.3 nm, and this is close to the thickness of bilayer MoS_2. This indicates that in the multilayer region Al_2O_3 growth took place. Also, Al_2O_3 deposition can be seen at the edges of the monolayer MoS_2 flakes resulting in a high step at the edge of the MoS_2 flake. This is attributed to a higher abundance of reactive sites such as dangling bonds and defects at the edges of the MoS_2 layers acting as anchor sites for the deposition of Al_2O_3.[44] Fig. 2(b) shows an AFM topography image of an ALD-Al_2O_3 layer on a perylene bisimide-covered MoS_2 flake with 45 cycles of TMA/H_2O at 80 °C. In contrast to Fig. 2(a), the Al_2O_3–MoS_2 surface in Fig. 2(b) is uniform and lies higher than the SiO_2 substrate. Thus, the perylene bisimide layer acts as a seed for ALD growth, resulting in a homogenous and continuous Al_2O_3 layer. Fig. 2(d) shows the line profiles of Fig. 2(b) from the MoS_2 flake to the substrate. The step height between the monolayer and substrate is approximately 1.75 nm, and this exceeds the monolayer thickness. The additional thickness is attributed to the perylene bisimide layer. Thus, the perylene bisimide functionalisation allows the ALD of dielectrics on clean dangling-bond-free TMD surfaces.

Having optimized the dielectric deposition, we investigated the viability of our non-covalent functionalisation to optimize the gate-stack formation of 2D material FETs. The process flow to yield fully encapsulated top-gated MoS_2 FETs (device type 1) is shown in the schematic in Fig. 3(a). It follows the standard device fabrication processes with E-Beam resist (PMMA) deposition directly onto the whole substrate; however in our case the PMMA was deposited after the deposition of perylene bisimide (Fig. 3(b)). Source/drain electrodes were patterned by EBL and deposited by evaporation. After lift-off, the Al_2O_3 gate dielectric was deposited on the entire MoS_2 channel region defined by EBL. This was followed by the deposition of the top gate electrode, after another lithographic step. An optical image of one device is shown in Fig. 3(c). Raman spectroscopy was used to confirm the presence of the MoS_2 monolayer and perylene SAM after the completion of the gate stack. Fig. 3(d) shows the peaks at positions at ~384 cm^{-1} and 401 cm^{-1} for the completed device, corresponding to the E′ and A'$_1$ modes of MoS_2, respectively. Furthermore, the spectra exhibit several peaks in the region of 1300 cm^{-1} to 1600 cm^{-1} typical of perylene bisimide. This underlines the remarkable stability of the perylene SAM, and it withstands the polymer removal with acetone and the ALD process.

Fig. 4(a) shows the I_{DS}–V_{DS} output characteristics at various top-gate voltages (V_{TG}) of device type 1. The SiO_2 substrate of the device was grounded during all measurements, reducing the possible capacitive coupling between top- and back-side dielectrics.[49] Linear behavior is observed at each V_{TG}, which indicates that the integration route yields good contacts and that the perylene bisimide layer does not significantly affect the contact properties between MoS_2 and the electrodes. Fig. 4(b) shows the typical I_{DS}–V_{GS} transfer characteristics of device type 1. This exhibits a counter clockwise hysteresis. The reverse sweep of the top-gate voltage, V_{TG}, exhibits a higher conductivity compared with the forward sweep of V_{TG}. The counter clockwise hysteresis can be attributed to the positive

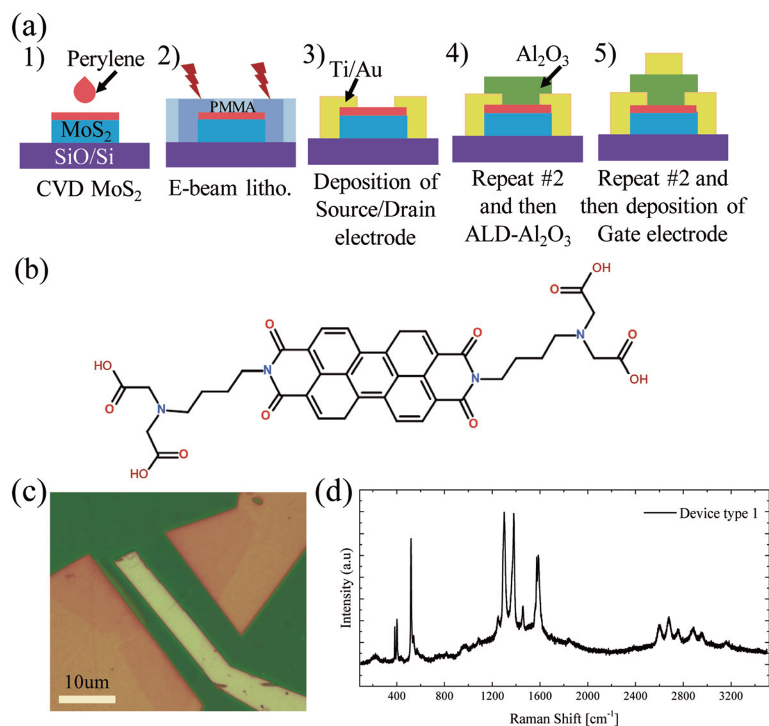

Fig. 3 Top-gated MoS_2 FET type 1: (a) Schematic of the process flow. (b) Chemical structure of the perylene bisimide derivative. (c) Top view optical image of the fully fabricated device. (d) Raman spectrum of the channel area of a fully fabricated device.

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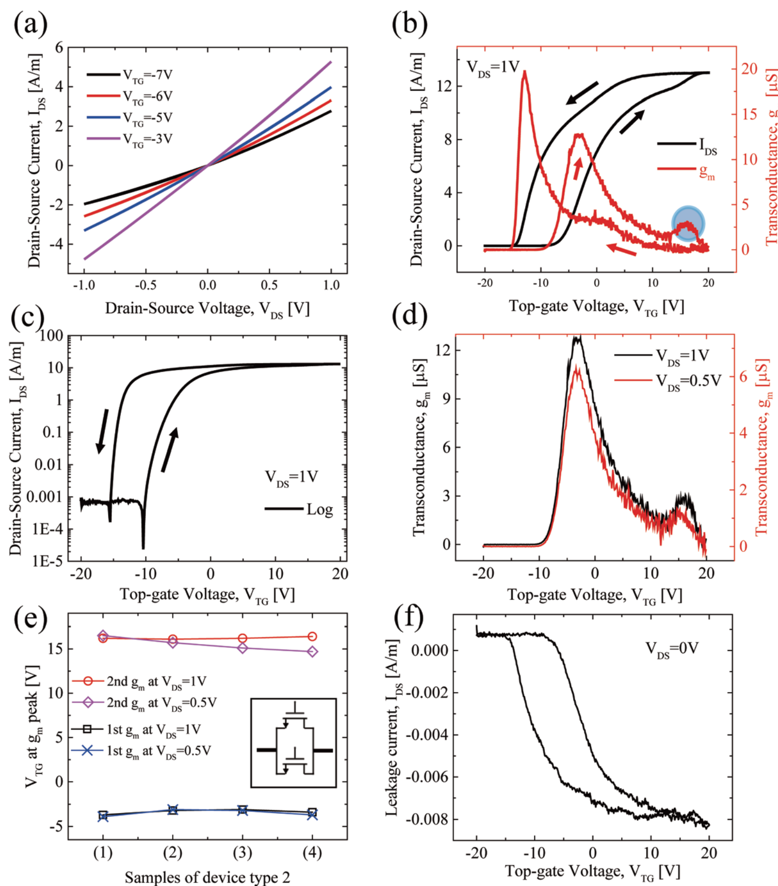

Fig. 4 Electrical characterisation of device type 1: (a) Output characteristics. (b) Transfer characteristics (black line) and transconductance (red line) curves for various top-gate voltages at V_{DS} = 1 V. The blue circle highlights the second transconductance peak. (c) Logarithmic plot of transfer characteristics. (d) Transconductance curves at V_{DS} = 0.5 V (red line) and 1 V (black line). (e) Top-gate voltages for the first and second transconductance peaks of type 1 devices at V_{DS} = 0.5 V and 1 V. Inset: equivalent circuit model with two transistors connected in parallel. (f) Plot of leakage current *versus* top-gate voltage.

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mobile charges in Al_2O_3.[50,51] In the forward V_{TG} sweep, positive mobile charges in Al_2O_3 move to the Al_2O_3/(perylene bisimide)/MoS_2 interface. In the reverse V_{TG} sweep, the positive mobile charges located near the MoS_2 surface induce an additional electrical field, and this leads to a lower threshold voltage (V_{TH}) and increases the current. Additionally, we compared the transfer characteristics between two back-gated MoS_2 FETs, with and without a perylene bisimide layer on the MoS_2 channels. As shown in Fig. S2(c) and (f) of the ESI,† both devices show a similar hysteresis trend, indicating that the perylene bisimide layer does not play an important role in the observed hysteresis. Sub-threshold swing is 283 mV per decade for the forward sweep and 214 mV per decade for the reverse sweep. The field-effect mobility (μ_{FE}) is calculated by the transfer characteristic using the following equation:

$$\mu_{FE} = \frac{Lg_m}{WC_{Al_2O_3}V_{DS}} \quad (1)$$

where $C_{Al_2O_3}$ denotes gate dielectric capacitance, g_m denotes transconductance, V_{DS} denotes drain–source voltage, L denotes channel length, and W denotes channel width. The channel shape does not often correspond to a rectangle, and thus the channel width is obtained by dividing the total channel area by the channel length. The μ_{FE} of the device is 21.4 $cm^2 V^{-1} s^{-1}$ for the forward sweep and 33.4 $cm^2 V^{-1} s^{-1}$ for the reverse sweep. The red line in Fig. 4(b) indicates the g_m of the device. The slope of drain/source current significantly increases until the g_m reaches a peak, and then decreases when V_{TG} increases. However, the device exhibits an intriguing second g_m peak for the forward V_{TG} sweep (blue-circled region) which is consistent with a small hump in the transfer characteristics at the same V_{TG}. Such a second g_m peak was also observed at various V_{DS} (Fig. 4(d)) in four out of five samples. Interestingly, as shown in Fig. 4(e), the second g_m peak appears at similar V_{TG} (~16 V) in all four samples regardless of V_{DS}, indicating that there is a common reason for the second g_m peak with reproducibility. Similar signatures in the transfer characteristics were observed in SOI MOSFETs,[52–56] polysilicon thin film transistors,[57] and gate injection GaN-based transistors.[58] Even in the case of the previous studies of SOI MOSFETs, which are more optimized than the MoS_2 FETs studied here, the origin of additional

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transport carriers varied depending on the device structure and materials. Thus, the origin of the second g_m peak cannot be exactly determined at this stage. However, as shown in Fig. 4(b), a slight increase in current was observed at V_{TG} of the second g_m peak. As discussed in previous studies,[52–58] the injection of additional transport carriers could be considered as one of the reasons for the second g_m peak. In the case of device type 1, the leakage current (see Fig. 4(f)), obtained by measuring the I_{DS} at V_{DS} = 0 V under a V_{TG} sweep, can be ruled out as a source of the additional carriers, since it is too low to affect the transfer characteristics. The devices can be expressed using an equivalent circuit model, composed of a main transistor connected to a parasitic transistor in parallel, as shown in the inset of Fig. 4(e). In the equivalent circuit model, the threshold voltage of the main transistor differs from that of the parasitic transistor. The second g_m peak value is small compared to the first g_m peak, as shown in Fig. 4(b). This is because the current generated after the parasitic transistor turns on is low.

A second more advanced process flow avoiding any contact of the channel region with the polymer resist was developed. As shown in Fig. 5(a), for device type 2 we deposited the Al_2O_3 layer on the whole substrate directly after perylene bisimide functionalisation. The source/drain electrodes were patterned by EBL, effectively creating contact holes by wet etching of the Al_2O_3 layer with an etch stop on the MoS_2. This realisation of vertical interconnects (VIAs) with metal evaporation to contact 2D materials is an important step in their successful integration. Importantly, this process flow has an advantage that the MoS_2 channel is never in contact with the polymer resist. The presence of perylene between the Al_2O_3 and the MoS_2 was confirmed by using Raman spectroscopy. The spectra were obtained after device fabrication was completed. Like device type 1, the typical signatures for MoS_2 at ∼385 cm^{-1} and 405 cm^{-1} and perylene at 1300 cm^{-1} to 1600 cm^{-1} are observed as shown in Fig. 5(c).

In Fig. 6(a), the output characteristics of device type 2 are shown. They exhibit a linear behavior like device type 1, indicating that the contacts between the monolayer MoS_2 and electrodes, which were defined by VIA etching and filling, were well established. This is an important achievement for the integration of 2D materials. Fig. 6(b) shows the transfer characteristics and transconductance of the device. A counter clockwise hysteresis appears, similar to the device type 1. Subthreshold swing is 255 mV per decade for the forward sweep and 224 mV per decade for the reverse sweep. The μ_{FE} of

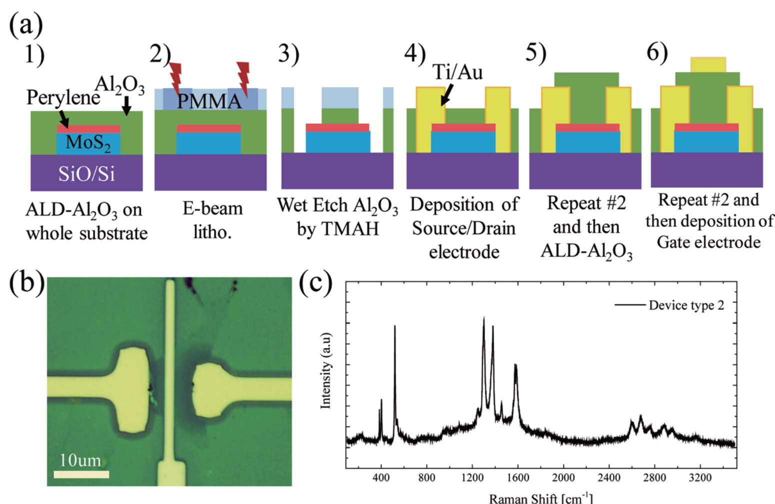

Fig. 5 Top-gated MoS_2 FET type 2: (a) Schematic of the process flow. (b) Top view optical image of the fully fabricated device. (c) Raman spectrum of the channel area of a fully fabricated device.

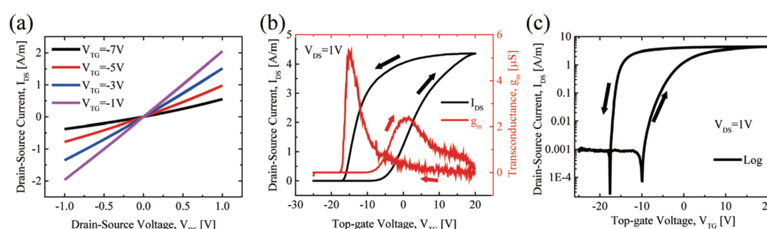

Fig. 6 Electrical characterisation of device type 2: (a) output characteristics. (b) Transfer characteristics (black line) and transconductance (red line) for various top gate voltages at V_{DS} = 1 V. (c) Logarithmic plot of transfer characteristics.

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device was extracted to be 22 $cm^2 V^{-1} s^{-1}$ for the forward sweep and 48.7 $cm^2 V^{-1} s^{-1}$ for the reverse sweep. Unlike device type 1, the second g_m peak was not observed in device type 2, as shown with a red line in Fig. 6(b).

The main difference between device type 1 and 2 is that in the latter case the functionalized MoS_2 channel was not in contact with the resist during the fabrication. It is well known that resist residues can remain on the film surface after development and lift-off processes. To investigate this, the MoS_2 surface was characterized by AFM during fabrication. Fig. 7(a) shows the functionalized MoS_2 surface after the development of the polymer resists during the fabrication of device type 1 (step 2 in Fig. 3(a)). A relatively rough surface with a root-mean-square (RMS) roughness of 0.54 nm was observed. This roughness is likely due to polymer residues which remain in the channel area. In contrast, the functionalized MoS_2 surface after wet-etching of the contact area (step 3 in Fig. 5(a)) of the device type 2 appears to be relatively flat (RMS roughness = 0.30 nm). Both the RMS and average values of the surface roughness of device type 1 clearly exceed those of device type 2. Thus one can deduce that while type 1 devices have polymer residues on the surface of the channel, type 2 devices have a relatively clean interface to the top gate dielectric. Thus we can tentatively attribute the second g_m peak to the polymer residue in the channel area in device type 1, however additional experiments are required to analyze the exact mechanisms that cause the second g_m peak.

To investigate the influence of resist residues on the device performance, five samples were fabricated and compared for each device type. The threshold voltage, mobilities and contact resistances of the devices are summarized in Fig. 7(c), (d) and (e). Device type 1 (34 nm) and 2 (40 nm) have different Al_2O_3 thicknesses. Even when applying the same gate voltage, the gate electric field is different depending on the dielectric thickness. While considering the gate electric field, the threshold voltage was multiplied by $C_{Al_2O_3}$. As shown in Fig. 7(c), the hysteresis ($V_{TH,reverse}$–$V_{TH,forward}$) of device type 2 (0.0235 V F m^{-1}) increased by 26% compared to device type 1 (0.0187 V F m^{-1}). During the second deposition of Al_2O_3 of device type 2, interface states would form between the first and second ALD-Al_2O_3

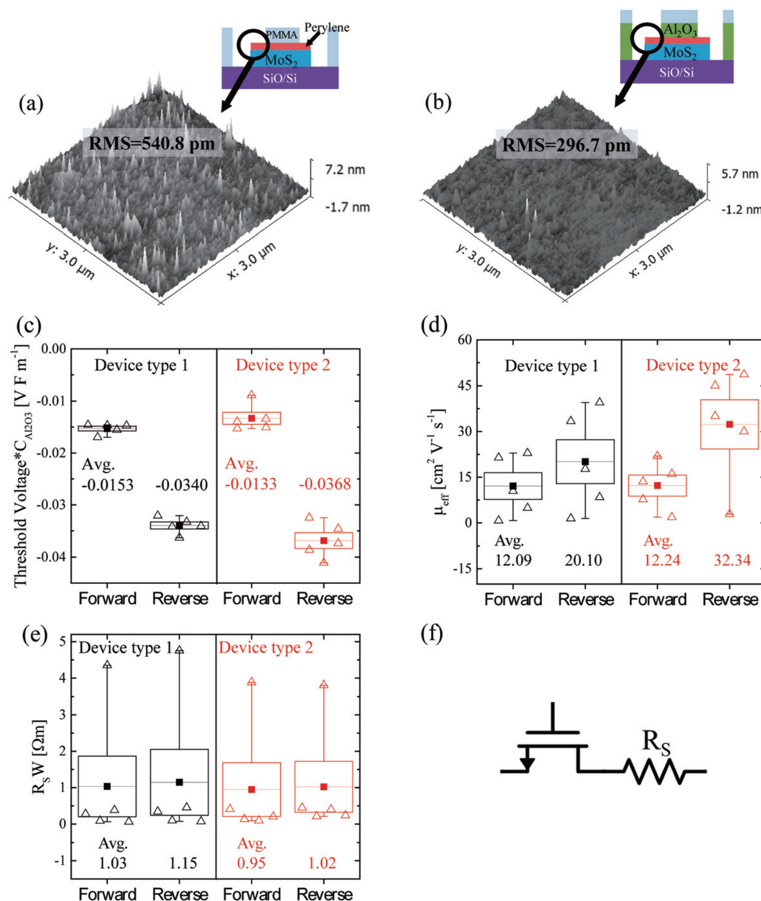

Fig. 7 AFM images of the device type 1 (a) and device type 2 (b) prior to the deposition of the source–drain electrode. (c) Threshold voltage multiplied by $C_{Al_2O_3}$, (d) field-effect mobilities and (e) contact resistance multiplied by the channel width. Distributions of five samples of device type 1 (black) and device type 2 (red) for the V_{TG} sweep directions. Open triangles denote the data for each sample. Filled squares denote the average of five samples. Boxes correspond to the standard error of samples. (f) Equivalent circuit with a serial resistor connected to the transistor. Contact resistance is extracted by using this model.

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layers and the overall quality of the Al_2O_3 of device type 2 would get worse, leading to large hysteresis compared to device type 1. As shown in Fig. 7(d), the average μ_{FE} of device type 1 is lower than that of device type 2. In particular, the average μ_{FE} of the device type 2 (32.3 cm^2 V^{-1} s^{-1}) for the reverse sweep increased by 61% compared to device type 1 (20.1 cm^2 V^{-1} s^{-1}). This can be tentatively assigned to the increased surface roughness and remote charge scattering. As shown in Fig. 7(a), the functionalized MoS_2 surface of device type 1 has resist residues in the channel area, unlike device type 2. Even though the resist residues may not directly adhere to MoS_2 due to the perylene SAM, it can increase the surface roughness and act like a fixed charge inside the gate stack. This latter disturbance can cause scattering by remote surface scattering.[59,60] Further studies are needed to understand why the μ_{FE} of both device types is more pronounced in the reverse sweep than in the forward sweep in Fig. 7(d). The effect of resist residues on the contact resistance of the device was also investigated. As shown in Fig. 7(e), in the high V_{TG} region in Fig. 4(b) and Fig. 6(b), the current is saturated due to the influence of contact resistance (R_s). R_s is extracted by using an equivalent circuit model with a resistor serially connected to the transistor as shown in Fig. 7(f). R_s is obtained by using the graphical method[61] and the following equation:

$$I_{DS} = \mu_{FE} C_{ox} \frac{W}{L} \left[(V_{TG} - V_{TH})(V_{DS} - I_{DS}R_s) - \frac{1}{2}(V_{DS} - I_{DS}R_s)^2 \right] \quad (2)$$

At V_{DS} = 1 V, R_s along each sweep direction was calculated by using the transfer characteristics. Different channel widths (W) were considered for each device, and the width was multiplied by R_s. The distribution of the R_sW of device type 1 and 2 is shown in Fig. 7(e). The average R_sW of device type 2 (0.95 Ωm) for forward sweep reduced by 8% compared to device type 1 (1.03 Ωm), and the average R_sW of device type 2 (1.02 Ωm) for reverse sweep reduced by 11% compared to device type 1 (1.15 Ωm). This strongly suggests that the absence of polymer residues in the source and drain contact regions reduces the contact resistance, but the effect of polymer residues on mobility exceeds that of the contact resistance. In Table 1 the best mobilities for various top-gated FETs with CVD-grown MoS_2 channels are listed. Compared to literature values our best device type 2 exhibits the second highest mobility reported so far. Thus the process flows with perylene bisimide functionalisation can be suggested as a viable route for MoS_2 integration, leading to reliable dielectric deposition with reproducible results and high mobilities.

Table 1 Summary of reported effective mobilities for the top-gated CVD MoS_2 FETs

Dielectric	Substrate	Atmosphere	μ_{FE} [cm^2 V^{-1} s^{-1}]	Ref.
Al_2O_3	SiO_2	Air	~2	62
AlN/Al_2O_3	SiO_2	Air	3.3	63
HfO_2	SiO_2	Air	11	64
Al_2O_3	Si_3N_4	~10^{-6} Torr	24	65
Al_2O_3	SiO_2	3.7 Torr	~33.4	Device type 1
Al_2O_3	SiO_2	3.7 Torr	~48.7	Device type 2
SiO_2/HfO_2	SiO_2	—	42.3	66
HfO_x	SiO_2	Air	55	67

Conclusion

In this study, top-gated FETs with CVD-grown MoS_2 were fabricated. A non-covalent perylene bisimide functionalization was used to facilitate ALD of Al_2O_3 as a dielectric and passivation layer. Perylene bisimide was simply deposited on MoS_2 by drop-casting at room temperature. Furthermore, we were able to define vertical contacts to the MoS_2 channels, yielding fully-encapsulated MoS_2 FETs. Perylene bisimide was non-destructively attached to MoS_2 and led to improved device performance as revealed by surface characterization and electrical measurements. The field-effect mobility for the MoS_2 FETs was found to be 48.7 cm^2 V^{-1} s^{-1}, which is the second highest among top-gated CVD MoS_2 FETs on SiO_2 substrates, and the highest with Al_2O_3 as the top-gate dielectric reported so far. Thus our work suggests that non-covalent functionalisation is a viable strategy to fabricate devices with monolayer 2D materials. Additionally, we investigated the effect of resist residues on the field-effect mobility and contact resistance. This study represents a significant step towards the fabrication of reproducible TMD-based devices, with interface engineering for passivation and dielectric deposition and contact formation as well as better understanding of the effects of polymer residues.

Conflicts of interest

There are no conflicts to declare.

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