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Charge transport mechanism in copper phthalocyanine thin films with and without traps

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We investigate the charge transport mechanism in copper phthalocyanine thin films with and without traps. Previously, charge transport in polycrystalline thin films has been widely described by the multiple trapping and release (MTR) model, without emphasizing the origin of the traps. In this work, polycrystalline organic thin films with and without traps have been grown by engineering different growth conditions. We find that the density of interface states at the grain boundaries can decide the mechanism of charge transport in organic thin films and completely different charge transport mechanisms can be observed in thin films with and without traps.

Introduction

The performance of organic devices based on amorphous[1,2] and polycrystalline[3,4] thin films depends on the efficiency of charge transport within thin films. In order to improve the performance of these devices, it is necessary to understand the mechanism of charge carrier transport in organic thin films. Copper phthalocyanine (CuPc) has been proved to be interesting and technologically important for applications in organic field effect transistors (OFETs),[5] organic light emitting diodes (OLEDs)[6] and organic solar cells (OSCs).[7] All of these devices are generally based on polycrystalline thin films and cannot be fabricated on single crystals due to poor device integration, cross-talk between devices and low mechanical flexibility.[5] Grain boundaries in polycrystalline organic thin films exhibit a large number of barriers and hence limit the charge carrier transport in organic thin film based devices due to trapping and detrapping of charge carriers. It has already been shown[5,8] that grain boundaries in organic thin films play an important role in deciding the performance of organic devices and charge transport in these devices can be significantly improved by engineering the growth parameters so that thin films with smaller numbers of grain boundaries can be obtained. However, there appears to be little investigation on how mechanism of charge transport in polycrystalline organic thin films gets affected when (i) density of grain boundaries is varied (ii) shape of the grains is varied and (iii) interface traps at the interface of grain boundaries are varied. Though, several models based on either analytical or simulation have been developed to investigate the charge transport mechanism in organic thin film,[9,10] two majorly discussed models to explain the transport mechanism in polycrystalline organic thin films are: multiple trapping and release (MTR) model[11–13] and percolation model (PM).[14]

PM based on variable range hopping within the energetic states in the Gaussian density of states (GDOS) of highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) (schematically shown in the left panel in Fig. 1) usually accounts for the carrier transport in amorphous films. Organic polymer thin films which are otherwise amorphous, consist of low density of trap states.[15] However, the carrier transport in polycrystalline thin films is usually described by the ubiquitous model, known as MTR.

According to this model,[16,17] charge transport is controlled by traps which are energetically located between HOMO and LUMO, as schematically shown in the right panel of Fig. 1. Most of the charge carriers reside at traps and temporarily get released to HOMO or LUMO, depending upon the position of the trap level and temperature. Surprisingly, the most important aspect of this model *i.e.* trap is always casually treated without emphasizing where the trap is or what is the origin of the trap in polycrystalline thin films.

Predominantly, there are two sources of traps in organic thin films: chemical impurities and interface states at grain

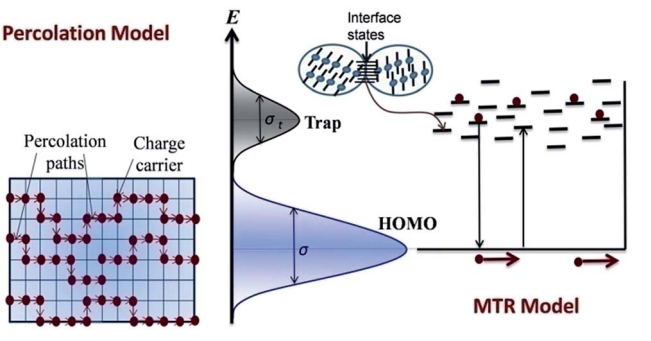

Fig. 1 Schematic representation of charge transport in a p-type organic semiconductor, according to the percolation model based on variable-range-hopping (left panel) and multiple trapping and release model (right panel).

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boundaries.[18–20] The chemical impurities can be reduced by repeated sublimation, but it is difficult to get rid of traps at grain boundaries in polycrystalline thin films. Although, there are several studies[12,21] proposing MTR model to explain charge transport in polycrystalline organic thin films, but it is not clear at all how MTR model can be applied when the density of traps reduced substantially. In view of inapplicability of MTR model, we have explored whether percolation based model could be used in case of polycrystalline thin films.

In this work, we have undertaken detailed investigation on charge transport mechanism in copper phthalocyanine (CuPc) thin films with and without traps by using a combination of two and three terminal devices so that charge transport can be studied along perpendicular and parallel to the film surface. We show that MTR model can explain the charge transport in the polycrystalline organic thin films having intrinsic traps at the grain boundary interfaces. However, it fails to explain the charge transport in polycrystalline thin films having nano-wire like structures with less grain boundaries in which there is either no or negligible quantity of traps. Surprisingly, the PM model explains the charge transport in these films which has more propensity towards crystallinity rather than being amorphous. Charge transport mechanisms in two terminal devices based on thin films with and without traps have also been found completely different.

Experimental details

CuPc, a co-planar organic molecule, has been chosen for this study for two reasons, (i) its exceptional thermal and chemical stability[5] and (ii) its ability to grow with different surface morphologies, required to have thin films with and without intrinsic traps. It seems impossible to attain the desired morphology with linear molecule, such as pentacene or any other acenes. High purity (>99.999%), triple sublimed CuPc, procured from Sigma Aldrich Chemical Co. USA has been used for this study to avoid any traps induced due to chemical impurities. For two terminal devices, 200 nm single layer of CuPc was sandwiched between ITO and Au or Al and Au. Thin films were deposited in oil free evaporation system at a base pressure of 5×10^{-6} mbar. For three terminal organic field effect transistors (OFETs), the heavily doped Si wafers with 300 nm SiO_2 layer were used as substrate. 100 nm thick CuPc films were deposited on the substrate with a deposition rate of 0.1 Å s^{-1} and at different substrate temperatures (T_G). Finally, Au was deposited on the organic layer to form the source and drain contacts. The devices had an identical channel width of 3 mm and channel lengths of 20 μm.

The grain boundaries in polycrystalline thin films are difficult to characterize, as the grains are too small to allow for measurements across individual grain boundaries. In case of poly-Si TFTs, several methods based on change in capacitance due to trapping and detrapping of charge carriers have been employed to characterize traps due to grain boundaries.[21–23] Unfortunately, none of these methods can be applied in polycrystalline organic thin films for their high resistivity and low carrier mobility. In view of these problems, techniques based on steady state or quasi-static measurements are desirable for the characterizations of defects in organic devices.[24] The electrical characterizations of two terminal devices and OFETs were carried out in rough vacuum (10^{-2} mbar) and using Keithley 485 picoammeter and Keithley 228A and Agilent E3643A voltage sources. In case of organic semiconductors, separation of bulk conduction known as space charge limited conduction (SCLC), which dominates when there is either no or small barrier at metal/organic interface from contact limited conduction known as injection limited current (IJL) which dominates when there exists a barrier at metal/organic interface is extremely important. We have considered two sandwiched devices, based on CuPc (ITO/CuPc/Au and Al/CuPc/Au). CuPc is a hole transport material with HOMO and LUMO at 4.8 eV and 3.0 eV, respectively.[25] The work functions of Al, ITO and Au are 4.2 eV, 4.8 eV and 5.2 eV, respectively. There would be either no or very small barrier for holes at Au/CuPc and ITO/CuPc interfaces, but a barrier of 0.6 eV exists at Al/CuPc interfaces.[25,26]

Organic thin films with and without traps

Organic materials were repeatedly sublimed to reduce impurities related traps as much as possible. But, to reduce structural disorder induced traps, it is required to engineer the growth parameters such as substrate temperature and evaporation rate, to have a certain morphology which results thin films with and without traps.[27] Traps due to structural disorder can be reduced substantially by growing organic thin films at low evaporation rate (F_G).[5] At low F_G, incoming molecules have enough time to obtain a favorable orientation resulting ordered growth with minimum structural disorders. Fig. 2 shows the AFM images of CuPc thin films grown at different substrate temperatures (T_G) (30 °C to 120 °C) with a fixed evaporation rate of 0.1 Å s^{-1} on SiO_2 surfaces. The grain size and shape vary gradually from isotropic at low T_G (30 °C) to anisotropic morphology at higher T_G. The CuPc films deposited at substrate temperature of 30 °C show nucleation growth having roughly uniformly distributed grains. Thin films deposited at 60 °C exhibit elongated grains with larger dimensions which convert into rod-like lamellae at 120 °C. This is attributed to the fact that at relatively low substrate temperature, the kinetic energy of the molecules is low and molecules are unable to migrate to meet the other existing islands and get adsorbed at random sites resulting new nucleation centers. Thus nucleation rate dominates the lateral growth resulting into polycrystalline grainy structure with almost equal sized grains (40–60 nm) and a large number of grain boundaries. These grain boundaries act as traps for the charge carriers and hinder the charge transport between source and drain in OFET.[5] At relatively high T_G, diffusion of molecules on the surface increases leading to the coalescence of already existing grains and clusters.

Hence as T_G increases, lateral growth starts dominating the nucleation growth, resulting unidirectional attachment of the molecules at higher T_G. This preferential direction of growth is due to π–π interactions along the adjacent molecules and

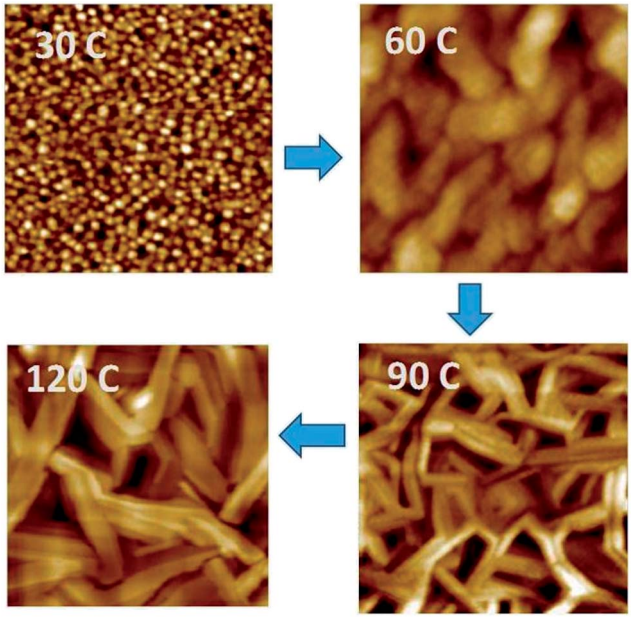

Fig. 2 AFM topographic (1 μm × 1 μm) images of CuPc thin films, deposited on SiO_2 at substrate temperatures (T_G) varied from 30 °C to 120 °C with a fixed evaporation rate of 0.1 Å s^{-1}.

results into greater sticking coefficient along this direction, under growth conditions of higher T_G and low F_G.

Hence desired morphology of thin films with and without grain boundaries can be obtained by varying the growth parameters (T_G and F_G) appropriately.

Arrangement of molecules in CuPc thin films

Fig. 3(a) shows the X-ray diffraction (XRD) pattern of CuPc thin film grown at 120 °C. The XRD pattern exhibits a strong peak at $2\theta \sim 6.8°$ which is due to (100) plane confirming α-phase triclinic structure.[28] From XRD, it can be concluded that *bc*-plane lies parallel to the substrate and is relevant for charge transport in OFET. Fig. 3(b) shows the arrangement of CuPc molecules in OFET geometry. In this plane, CuPc molecules adopt stacking along *b*-axis. Fig. 3(c) shows the arrangement of CuPc molecules perpendicular to the substrate *i.e.* along *a*-axis which is relevant for charge transport along perpendicular to *bc*-plane *i.e.* in two terminal sandwiched devices. The XRD pattern of CuPc thin films grown at 30 °C is identical, except the intensity of peak is less than that in thin film grown at 120 °C.

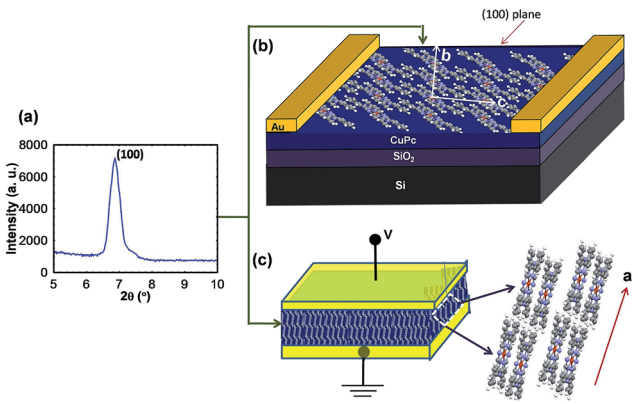

Fig. 3 (a) XRD of CuPc thin film grown at 120 °C on SiO_2 substrate. Schematic representation of arrangement of CuPc molecules (b) in a plane parallel to the substrate and (c) perpendicular to the substrate. These are relevant planes for charge transport in three and two terminal devices, respectively.

Transport along *a*-axis

J–V and *C–T* characteristics of two terminal devices with and without traps

Fig. 4 shows the current–voltage (*J–V*) characteristics of ITO/CuPc/Au based two terminal devices in which CuPc thin films were grown at $T_G = 30$ °C and 120 °C. In Fig. 4(a), initially, the current increases linearly (ohmic region) due to the thermally generated charge carriers. As the bias increases, current increases more than fourth power of voltage due to trap charge limited conduction (TCLC), following $J \propto V^{l+1}$ ($l > 1$).[29,30] This has been attributed to the exponential or Gaussian distribution of traps[30,31] which is further corroborated by a clear step at 230 K in capacitance temperature (*C–T*) characteristics obtained from thermally stimulated capacitance (TSCAP)[32] measurements, shown in the upper inset of Fig. 4(a). This step is observed due to combined effect of two processes; one generation of carriers with temperature and other loss of carriers due to trapping. The midpoint of the step has been used to determine the trap level (E_t), given by,[32] $E_t = k_B T_m \ln(\alpha T_m^4/\beta)$, where T_m is the midpoint of the step, k_B is the Boltzmann's constant, $\alpha \sim 1$ K^{-3} s^{-1} and β is the heating rate which is kept constant at 5 K min^{-1} during *C–T* measurement. A step at 230 K corresponds to the trap level at 0.5 ± 0.05 eV which confirms the existence of deep traps in CuPc thin films grown at low T_G. In TCLC regime, *J–V* characteristics of two terminal devices, in the Arrhenius form can be expressed as[31,33]

$$J = \left(\frac{\mu N_V q V}{d}\right) f(l) \exp\left[\frac{-E_a}{k_B T}\right] \quad (1)$$

where $f(l) = 2^{-l}\left(\frac{2l+1}{l+1}\right)^{l+1}\left(\frac{l}{l+1}\right)^{l}$ and E_a is the activation energy, given by

$$E_a = k_B T_c \ln \frac{q N_{tot} d^2}{2\varepsilon V} \quad (2)$$

where q is the elementary charge, N_V is the effective density of the states (DOS) in the HOMO of CuPc, μ is the mobility of charge carriers, N_{tot} is the density of trap states, d is the thickness of the thin film and ε is the dielectric constant of organic molecular semiconductor. $f(l) \approx 0.5$ when $l > 2$. Further from Fig. 4(a), it can be seen that the current is temperature independent at a particular voltage V_c, where E_a must be zero. So one gets from eqn (2),

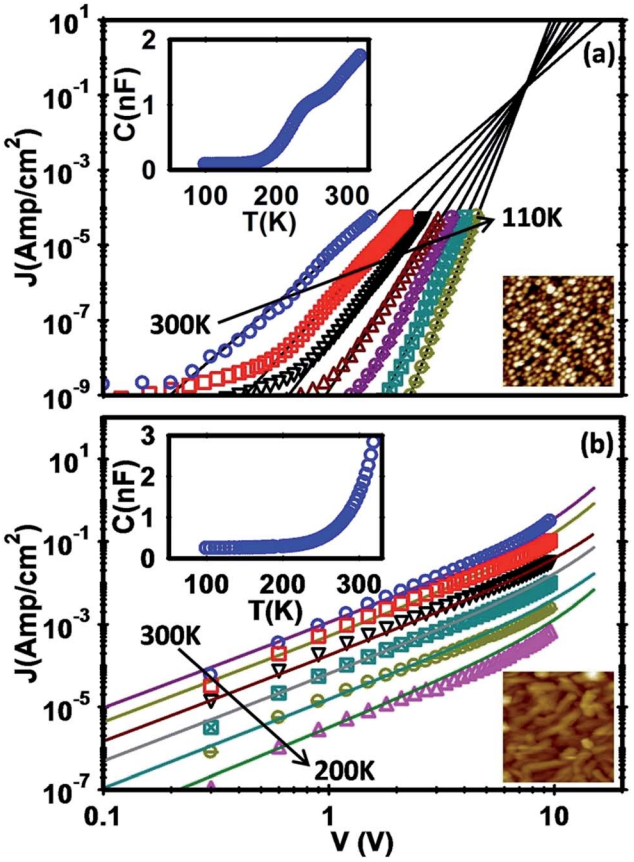

Fig. 4 Temperature dependent J–V characteristics of ITO/CuPc/Au based sandwiched devices in which CuPc thin films were grown at substrate temperature of (a) 30 °C and (b) 120 °C. Solid lines represent the theoretical fitting with TCLC [eqn (1)] (a) and SCLC with field dependent mobility [eqn (4)] (b), respectively. Upper insets show TSCAP measurements of Al/CuPc/Au based sandwiched devices with heating rate of 5 K min^{-1} in which CuPc thin films were grown at substrate temperature of (a) 30 °C and (b) 120 °C. Lower insets show the AFM (1 μm × 1 μm) of the CuPc thin films grown on ITO at substrate temperature of (a) 30 °C and (b) 120 °C.

$$V_c = \frac{qN_{tot}d^2}{2\varepsilon} \quad (3)$$

By extrapolating, log(J)–log(V) characteristics at various temperatures, V_c and N_{tot} are found to be ~8 V and 5.8 × 10^{16} cm^{-3}, respectively. N_{tot} is actually the concentration of interface states at grain boundaries, as will be shown below.

Fig. 4(b) shows the J–V characteristics of ITO/CuPc/Au based two terminal devices in which CuPc thin films were grown at T_G = 120 °C. Initially, the current increases linearly in this device, but as the bias increases, injected carrier density exceeds the intrinsic free carrier density and current follows SCLC.[34,35] SCLC is observed when there is either no or very low density of traps. In SCLC regime, slope starts from 2 and eventually increases with bias due to the field dependent carrier mobility $\mu(F,T)$, given by[36]

$$\mu(F,T) = \mu(0,T)\exp\left[\gamma(T)\sqrt{F}\right] \quad (4)$$

where $\mu(0,T)$ is the zero field charge carrier mobility and $\gamma(T)$ is the field activation factor. J–V characteristics have been simulated by solving the Poisson's equation, $dF/dx = qp(x)/\varepsilon$, describing the relationship between the electric field, F and the local charge density, $p(x)$ and continuity equation, $J(x) = qp(x)\mu[F(x),T]F(x)$ simultaneously.[34] Upper inset of Fig. 4(b) shows the TSCAP measurements of the corresponding device. We observe that there is no step in C–T characteristics. SCLC and absence of step further corroborates the absence of charge carrier traps in CuPc thin films grown at high T_G. Lower insets in Fig. 4(a) and (b) show the surface morphology of CuPc thin films grown on ITO at T_G = 30 °C and 120 °C, respectively. As discussed earlier, thin films at low T_G show nearly uniform distribution of isotropic grains and hence large number of in-plane interface states at grain boundaries. Charge carriers injected from ITO can be initially trapped by these large number of in-plane interface states in the first monolayer, resulting into TCLC along the perpendicular to the film. However, thin films at high T_G show rod like elongated nanowires providing very few soft grain boundaries, there will be less possibility of charge carriers injected from ITO, getting trapped by the in-plane interfacial states and charge transport occurs by the SCLC. We can conclude that charge transport, perpendicular to the film grown at low and high T_G takes place by two completely different mechanisms.

Characterization of traps from C–f characteristics

Fig. 5 shows the comparison of capacitance–frequency (C–f) characteristics of Al/CuPc/Au based Schottky diodes with traps (empty circles) and without traps (empty squares), under forward and reverse bias. In forward bias, initially, the capacitance decreases with frequency but beyond a certain frequency capacitance becomes independent of frequency. At higher frequency carriers are no longer able to follow the ac signal and contribution due to diffusion capacitance diminishes.[37] A step in C–f characteristics of the diodes with deep traps has been observed at ~1 kHz due to traps whereas this peak is absent in diodes without traps. In case of reverse bias, the capacitance is mainly determined by the depletion capacitance in low frequency region (in both the diodes with and without traps) and remains unresponsive at high frequency regions. Hence, under reverse bias, C–f characteristics of the diodes with and without traps are quite similar. In the forward bias, C–f characteristics over a wide range of frequency have been used to determine the energetic position and density of trap states.[36] At low frequency, all the traps are filled whereas at high frequency only those traps below certain demarcation energy (E_ω) will be filled and contribute to capacitance. E_ω is given by[38,39]

$$E_\omega = k_B T \ln\left(\frac{\nu}{\omega}\right) \quad (5)$$

where ν denotes an attempt-to-escape frequency, which is typically order of 10^{12} s^{-1} and $\omega = 2\pi f$, the angular frequency of the ac signal. So by varying the frequency, we can obtain the density of traps as a function of trap level. Following this approach, the traps distribution can be related to the derivative of the capacitance with respect to frequency and is given by[37]

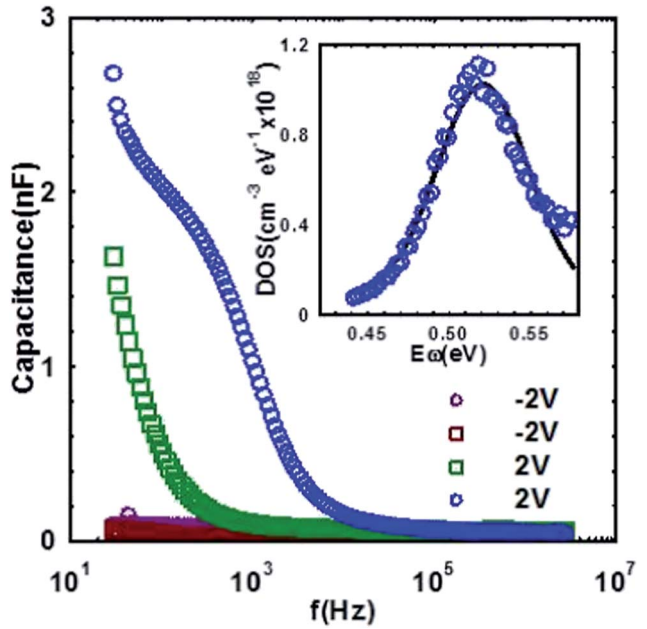

Fig. 5 C–f characteristics of Al/CuPc/Au based Schottky diodes in which CuPc thin films were grown at substrate temperature of 30 °C (empty circles) and 120 °C (empty squares). Insets show the energetic distribution of trap states obtained from C–f characteristics of the devices grown at 30 °C. Traps are absent in thin films grown at 120 °C. Solid line is fit with Gaussian [eqn (7)].

$$N_t(E_\omega) = \frac{V_{bi}}{qWk_BT}\frac{dC(\omega)}{d\ln\omega} \quad (6)$$

where W is the width of the depletion region and V_{bi} is the built-in potential due to different work functions of metal electrodes.[40] Inset of Fig. 5 shows the energetic distribution of trap states obtained by differentiating the C–f characteristics of Al/CuPc/Au based Schottky diodes with traps, under forward bias (2 V). Gaussian energetic distribution of traps has been observed in devices in which CuPc films were grown at low T_G. Width of energetic distribution of traps and position of the trap level with respect to HOMO has been obtained by fitting the experimental data with Gaussian distribution of traps as[41]

$$N_t(E_\omega) = \frac{N_{tot}}{\sqrt{2\pi}\sigma_t}\exp\left(\frac{(E_\omega - E_t)^2}{2\sigma_t{}^2}\right) \quad (7)$$

where σ_t is the width of energetic distribution of traps. Density of trap states as a function of energy along with fitting with eqn (7), results σ_t of 0.04 eV and the trap level at around 0.50 eV. The value of E_t matches well with those obtained independently from C–T characteristics. Hence C–f characteristics also corroborate the existence of deep traps in devices in which thin films were grown at low T_G.

Charge transport in *bc*-plane

Charge transport mechanism in OFETs with and without traps

The charge transport in *bc*-plane in CuPc has been investigated in field effect transistor (FET) geometry. To investigate the impact of the interface states on the charge transport mechanism in some quantitative way, we have estimated the maximum surface density of interfacial traps (N_s) in CuPc thin films grown at low and high T_G. Subthreshold swing (SS) is an important OFET parameter that can be used to estimate the density of these traps as,[42–44] $N_s = [SS\log(e)k_BT/q - 1]C_i/q^2$, C_i being the capacitance of dielectric constant per unit area. SS itself is estimated as,[42] $SS = [d\log(I_{DS})/dV_G] - 1$. SS for the OFETs fabricated at low and high T_G have been found to be 9.8 V per decade and 4.89 V per decade, respectively. Then N_s calculated form SS have been found to be 1.04×10^{13} cm^{-2} eV^{-1} and 5.18×10^{12} cm^{-2} eV^{-1}, for the OFETs at low and high T_G, respectively. It means that high density of grain boundaries creates additional interfacial traps in the CuPc thin films at low T_G.

Next, to understand the charge transport mechanism in polycrystalline thin films with different concentration of interfacial traps, μ as a function of carrier concentration (p) for the OFETs based on CuPc thin films with and without traps have been plotted in Fig. 6(a) and (b), respectively. Insets in Fig. 6(a) and (b) show the room temperature output characteristics (I_{DS}–V_{DS}) of the respective OFETs at different V_G. I_{DS} in OFETs without traps are almost two orders of magnitude higher than that in OFETs with traps. μ at different p have been calculated from the linear region of the (I_{DS}–V_{DS}) using the relation[26]

$$I_{DS} = \mu\frac{w}{L}C_i(V_G - V_T)V_{DS} - \frac{V_{DS}{}^2}{2} \quad (8)$$

where w is the channel width, L is the channel length and V_T is the threshold voltage. p has been calculated using the relation, $p = C_i(V_G - V_T)/qt$, t, being the thickness of the accumulation layer and has been taken 10 nm. The linear relation for the log(μ)–log(p) plots suggests the power law dependence of μ on p *i.e.* $\mu \propto p^n$, where n is the temperature dependent parameter.

Further, we observe the larger modulation in μ with V_G for the OFETs without traps compared to those with traps. Generally, the dependence of μ on p in OFETs can be explained as follows. Upon increasing V_G, the injected carriers fill the traps at grain boundaries and lower energy states at the edge of the HOMO or LUMO in the organic semiconductors and any

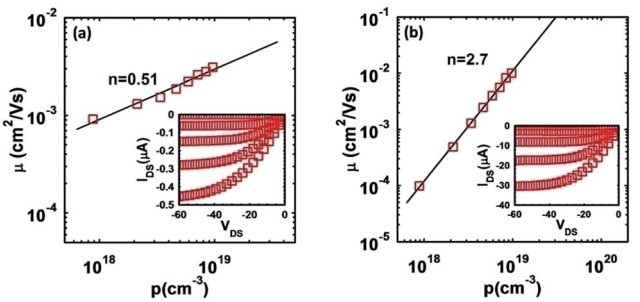

Fig. 6 Dependence of room temperature charge carrier mobility (μ) on charge carrier concentration (p) in CuPc based OFETs fabricated at substrate temperature of (a) 30 °C and (b) 120 °C. Insets show the room temperature I_{DS}–V_{DS} characteristics of respective OFETs at different V_G with a step of 20 V. Solid lines are power law fit $\mu \sim p^n$, where $n = T_{MTR}/T - 2$ or $T_{PM}/T - 1$, according to eqn (9) and (10), respectively.

additional charges will start to fill higher energy states towards the center, which require low activation energy to hop away to the neighboring sites, resulting higher μ with increasing V_G *i.e.* with increasing p. Hence for OFETs with traps, most of the charge carriers are captured by the interface states at grain boundaries *i.e.* grain boundaries impose significant barriers and prevent the charge carriers from reaching to transport level. Whereas for OFETs without traps, injected carriers easily fill the lower energy hopping sites existing in the tail of the GDOS and additional carriers occupy higher energy sites, resulting a sharp increase in mobility. In a recent study, similar effect of grain boundaries on the current modulation with gate bias has been observed.[45]

MTR or PM

Now, let's apply two well known models: MTR[11,12] and PM[14] to the OFETs with and without traps. In the MTR model, the localized levels between HOMO and LUMO serve as traps for charge carriers. Depending on the trap depth, T and V_G, the carriers temporarily get released by thermally activated process to HOMO. Under the influence of V_G, μ gradually increases due to increased carrier concentration excited to the extended states *i.e.* activation of carriers from a localized state to HOMO. According to this model the charge carrier mobility, μ in OFETs is given by[17]

$$\mu^{MTR} = \mu_0^{MTR}\left[\frac{C_i V_G}{qN_t}\right]^{\frac{T_{MTR}}{T}-2} \quad (9)$$

where μ_0^{MTR} is weakly temperature dependent prefactor, T_{MTR} is the characteristics temperature which defines σ_t for the trap states as $\sigma_t = k_B T_{MTR}$. From Fig. 6(a) and (b) and using eqn (9), we get T_{MTR}, 753 K and 1410 K for the devices with and without traps, respectively and the corresponding width of the energetic distribution of trap states are found to be 61 meV and 130 meV respectively. The width of energetic distribution of traps (~60 meV) obtained from MTR model for CuPc thin films grown at low T_G matches well with the value obtained from *C–f* characteristics but the value obtained for thin films grown at high T_G is more than the width of HOMO (100 meV).

Moreover, MTR model estimates, the width of energetic distribution of traps to be larger for the OFETs without traps than for the OFETs with traps which is contradicted. Hence charge transport in organic thin films having traps is governed by MTR model but the same model is not applicable for thin films without deep traps. However, same data can be analyzed by PM. According to this model,[14] charge carriers move due to thermally activated hopping within the localized states in the energetically distributed density of states (DOS) of HOMO or LUMO. In this model, the charge carrier mobility, μ in OFETs is given by[14,46]

$$\mu^{PM} = \mu_0^{PM}\left[\frac{(C_i V_G)^2}{2k_B T_{PM}\varepsilon_s}\right]^{\frac{T_{PM}}{T}-1} \quad (10)$$

where μ_0^{PM} is weakly temperature dependent prefactor and T_{PM} is the characteristic temperature which represents the width of HOMO and LUMO as $\sigma_{PM} = k_B T_{PM}$. From Fig. 6(a) and (b) and using eqn (10), we get T_{PM}, 453 K and 1110 K in the devices with and without traps respectively and the corresponding width of the DOS are found to be 45 and 95 meV, respectively. The calculated width of the DOS for OFETs without traps is around ~100 meV which is the typical width of the HOMO or LUMO in organic semiconductors.[47] The unusually low value of width of DOS with traps indicates that PM model which is otherwise successful[48] in case of OFETs without traps, is not suitable for OFETs having traps.

Temperature dependence of μ in *bc*-plane of CuPc thin films with and without traps

To justify our arguments on the charge transport mechanism in the OFETs with and without traps, we have also performed temperature dependent measurements on I_{DS}–V_{DS} and μ as a function of T, for different V_G have been plotted in Fig. 7. As can be seen in Fig. 7(a), μ at different V_G in OFETs with traps follow Arrhenius temperature dependence, $\ln \mu \sim 1/T$. Arrhenius like temperature dependence of μ interprets that MTR model should be able to successfully explain the charge transport in OFETs with traps.[43] However, non-Arrhenius-like temperature dependence of μ, ($\ln \mu \sim 1/T^2$) can be seen in the OFETs without traps in Fig. 7(b) which is a direct consequence of the hopping transport within the GDOS in organic semiconductors, as discussed in correlated Gaussian disorder model (CGDM).[49,50] Hence, PM, based on VRH seems to be applicable to explain charge transport in OFETs without traps.

Anomalous temperature dependence of I_{DS} in OFETs with traps

To reveal the nature of traps and their resulting impact on charge carrier transport in disordered organic semiconductors, temperature dependence of I_{DS} at two different V_G of 60 V and 90 V for OFETs based on CuPc thin films having traps has been shown in Fig. 8(a). Initially I_{DS} decreases with decreasing temperature but at around 75 K and 65 K for $V_G = 60$ V and 90 V, respectively, magnitude of current increases suddenly by several orders and then remains almost constant. This anomalous behavior in current–temperature (I_{DS}–T) characteristics can be explained on the basis of grain boundary controlled charge carrier transport in CuPc thin film with traps.[51] Fig. 8(b) shows the energy-level diagram including band-bending due to the trapping of positive charge at the grain boundary interface in CuPc thin films. High density of localized energy levels inside the band gap of the semiconductor exists due to the interface states lying between grain boundaries in polycrystalline thin films with traps.[50,51] The levels which lie below the Fermi level E_F, are filled, at thermal equilibrium. Consequently, a negative charge at the interfaces and space-charge regions on the both sides, of grain boundaries are generated. Positive charge,

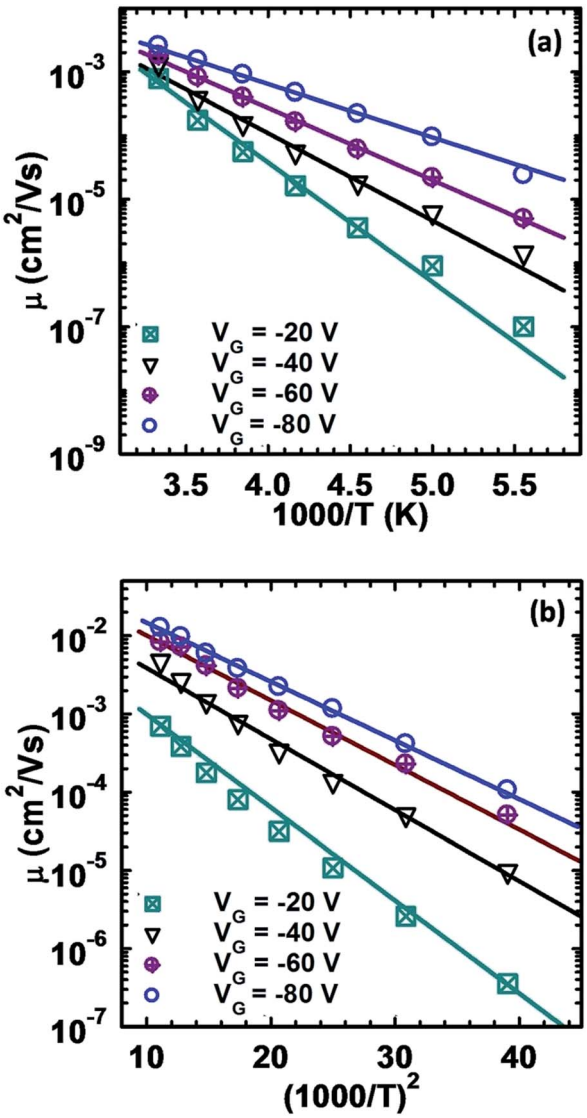

Fig. 7 Temperature dependence of μ, measured at different V_G for CuPc OFETs (a) with and (b) without traps. Solid lines in (a) and (b) represent the fitting according MTR model and PM, respectively.[43,48]

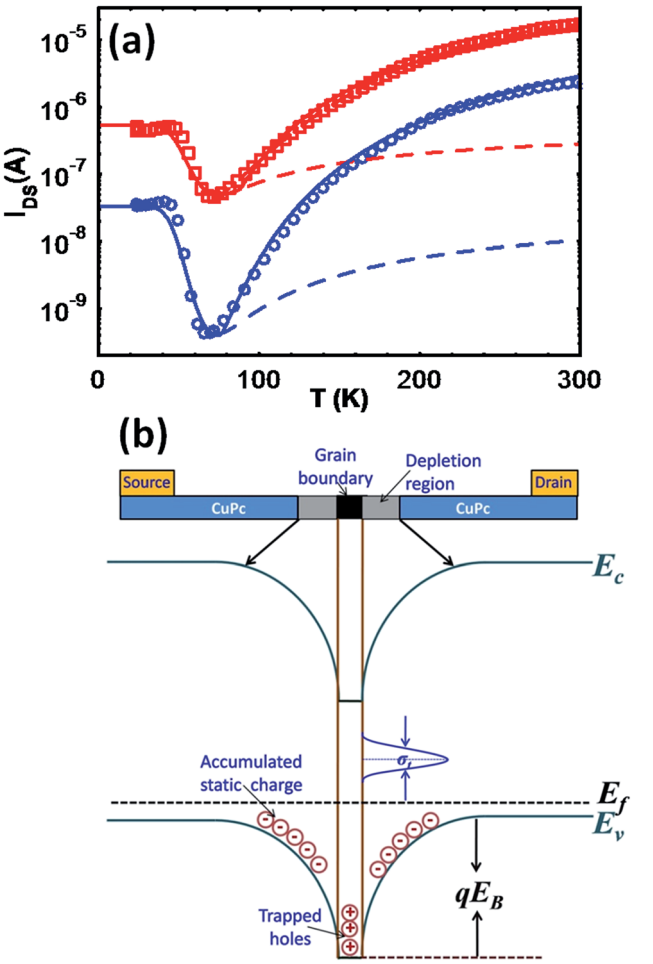

Fig. 8 (a) Temperature dependence of I_{DS} at $V_G = 60$ V (open circle) and $V_G = 90$ V (open square) for OFETs based on CuPc thin films with traps. Abrupt increase in I_{DS} at ~75 K for $V_G = 60$ V and at ~65 K for $V_G = 90$ V has been observed. Dashed lines represent the theoretical fitting according to eqn (14), without inclusion of hopping barrier (Δ) *i.e.* by putting $\Delta = 0$ in eqn (14) whereas solid lines represent the theoretical fitting with a finite value of Δ. (b) The schematic representation of energy-level diagram including band-bending at grain-boundary interface in CuPc thin films. E_c and E_v represent the LUMO and HOMO edges, respectively and E_F is the equilibrium Fermi level.

trapped at the grain-boundary interface creates a potential barrier for charge carrier transport and the height of this barrier (E_B) can be estimated[51,52]

$$E_B = \frac{q^2(n_T)^2}{8\varepsilon N_A} \quad (11)$$

where N_A is the acceptor concentration inside the grain, n_T is the density of occupied traps at grain boundary interface. n_T depends on the Fermi level, hence on T and for a Gaussian distribution of trap in organic semiconductors, can be given by[50]

$$n_T = \int_0^\infty \frac{N_{tot}}{\sqrt{2\pi}\sigma_t} \frac{\exp\left[\frac{-(E-E_t)^2}{4\sigma_t^2}\right]}{1+\exp\left[\frac{(E-E_F)}{k_B T}\right]} dE \quad (12)$$

where E_T represents the maximum height of the Gaussian distribution. E_F is given by

$$E_F(T) = k_B T \ln[N_V/p] \quad (13)$$

I_{DS}, in polycrystalline thin films with large number of grains is controlled by the rate of charge carrier jumps across the grain boundary as[53]

$$I_{DS} = I_0 \exp[-(E_B + \Delta)/k_B T] \quad (14)$$

where Δ is an additional barrier due to hopping conduction. Experimental I_{DS}–T characteristics have been simulated according to the eqn (11)–(14) and results are also presented in Fig. 8(a). It is to be noted that in low temperature region (upto around 75 K and 65 K for $V_G = 60$ V and 90 V, respectively), I_{DS}–T

characteristics can be excellently fitted without inclusion of Δ *i.e.* after putting $\Delta = 0$ in eqn (14). Hence at low temperatures, charge transport in polycrystalline thin films is completely controlled by grain boundaries. However, at high temperature simulation results deviate from experimental one (dashed lines in Fig. 8(a)) because an additional barrier Δ due to hopping conduction also contributes. Hence for temperatures higher than ~75 K and 65 K for $V_G = 60$ V and 90 V, respectively, Δ has a finite value. After adding Δ to E_B, experimental data could be excellently fitted at high temperatures (shown by solid lines in Fig. 8(a)). From fitting Δ has been found to be 82 meV and 43 meV for $V_G = 60$ V and 90 V, respectively.

Conclusions

In conclusion, we have identified and characterized the traps in polycrystalline organic thin films of CuPc using two and three terminal devices. It has been found that the trap density can be controlled by varying growth conditions and CuPc thin films grown at low substrate temperatures are proved to have large concentration of traps. The presence of traps is analyzed by TCLC in two terminal devices. *C–f* and *C–T* characteristics also demonstrate the presence of traps in CuPc thin films grown at low TG. Width of the trap distribution from MTR model is in agreement with that obtained independently from *C–f* characteristics of CuPc based organic Schottky diodes. Hence MTR model can be applied to the charge carrier transport in polycrystalline organic thin films with isotropic grainy structure. Charge carriers trapped by interface states at grain boundaries cannot hop to HOMO or LUMO unless they get sufficient energy to be released because trapped charges at the grain-boundary interfaces lead to the formation of a potential barrier for charge transport process. Polycrystalline thin films grown under favorable growth conditions to achieve anisotropic morphology with fewer grain boundaries seem to be providing a percolative passage for the carrier transport.

Conflicts of interest

There are no conflicts to declare.

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