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Investigation of micro- and nanoscale barrier layer capacitance mechanisms of conductivity in $CaCu_3Ti_4O_{12}$ *via* scanning probe microscopy technique†

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In this work we disclose micro- and nanoscale origins of the unusually high dielectric constant characteristic of $CaCu_3Ti_4O_{12}$ (CCTO) ceramic by using the Scanning Probe Microscopy (SPM) technique. Two main mechanisms responsible for the colossal dielectric constant specific to the CCTO compound have been revealed. There is a microscale barrier layer capacitance (MBLC) mechanism, attributed to the potential grain-to-grain barriers, and a nanoscale barrier layer capacitance (NBLC) mechanism, attributed to the potential barriers created by the structural defects such as twinning or slip planes. Using the contact spreading resistance mode of SPM, we have found two types of surface morphology which, being originated from planar defects, can be related to the NBLC mechanism. A clear confirmation of NBLC as the origin of the huge dielectric constant in CCTO has been obtained *via* the local current–voltage dependence measurements. By using this method, we have found the existence of two sources of conductivity (charge transfer and charge hopping) which simultaneously contribute to the NBLC mechanism. These sources (providing semiconducting and n-type conducting behavior, respectively) have been associated with the different stacking faults predicted for CCTO. The present work promotes a general understanding of anomalous colossal dielectric constant behavior in CCTO material at the macro- and nanoscale levels.

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Introduction

Dielectrics with colossal dielectric constant ($\varepsilon > 10^3$) are a matter of great interest since their use as passive components could provide an improvement in the efficiency of electronic devices and ensure the miniaturization of capacitive electronic elements. These materials can find application as high energy-density storage capacitors (usually referred to as super-capacitors), as high-k gate oxides for field-effect transistors or as microwave dielectric resonators, substrates and other microwave elements. Nowadays, only five mechanisms underlying the colossal dielectric constant (CDC) are recognized. Those are ferroelectricity, charge-density wave formation, hopping charge transport, metal-insulation transition and interface effects.[1] Most of the capacitive materials that are being used in electronic industry exploits ferroelectricity as the main origin of CDC. Among them, $BaTiO_3$, $PbZr_{1-x}Ti_xO_3$ and $Ba_{1-x}Sr_xTiO_3$ are the most representative ones. However, this class of materials exhibits a strong temperature dependence of dielectric properties related to the existence of a ferroelectric phase transition. This fact implies some limitations to the application of ferroelectrics as CDC in certain cases.

Calcium copper titanate, $CaCu_3Ti_4O_{12}$ (CCTO), a non-ferroelectric material, whose exceptional dielectric properties were for the first time reported in 2000,[2] attracted the attention of the scientific community because of its CDC ($\varepsilon > 10^5$), observed both in ceramics and single crystals. Moreover, the absence of ferroelectric transition makes CCTO properties quite stable, with a wide range of temperature-independent dielectric behaviour. However, the manifestation of high dielectric losses ($\tan\delta > 0.1$), particularly for frequencies around the typical Maxwell–Wagner dielectric relaxation (~MHz) deteriorates the exclusive permittivity properties of CCTO.[3] Besides the challenge linked with the optimization of CCTO properties, regarding its possible prospects to applications in electronic devices, a conclusive explanation about the polarization mechanisms that could justify the dielectric behaviour of CDC is still missing. Discarding the existence of any ferroelectric nature due to geometrically frustrated symmetrical off-center displacement of Ti ions, and/or any other lattice contribution,[4] the experimental data, collected during the last decade,

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point out to extrinsic barrier mechanisms as the main origin of the observed dielectric polarization. Sinclair *et al.*[5] admitted the CDC of CCTO to be the result of an electronically heterogeneous microstructure associated with the semiconducting grains having the insulating surfaces formed during the sintering process. These internal barrier layers, formed by the interface grain-to-grain boundary, operate as multiple micro-capacitors, accumulating electric charge at the grain surfaces when an external electric field is applied. This model correctly explains the behaviour of polycrystalline CCTO samples,[6,7] but fails to justify the CDC values measured in CCTO single crystals. Alternatively, Krohns *et al.* proposed the effect of the electrode–sample interface, known as electrode process polarization state.[8] This polarization may arise from the depletion layers of Schottky or metal–insulator–semiconductor (MIS) diode structures at the interfaces between the metallic electrodes and the bulk sample.[8] Although this effect can occur both in polycrystalline and single crystal CCTO samples, this hypothesis was later discarded. Since the removal of samples surface does not change, as much as expected, the CDC values of the samples, electrode polarization process cannot stand as the main polarization mechanism.[9] Other barrier models, valid for poly and single crystals, were firstly suggested by Subramanian *et al.*[10] and further developed by Bueno *et al.*[11] In ref. 10, the plane defect model due to the twinning parallel to the (100), (010), and (001) planes was proposed as a plausible microscopic explanation for the gigantic dielectric constants in CCTO material and the local electronic structure of twinning planes were examined precisely. In ref. 11, this approach was significantly developed and manifested as a polaronic stacking fault defect model. In this model, the stacking faults at the nanoscale level work as a large association of internal barrier layer capacitors, thus resulting in the huge dielectric constant observed in CCTO based materials. This phenomenon was named as nanoscale barrier layer capacitance (NBLC) mechanism and a huge enhancement of polaronic defects was predicted. Later on, Ribeiro *et al.* showed that the Debye relaxation process appearing in polycrystalline CCTO samples at high frequency had polaronic nature.[12]

Nevertheless, the conductivity process within the CCTO grains is still an open question. Both electron transfer through polarons[11] and localized hopping charge carriers,[13] confined within small domains, can explain the conductivity behavior in CCTO ceramics. Two kinds of morphologies were initially identified in polycrystalline CCTO ceramic samples: terraces with ledges and bump domains.[14] These structures were observed inside grains after treating the samples at higher etching temperatures and longer etching times (as compared with a conventional preparation procedure). The self-intertwined domain structures inside the grains of the polycrystalline CCTO were investigated in details by scanning electron microscopy (SEM) and high-resolution transmission electron microscopy (HRTEM) in ref. 15. The main origin of the observed morphologies was found to be associated with screw-like dislocations resulting from spiral growth of the crystal.

In this work, we present an experimental confirmation for the inhomogeneous conductivity in CCTO ceramics that is measured at the macro- and nanoscale levels. Two main mechanisms responsible for the colossal dielectric constant behaviour of the CCTO sample were found. There is a micro-scale barrier layer capacitance (MBLC) mechanism, attributed to the potential grain-to-grain barriers, and a nanoscale barrier layer capacitance (NBLC) mechanism, attributed to the potential barriers, which are created by the structural defects such as twinning or slip planes. An adequate interpretation of the nanoscale dielectric responses based on the appropriate existing models (electrical equivalent circuit containing MBLCs and NBLCs parts) and its comparison with the macroscopic complex impedance experimental data are presented.

Methodology

Synthesis of the sample

Ceramic pellet of CCTO was prepared by a conventional solid state reaction method using the powders of calcium carbonate $CaCO_3$ (Fluka, Honeywell Research, 99%), titanium oxide TiO_2 (Sigma-Aldrich, 99%) and copper oxide CuO (Sigma-Aldrich, 99%) taken in stoichiometric cation ratio. The reagents were mixed in a planetary mill during 20 min at 200 rpm, and the mixture was calcinated at 900 °C for 12 h. The calcined powder was grinded using a mortar and a pestle and uniaxially pressed into cylindrical pellets with a diameter of 12 mm and a thickness of 3 mm by applying 1.2 tons load for 5 min. Sintering was performed at 1050 °C for 12 h. The sintering temperature was chosen in agreement with the previous study,[6,16] showing the clear benefits of the corresponding temperature range in comparison with other tested temperatures. Grinding and mechanical polishing of the sintered sample was performed using SiC abrasive papers (ranging from 500 to 1200 grits) and diamond paste. To reveal the grain boundaries, the mechanically-polished sample was thermally etched at 950 °C for 1 h.

Measurement details

Structural analysis was performed using a Philips X'pert diffractometer with Cu Kα radiation. The X-ray diffraction (XRD) pattern was collected in the angle range $10^\circ \leq 2\theta \leq 80^\circ$ with a step of 0.026° and a dwell of 2 s per step. The diffraction data were analyzed by the Le Bail method[17] using the FullProf software package.[18] The microscale morphology and chemical analysis of the sample were performed using a Hitachi S4100-1 scanning electron microscope (SEM) equipped with an energy-dispersive X-ray spectroscopy (EDS) detector. The dielectric properties of the sample were measured with an Agilent 4294A LCR meter within a frequency range from 40 Hz to 110 MHz. For this measurement, the opposite sides of the samples were painted with silver paste. All the dielectric measurements were done in a homemade cryostatic bath system within the temperature range between 86 and 350 K. The dielectric setup was implemented in C_p–R_p configuration which allows measuring the complex permittivity:

$$\varepsilon^*(\omega) = \varepsilon'(\omega) - i\varepsilon''(\omega), \quad (1)$$

and calculate ε' and ε'' according to the equations:

$$\varepsilon''(\omega) = \frac{d}{\omega R_p A \varepsilon_0} \quad (2)$$

$$\varepsilon'(\omega) = C_p \frac{d}{A\varepsilon_0} \quad (3)$$

where d is the sample thickness, A is the electrode area, ε_0 is the vacuum permittivity, R_p and C_p are the resistance and capacitance of the sample, respectively, measured in a parallel RC circuit configuration. Finally, the nanoscale morphology and conductive properties of the sample were investigated using a NTEGRA Aura (NT-MDT) scanning probe microscope (SPM) operating in Atomic Force Microscopy (AFM) and Spreading Resistance (SR) modes. Since SR mode suggests a tight tip-surface contact, the setpoint level (controlling the contact stiffness) was chosen as 1.5 times exceeding the value recommended for ceramic samples measured in contact modes. The SR measurements were done at a slow scan rate of 0.1 Hz. The RMS roughness of a typical 5 μm × 5 μm scan was about 5 nm (Fig. 1-ESI†). A range of dc bias voltage applied during the SR scanning varied between 0.5 and 10 V. The stiff NSG30 (NT-MDT) probes (320 kHz, 40 N m^{-1}, Pt/Ir coating) have been used. Taking into account that the Pt/Ir metal coating wears off the tip rather easily and this further accentuates topographic artefacts, every new set of scans was done with a new tip. The tips were examined for the wear off and damage by comparing the resonance frequency before and after scanning and by controlling the SR image decay (Fig. 2-ESI†). The topography and SR calibration was done on a calibration grid (TGQ1, NT-MDT) at room temperature and humidity of about 30% using the scan parameters described above.

Results and discussion

It has been previously reported that CCTO ceramics contain crystal grains whose size can vary in a very broad range.[19] Fig. 1(a) illustrates a polished surface of CCTO sample and demonstrates this wide (from 5 μm to 50 μm) grain size distribution. The presence of CuO impurities, as a segregation phase around the CCTO grains, has been revealed by the EDS measurements (Fig. 1(b)). The CCTO is, however, the major phase presented in the sample, as can be seen from the XRD data shown in Fig. 1(c).

Fig. 2 presents the real and imaginary parts of the dielectric permittivity spectra. For all the studied temperature range [86–350 K], the dielectric relaxation decays are easily identified through the huge decrease of ε' followed by an increase of ε'' which reaches its maximum shifting towards higher frequencies with increasing temperature. The Debye-like dielectric relaxation presents a static dielectric constant (ε_s), which slightly increases with temperature and reaches 7943 at 90 K. This value is sufficiently high to consider the investigated CCTO sample as a material with colossal dielectric constant. Although the values of ε' and ε'' increase in low frequency region (f < 1 kHz) and at temperature above 300 K, this could be explained by the appearance of Jonscher low-frequency dispersion.[20] At the low frequency range, the imaginary part of the complex dielectric constant (ε'') depends on frequency according to Jonscher's power law:

$$\varepsilon'' = K(T)\omega^{n-1} \quad (4)$$

where $K(T)$ is a frequency independent parameter and n is a constant ($0 < n < 1$). This dispersion phenomenon is affected by an interfacial effect at the electrode/sample surface region that promotes the accumulation of charge carriers at these interfaces.[5,6] The imaginary part of complex permittivity spectra (ε'' *vs.* log f) within the several temperatures (see in Fig. 2(a)) presents the dielectric relaxation peaks at high frequency region which can be associated to the bulk dielectric response. Once this relaxation process is thermally activated, Arrhenius law was used to calculate the activation energies associated with this process. The variation of relaxation frequency (f_{max}) with temperature is expressed by the equation:

$$f_{max} = f_0 e^{-E_a/KT} \quad (5)$$

where f_0 is the relaxation frequency for high temperature and E_a the activation energy for the relaxation process. The linear fitting of ln f_{max} as a function of the inverse temperature ($1/T$) is presented in Fig. 2(b). The analysis of fitting curve and the linearization of eqn (5) gave the activation energy value of 100 ± 2 meV for observed relaxation process. Comparing this result with the literature reporting the activation energy of polaronic relaxation process in more than 50 perovskites,[21] we notice an evident proximity of CCTO to the same polaronic relaxation behaviour.

The experimental result on conductivity of the sample at high frequencies has also revealed a strong polaronic nature of dielectric permittivity (Fig. 2(c)). Indeed, at low temperature conditions (T < 200 K) and high frequency (f > 1 kHz) the conductivity behaviour of the CCTO sample obeys the Universal Dielectric Response (UDR):[20]

$$\sigma = \sigma_{dc} + \sigma_0 f^s \quad (6)$$

where σ_{dc} is the dc bulk conductivity, σ_0 a constant, f the frequency and s an exponent (s < 1). The performed fitting of σ *vs.* frequency done in the temperature range from 86 K to 150 K by using the eqn (6) is consistent with the UDR phenomenology at high frequencies (Fig. 2(c)). The calculated values of s, σ_0, and σ_{dc} are presented in Table 1.

The employment of scanning probe microscopy technique implemented in contact atomic force microscopy and spreading resistance microscopy modes allowed the analysis of CDC phenomena at the micro- and nanoscale levels to be performed. The AFM study of the surface morphology (Fig. 3(a)) revealed a broad (ranging from 5 μm to 50 μm) grain size distribution, thus confirming the data obtained with the SEM technique (Fig. 1(a)). The current distribution correlates with topography and a clear difference between the grains and grain boundaries can be seen (Fig. 3(b)). These results are consistent with the so-called macroscale barrier layer capacitance (MBLC) mechanism of conductivity described in details in ref. 5 and 6. The MBLC

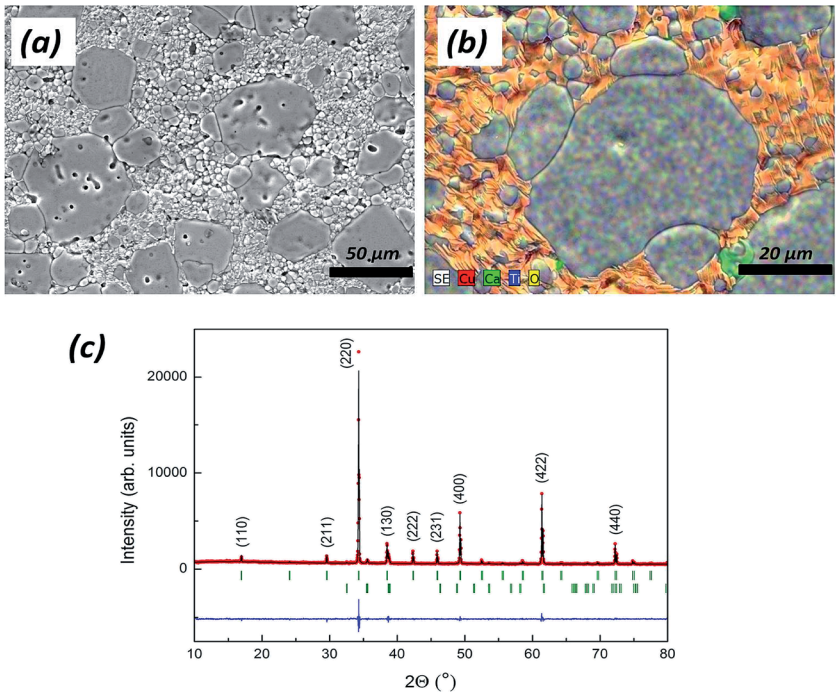

Fig. 1 Microscopy images of CCTO sample obtained with (a) SEM and (b) EDS mapping. (c) Observed (red symbols), calculated (black line) and difference (blue line) XRD patterns obtained for the $CaCu_3Ti_4O_{12}$ sample (a = 7.393(1) Å, space group $Im\bar{3}$) at room temperature. Tick marks indicate the positions of allowed Bragg reflections for the main phase (upper row, the most intensive peaks are indexed) and for the CuO impurity (lower row).

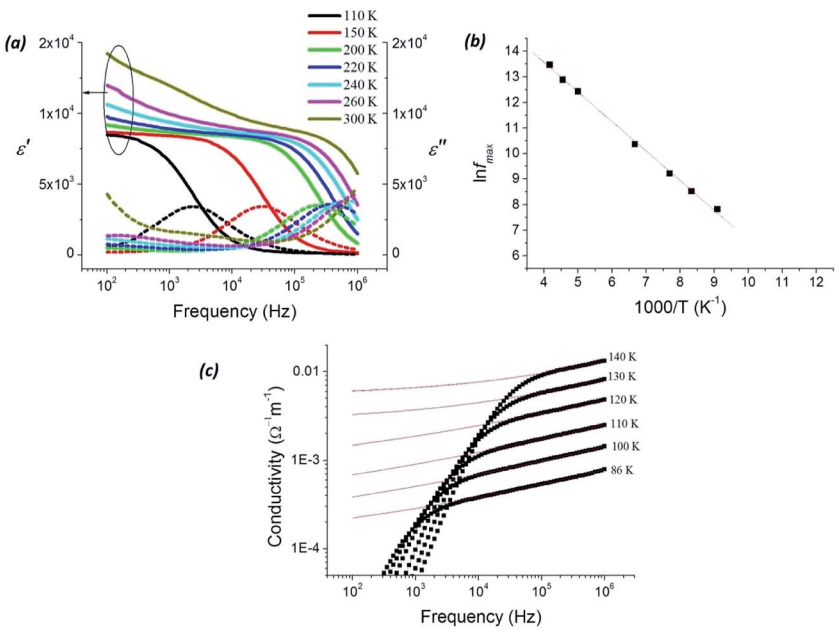

Fig. 2 The real and imaginary dielectric permittivity spectra (a), Arrhenius law (b) and universal dielectric response (c) fittings.

mechanism is considered as controlling the conductivity behavior at the macroscale level. It is known as the main origin of CDC in CCTO materials.[5–9] In agreement with the predictions given in ref. 5 and the measurements carried out in ref. 6, we revealed, by using the SPM technique, the higher concentration of charge carriers near the grain boundaries (Fig. 3(b)). This effect has been described in details by Sinclair *et al.*,[5] which showed that during the sintering process the semiconductive grains partially oxidized and the insulating grain boundaries were formed. This phenomenon causes the arising of Schottky type barriers acting as an association of multiple micro-capacitors and resulting in electric charge carrier

Table 1 Parameters and error of UDR function fitting

T (K)	σ_{dc} (Ω^{-1} m^{-1})	σ_0 (Ω^{-1} m^{-1})	s	$\Delta\sigma_{dc}$ (Ω^{-1} m^{-1})	$\Delta\sigma_0$ (Ω^{-1} m^{-1})	Δs
86	1.2×10^{-4}	4.0×10^{-5}	2.0×10^{-1}	0.2×10^{-4}	0.5×10^{-5}	0.7×10^{-4}
100	1.7×10^{-4}	9.0×10^{-5}	1.9×10^{-1}	0.3×10^{-4}	1.0×10^{-5}	0.6×10^{-4}
110	2.7×10^{-4}	1.8×10^{-4}	1.8×10^{-1}	0.5×10^{-4}	0.2×10^{-4}	0.6×10^{-4}
120	7.9×10^{-4}	2.8×10^{-4}	1.9×10^{-1}	0.3×10^{-4}	0.9×10^{-5}	0.2×10^{-4}
130	2.7×10^{-3}	1.8×10^{-4}	2.5×10^{-1}	0.9×10^{-4}	0.2×10^{-4}	0.5×10^{-4}
140	5.4×10^{-3}	1.8×10^{-4}	2.7×10^{-1}	0.4×10^{-3}	0.4×10^{-4}	0.1×10^{-3}

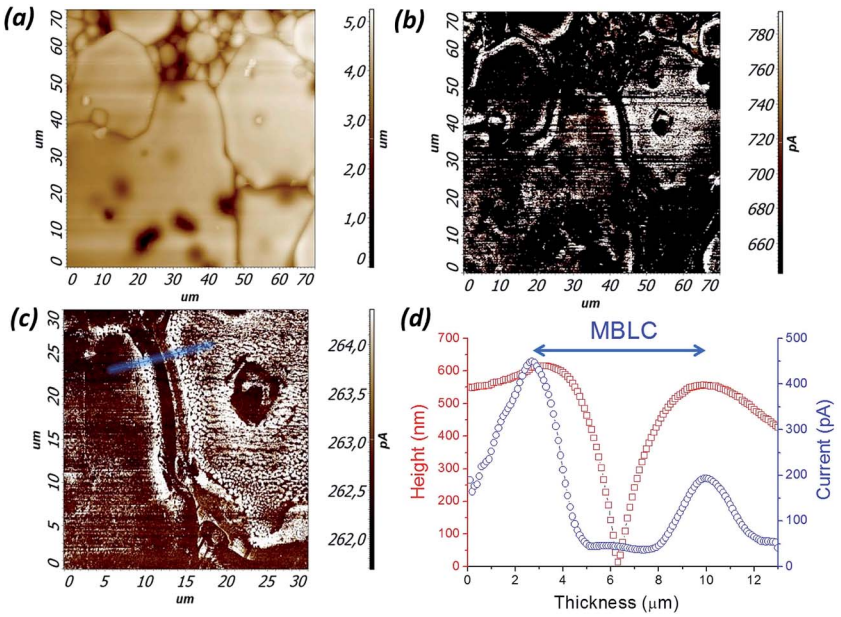

Fig. 3 (a) Surface topography, (b and c) spreading resistance scan images and (d) MBLC height and current profiles. The scanning was done at 0.1 Hz (512 × 512 pixels) and dc bias voltage of 1 V.

accumulation. Thus, in this work we show, for the first time, the evidence of the charge accumulation states near the CCTO grain boundaries which were measured experimentally at the micro-scale level (see Fig. 3(c and d)). The current distribution scan image within the two grains illustrates the MBLC mechanism and its conductivity pattern, including charge carriers' accumulation states at grain boundaries and insulating gap between them. An average width for the insulating gap between the grains is around 5 μm with a depth of around 500 nm. The mean current drop between the conductive and insulating states attains 0.5 nA (Fig. 3(d)).

However, the MBLC mechanism seems not to be solely responsible for CDC properties in CCTO ceramics. The additional mechanism should originate from the existence of an insulating/conductive mesh inside CCTO grains, as can be seen from Fig. 3(c). As the scan resolution is increased, the complex topography of separate CCTO grain becomes seen (Fig. 4(a)). It has been previously reported[14,15] that there are two types of surface morphologies which could be found on the surface of CCTO by using the scanning electron microscopy (SEM) and high-resolution transmission electron microscopy (HRTEM) techniques. There are terrace-ledge and bump domain morphologies associated with the spiral growth of crystals *via* a screw dislocation. In our research we confirm the coexistence of these morphologies *via* the contact AFM measurements (Fig. 4(a), Fig. 3-ESI†) and describe the bump domains (in our work we named it as "a mesh-type morphology") as also composed of terrace-ledge domains. It has been suggested[14] that grain morphology in CCTO is strongly affected by synthesis conditions. It has been pointed out that the increase in sintering time suppresses the terrace-ledge morphology and promotes changes in the state of the spiral growth dislocations.[14] Moreover, it has been shown that the terrace-ledge morphology appears only under thermal etching.[14] All these conditions are expected to cause a huge difference in the conductivity behavior of the areas associated with the different morphological types. In the current work we present the experimental evidence for this prediction by using the contact spreading resistance mode measurements.

As can be seen from Fig. 4(b), the current distribution matches with the topography scan image and presents a clear mapping of conductive behavior for different type of surface morphologies. A precise scan of terrace-ledge domain area was done at the region limited by a red square (see in Fig. 4(a)). The

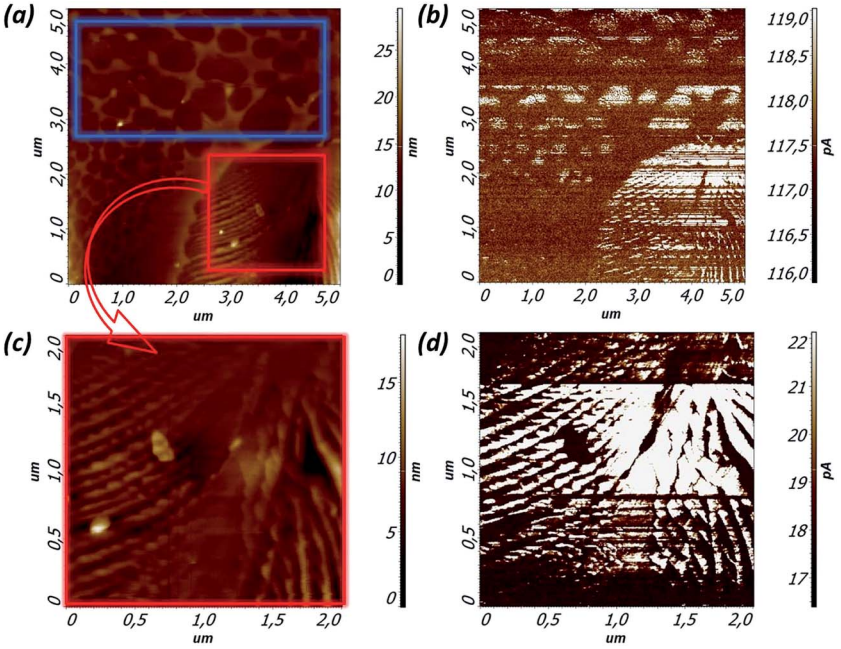

Fig. 4 (a, c) Surface topography and (b, d) spreading resistance scan images for terrace-ledge (red square) and mesh type (blue rectangle) morphology areas of CCTO sample. The scanning was done at 0.1 Hz (512 × 512 pixels) and dc bias voltage of 1 V.

results of morphology and current distribution scans are presented in Fig. 4(c and d). As follows from the scan image analysis, the terrace-ledge domain area represents an alternation of barriers and gaps in topography image scan which correspond to the conductive and insulating stripes in current distribution image scan. An average width and height of the barriers were 100 nm and 2 nm, respectively. The corresponding current, when a dc bias voltage of 5 V was applied, was about 10 nA. Based on the previous theoretical predictions[10,11] and some indirect measurements,[11–15] we claim the direct evidence for the nanoscale barrier layer capacitance (NBLC) mechanism of conductivity.

Generally, the theory of NBLC mechanism is based on collective effect of negatively charged TiO_5 clusters of the stacking fault substructure, which forms a polaronic defect with neighboring Cu^{2+} atoms.[10] Moreover, it has been predicted that these defects are the most likely reason for the maintenance of the high dielectric constant at the high frequency, up to the MHz range.[20] It has been shown[12–15] that the conductive properties within the grains of polycrystalline CCTO are dependent on both nanoscale internal barriers and electronic conduction paths. This model has been discussed by considering a configuration that gathers conduction barrier and insulating polaronic plane.[11,12] In the present work we confirm this prediction *via* the direct visualization of dual conductivity behavior of CCTO grain at the nanoscale level, which demonstrates the existence of conductive barriers and insulating gaps (polaronic plane). Thus, the results obtained in this work represent the first direct assessment of the NBLC electrical response, performed at the nanoscale level.

A precise scan of mesh type morphology area is presented in Fig. 5(a), where the coexistence of bump and terrace-ledge domains can be seen. However, only the terrace-ledge domain area was found to be conductive, as follows from the current distribution image scan (Fig. 5(b)). The detailed scan of terrace-ledge domain area, included in the mesh type morphology, is presented in Fig. 5(c). A clear contribution of NBLC mechanism associated with the alternation of conductive barriers and insulating gaps was revealed (Fig. 5(d)). An average width and height of the barriers were 200 nm and 2 nm, respectively. These results are quite similar to those obtained for the area shown in Fig. 4(c and d). However, the corresponding current behavior is dramatically different from that observed for the previously studied terrace-ledge morphology area. To distinguish the difference between the terrace-ledge domains, we denote those unrelated to the mesh type morphology as "terrace-ledge 1" (Fig. 4(a and c)) and those related to the mesh type morphology as "terrace-ledge 2" (Fig. 5(a and c)).

We consider that the alternate conductive barriers and insulating gaps that appear in both terrace-ledge and mesh type morphology areas have the same origin – the NBLC mechanism. The point is that there is a noticeable difference between them, as clearly revealed by the dissimilar conductivity behavior. The comparison of the two morphology areas demonstrates that when 1 V dc bias voltage is applied, a mean current response of 22 pA (Fig. 4(d)) and 2.6 pA (Fig. 5(d)) is measured for the terrace-ledge 1 and terrace-ledge 2 domains, respectively. Another difference appears in the mean width (100 nm *vs.* 200 nm) of conductive barriers for terrace-ledge 1 and terrace-ledge 2 domains (Fig. 6(a and b)).

The origin of the difference in the conductivity behavior has been investigated *via* the local current–voltage measurements. The *I–V* curves have been obtained on conductive and insulating parts of NBLC structure in order to reveal the maximum current

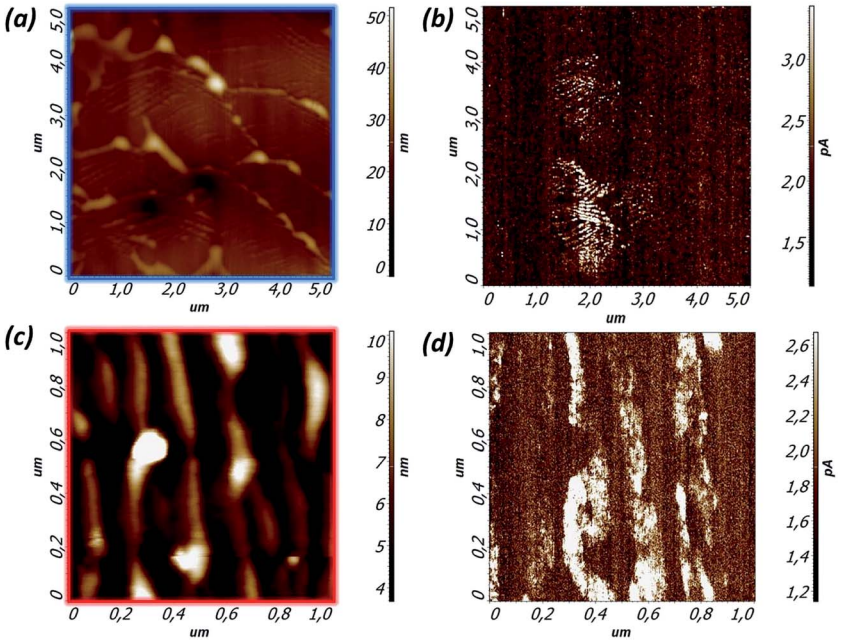

Fig. 5 (a, c) Surface topography and (b, d) spreading resistance scan images for terrace-ledge domains embedded into the mesh type morphology area of CCTO sample. The scanning was done at 0.1 Hz (512 × 512 pixels) and dc bias voltage of 1 V.

intensity and conductivity type. The current measurements on conductive barriers within the terrace-ledge 1 domain reveal a typical semiconductor *I*–*V* dependence (which is partly influenced by the Schottky contact) with the threshold voltage of 1 V and −2 V and the saturation voltage of around ±8 V (Fig. 6(c)). The *I*–*V* measurements performed on the insulating gap revealed a low current value of about 8 pA, when a 10 V dc bias voltage was applied (inset in Fig. 6(c)). On the contrary, the current–voltage measurements carried out on the terrace-ledge 2 domain structure embedded into the mesh type morphology area demonstrate another type of *I*–*V* curve. For this current–voltage dependence we assume that the conductivity behavior

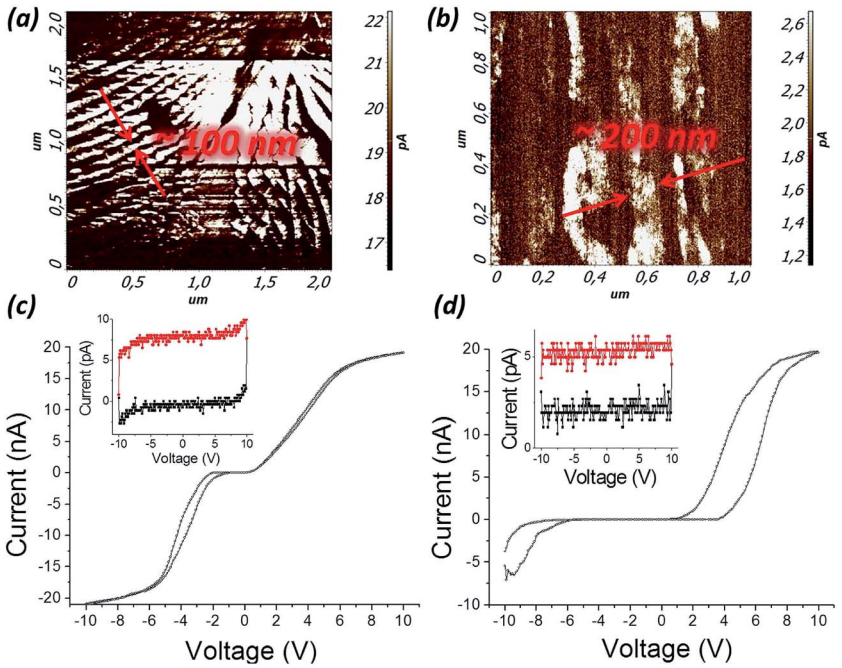

Fig. 6 Spreading resistance scan images for (a) terrace-ledge 1 and (b) terrace-ledge 2 domains of CCTO sample. Current–voltage dependences obtained on conductive part of (c) terrace-ledge 1 and (d) terrace-ledge 2 domains of CCTO sample. Inserts show the *I*–*V* measurements performed on insulating parts.

should be affected by both the Schottky and n-type semiconductor mechanisms. The n-type conductivity behavior was, for the first time, described in ref. 22, reporting on a clear n-type nature of the CCTO grains and ref. 23, suggesting that the majority of charge carriers in the explored area are electrons and that the main mechanism of conductivity is electron hopping. Thus, n-type conductivity behaviour with the threshold voltage of 2 V and −7 V and the saturation voltage exceeding ±10 V was detected (Fig. 6(d)). The hysteresis in the current–voltage curves is linked with the diode-like rectifying *I–V* characteristic, indicating a forward pass diode behaviour and a reverse diode behaviour for a backward sweep (similar to that observed in the ref. 24). It can be seen that during the measuring cycle the diode polarity can be switched in the range of 4–6 V. The *I–V* curve measurements for insulating gap found a low current value of about 6 pA when a 10 V dc bias voltage was applied (insert at Fig. 6(d)). Thus, we claim that the mechanism of conductivity inside the CCTO grains could be successfully described in the framework of NBLC model, but the coexistence of different-type morphology areas with the dissimilar conductivity behaviour should be taken into account.

It is worth to emphasize that the average MBLC and NBLC gap widths in the CCTO ceramics reach 5 μm and 200 nm, respectively. These are approximately 170 and 7 times larger than the Pt/Ir-coated tip apex (∼30 nm) (Fig. 4-ESI†). Moreover, not all terrace-ledge domains demonstrate a correlation between the topography and SR signal (see the cross-sections in Fig. 5-ESI†). Taking into account the small topography roughness as well as the scanning parameters described above (*i.e.* the large setpoint, high cantilever stiffness and low scanning rate) we consider that we maintain a permanent tight tip-surface contact during the scanning. Accordingly, we believe that our measurements adequately reflect the MBLC and NLBC mechanisms proposed. In order to confirm the origin of the SR signal and exclude the possibility that the observed effects are solely determined by the reduction in contact area at step edges, we repeated the experiments at different scan directions (Fig. 6-ESI†).

Our research is based on the phenomenology considering that the observed CDC behavior in CCTO material requires the coexistence of conductive barriers and insulating gaps caused by the twin boundaries, planar defects and slip planes within the crystallographic structure of the sample. In general, this approach has been initially proposed in ref. 9 and significantly developed in ref. 10 and 11 to yield the structural model for planar defects. Following this model, the ideal arrangement of a perfect crystal of CCTO, where the CuO_4 square planes containing Cu^{2+} ions share corners with the TiO_6 octahedra containing Ti^{4+} ions, could be disrupted as a result of twinning in a CCTO crystal.[10–12] This disturbance may create the plane defects and make the Cu and Ti environments conductive by accommodating Cu^{+} and Ti^{3+} ions. Simultaneously, it creates the insulating barrier because of the associated charge balance which requires the existence of oxygen vacancies in the defect plane.[10] Accordingly, we consider that the observed terrace-ledge 1 domain structure is originated from the twinning or slip planes against the [100] direction along the (220) plane, which is fully consistent with the previous reports.[10–15] This sliding motion of one atomic plane by half unit cell – a stacking fault – can explain the dielectric and semiconducting properties of polycrystalline CCTO sample. Indeed, the main conductivity mechanism along the stacking fault ((220) plane) is an electron transfer between TiO_5 cluster and Cu^{2+}-containing adjacent structure.[10–12]

Another scenario is likely realized for the mesh type morphology areas, in which the terrace-ledge domains have increased barriers width and exhibit the change in the conductivity behavior. In accordance with the theoretical predictions given in ref. 10, one of the possible mechanisms for the observed phenomena could be the stacking faults that come from a twinning or slip planes against the [100] direction along the {110} planes. This consideration is generally consistent with the assumption of oxygen vacancies increasing in order to reach higher stability in group of four adjacent TiO_5 square pyramids that become connected to the four O atoms of a CuO_4 square plane to form four slightly distorted TiO_6 octahedra.[10] Therefore, the local charge neutrality would be kept by the reduction of Cu^{2+} to Cu^{1+} and the formation of oxygen vacancies. This kind of stacking fault makes the electron hopping to be the main mechanism of conductivity in such distorted structure.[12,22,23] Finally, this results in n-type conductivity.

Taking into consideration the results obtained, we can construct a principle scheme explaining the conductivity behavior in polycrystalline CCTO sample (Fig. 7 (a); the spreading resistance mode is known as a surface technique (the current flows between the SPM probe and the clamping contact located on a sample surface), so only the surface current distribution was measured). This scheme represents the main mechanisms involved in CDC behavior of CCTO. Those are microscale barrier layer capacitance (MBLC) mechanism, which depends on potential grain-to-grain barriers, and nanoscale barrier layer capacitance (NBLC) mechanism, which depends on potential barriers that are created by structural defects such as twinning or slip planes. We believe that NBLC mechanism is associated with the existence of a number of intertwined domain structures which causes the alternation of conductive and insulating parts. The number of distinct intertwined domain structures should be dependent on possible disruption plane combination. It has been predicted that there should be several possibilities for plane defect along {110} planes resulting from a twinning parallel to the (100), (010), and (001) planes.[10–12] In the current work we found two of them distinguished by the conductivity type.

In accordance with the mechanisms proposed, we are able to construct a principle local electric scheme for the CCTO sample (Fig. 7(c)), where the MBLC is defined uniquely (see Fig. 3(c and d)) and the NBLC consists of two components associated with terrace-ledge 1 (Fig. 6(a)) and terrace-ledge 2 (Fig. 6(b)) domains. The calculated from the *I–V* curve values for the MBLC and NBLC-related impedance ($Z_{MBLC} \sim 10$ GΩ, $Z_{NBLC1} \sim 40$ GΩ and $Z_{NBLC2} \sim 250$ GΩ) demonstrate that the global impedance $Z = (Z_{MBLC} + Z_{NBLC1} + Z_{NBLC2}) \times S$ normalized on the scan area factor ($S \sim 10^{-6}$) is about 0.3 MΩ. This value is consistent with macroscopic complex impedance data presented in Fig. 7(b). Consequently, this result shows that the impedance is mainly determined by the NBLC mechanism of conductivity.

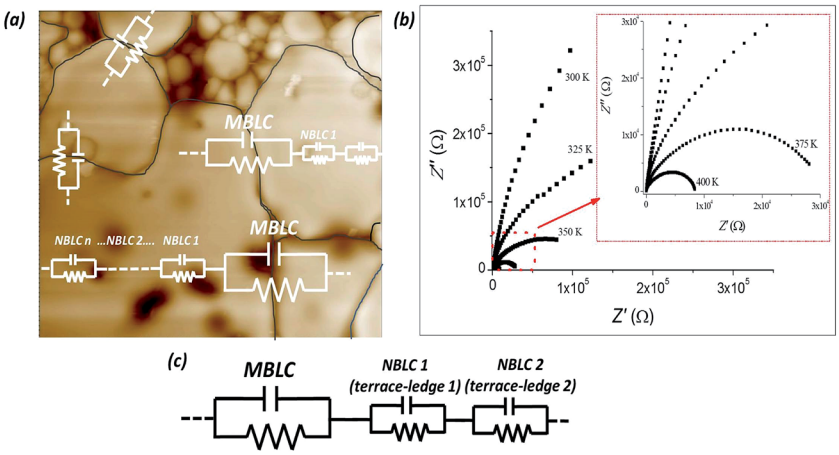

Fig. 7 The principle scheme for (a) general case and (c) measured polycrystalline CCTO sample. (b) The real and imaginary impedance spectra.

Conclusions

To sum up, we proposed the direct experimental evidence for MBLC mechanism attributable to potential grain-to-grain barriers and NBLC mechanism associated with potential barriers created by structural defects such as twinning or slip planes. The SPM study allowed two distinct types of surface morphology related to the NBLC mechanism of conductivity to be discovered. These terrace-ledge 1 and terrace-ledge 2 domains have obvious structural difference underlying the change in the conductivity mechanism from electron transfer to electron hopping. We believe that results obtained contribute to general understanding of anomalous CDC behavior in CCTO and related materials.

Conflicts of interest

There are no conflicts of interest to declare.

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