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Growth of single-crystalline cubic structured tin(II) sulfide (SnS) nanowires by chemical vapor deposition†

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Single crystalline tin(II) sulfide (SnS) nanowires are synthesized using a chemical vapor deposition (CVD) method with the support of gold as catalyst. Field emission electron microscopy studies show that SnS nanostructures grown at temperatures between 600 and 700 °C have wire-like morphology. These nanowires have an average diameter between 12 and 15 nm with lengths up to several microns. These NWs consist of uniform and smooth surfaces, and exhibit nearly stoichiometric chemical composition (Sn/S = 1.13). Transmission electron microscopy analysis reveals that the NWs consist of single crystalline cubic crystal structure with a preferential growth direction of ⟨100⟩. Field-effect transistor devices fabricated with SnS nanowires show that the nanowires consist of p-type conductivity along with carrier density of 6×10^{18} cm^{-3}.

Introduction

One-dimensional (1D) nanostructures of semiconductor materials have received great attention in the development of various prototype devices due to their distinct properties.[1–6] As compared to their bulk counterparts, semiconductor nanostructures exhibit high surface-to-volume ratio, and unique electrical and optical properties. In this regard, tin(II) sulfide (SnS), IV–VI group compound semiconductor, has received considerable attention due to its favorable chemical and physical properties. In general, SnS exhibits a direct optical band gap of 1.35 eV and p-type electrical conductivity. It is a double-layer structured compound, and usually crystallizes in the form of orthorhombic structure with lattice parameters $a = 0.433$, $b =$ 1.119, and $c = 0.398$ nm. The electrical and optical properties of SnS can be easily tailored by doping with appropriate dopants.[7–10] It exhibits stable structural and optical properties, even at low temperatures.[11] Further, the constituent elements of SnS are abundant in nature, and do not pose any health or environmental hazards. Based on the optical band gap, the possible light conversion efficiency of SnS-based devices is about 25%.[12] These interesting properties make SnS a suitable candidate for the development of various electrical and optoelectronic devices.[13]

Over the past couple of years, the synthesis of nanostructures with specific morphologies and crystal structures has been of great concern, since the optical and electrical properties of materials strongly depend on their shape and size, as well as structure.[14] Thus, the ability to tune the physical properties of SnS at nanoscale probably leads its applications to diverging fields. In this regard, different types of SnS nanostructures, including nanoflakes, nanowires,[15] nanorods,[16–20] nanobelts,[21] nanoflowers,[22] nanoparticles,[23–25] nanoboxes,[26,27] and nanosheets[28,29] have been realized, using various synthetic methods. Noticeably, most of the realized SnS nanostructures consist of orthorhombic crystal structure. However, Greyson *et al.* have synthesized zinc blende ($a = b = c = 0.585$ nm) structured SnS nano- and micro-crystals using thermal decomposition of tine chloride and sulfur powder.[30] Further, as compared to usual orthorhombic SnS nanostructures, these zinc blende structured SnS nanocrystals exhibit quite different optical properties.

On the other hand, at higher temperatures, SnS exhibits a phase transition from orthorhombic to tetragonal, and its lattice parameters a and c equal 0.423, and $b = 1.151$ nm,

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respectively. In our recent investigations on the development of nanocrystalline SnS structures by a thermal evaporation technique, we noticed that SnS also exhibits a transition from orthorhombic to tetragonal phase at a growth temperature of 410 °C, which is treated as a phase transition temperature.[31] At this temperature, the lattice parameters of tetragonal SnS are evaluated ($a = c$) as 0.42 and $b = 1.13$ nm, respectively, and its Sn to S atomic percent ratio is found to be ~1.2.

In this direction, by keeping all these issues in mind, we have initiated the synthesis of SnS nanowires by chemical vapor deposition (CVD) using gold (Au) as metal catalyst under the well-established vapor–liquid–solid (VLS) process, and have explored their physical and chemical properties. The SnS nanostructures grown under optimized conditions are highly dense, long, and have uniform surface morphology and excellent chemical stoichiometry. In this paper, we report the methodology for the growth of SnS nanostructures on two different substrates, and the optimized growth conditions for uniform single crystalline SnS nanowires. Furthermore, a plausible growth mechanism is also reported and discussed.

Experimental procedure

Materials and chemicals

(100) n-type silicon (Si, $\rho = 0.005$ Ω cm) substrate, (001) sapphire substrate (c-plane). Sulfur-rich SnS powder (Sn/S atomic% ratio of 0.95) synthesized by following the procedure reported elsewhere[32] and gold (99.99) was purchased from Sigma-Aldrich.

Growth of SnS nanostructures

SnS nanostructures were synthesized in a homebuilt chemical vapor deposition (CVD) system. Fig. SI1 in the ESI† shows a schematic of the procedure. A fine power of SnS was taken in a ceramic boat, and placed 5 cm away from the center of the tube. Cleaned (100) n-type Si and (001) sapphire substrates coated with gold (5 nm) (see SI2†) were placed at the center of the tube under downstream direction of the carrier gas. Then, the CVD system was initially evacuated to base pressure of 4×10^{-2} Torr, and then purged with argon gas with the flow rate of 100 sccm (standard cubic centimeter per minute) for three times. The system was then heated to a fixed temperature. In the present work, the growth was carried out at different temperatures varying from 500 to 950 °C. The growth time and operating pressure of the system were kept constant at 10 min and 20 Torr, respectively. After successful completion of the process, the system was allowed cool-down to room temperature.

Fabrication of FET devices

Field-effect transistor devices were fabricated on Si/SiO$_2$ substrates (2×2 cm^2) by photolithography. Here, highly doped p-type Si substrates ($\rho = 5 \times 10^{-3}$ Ω cm) with thermally grown 100 nm thick SiO$_2$ layer were used as gate electrodes. Initially, SnS nanowires were detached from substrates by sonication into ethanol solvent, and they were dispersed on Si/SiO$_2$ substrates. Photoresists were deposited by spin-coating, and dried on hot-plate at pre-optimized temperatures. Patterns were developed by exposing the samples to light under mask, and followed by a lift-off process. Bilayer contacts (Ti/Au) were deposited by e-beam evaporation with a thickness of ~100/50 nm, and then the lift-off process was carried out.

Characterization

Field emission scanning electron microscopy (FESEM) was used to examine the surface morphology. Energy dispersive X-ray spectroscopy (EDS) embedded with FESEM was adopted to estimate the chemical composition of the as-synthesized structures. High resolution FESEM images have been analyzed by ImageJ 1.43u (Wayne Rasband, National Institutes of Health, USA; http://rsb.info.nih.gov/ij). Transmission electron microscopy (TEM), high-resolution TEM (HRTEM) and selected area electron diffraction (SAED) were used to confirm the crystallographic properties. Finally, the electrical characteristics of SnS nanowires were investigated by studying the FET devices using probe station (with four-probe configuration) attached with semiconductor parameter analyzer.

Results and discussion

The product grown on both substrates at all temperatures appears silver gray in color, which is very similar to the color of SnS source powder. FESEM images of SnS nanostructures grown at 500 °C (Fig. SI3(a) and (b)†) consist of button-mushroom like crystals (some of them have spherical shaped bright particles as heads). After increase of the growth temperature from 500 to 550 °C, the button-mushroom shaped crystals are slightly elongated, and look like NWs (Fig. SI3(c) and (d)†). These nanowires consist of gold particle as head. The average length of the nanowires grown on both the substrates is about 200 nm; however, the diameter of nanowires grown on Si substrate is slightly different than that of the nanowires on sapphire substrate. Noticeably, the diameter of the nanowires on both the substrates is clearly lower than the diameter of gold particles, as can be clearly seen from the insets of (Fig. SI3(c) and (d)†). For example, the average diameter of SnS nanowires grown at 550 °C is about 17 (19 in case of Si) nm, and their corresponding Au nanoparticles average diameter is 22 nm.

FESEM images of SnS nanowires grown at 600 °C (Fig. SI3(e) and (f)†) reveal that the structures grown at 600 °C consist of different morphologies, including nanowires, nanorods, helices, and aggregated balls with different dimensions (shown in Fig. SI4(a)†). As compared to the structures grown at 550 °C, these structures consist of a greater number of NWs, which have the length of 2–4 times that of a micron (see SI4(b)†). FESEM images of SnS nanostructures grown on sapphire and Si substrates at 650 °C are shown in Fig. 1. It reveals that the as-grown structures consist of lengthy nanowires, which have uniform and smooth surface morphology. The growth of nanostructures on both the substrates is freestanding and denser. Note that these nanowires consist of high aspect ratio, since the average diameter of the nanowires vary between 13 and 14 nm, which depends on nature of Au crystallites size over substrates (as can be seen from the insets of Fig. 1(a) and (b)),
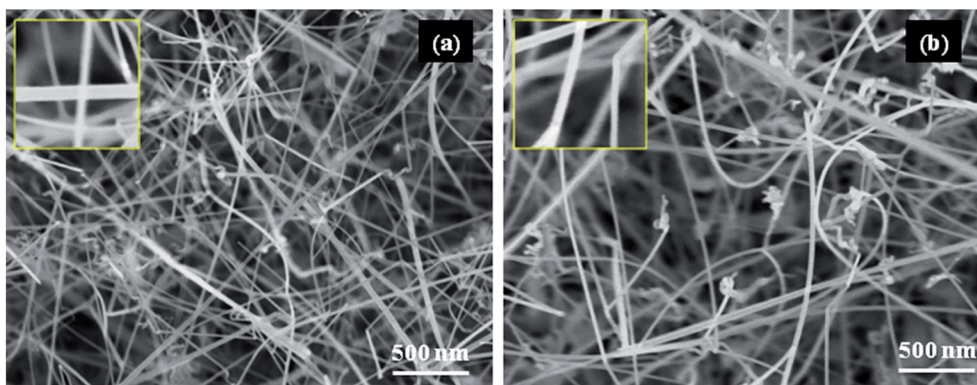
Fig. 1 FESEM images of SnS nanostructures grown at the growth temperature of 650 °C on (a) sapphire and (b) Si substrates, respectively.

and their lengths are up to several microns (see SI5†). Yue *et al.* have realized similar SnS nanostructures at 800 °C growth temperature using SnS + S powders as precursors by gold nanoparticles assisted chemical vapor deposition on ITO substrates under the flow of Ar + H_2 gases.[15] Similar to present work, Ga_2S_3 nanowires have been realized in ambient pressure CVD system by using Ga metal and H_2S (∼400 sccm) as sources of Ga and S at growth temperatures of 650–800 °C.[33] On the other hand, Wu *et al.* developed led sulfide nanowires on several metal thin films coated substrates using $PbCl_2$ and S as precursors for Pb and S at growth temperatures varied between 600 and 650 °C.[34]

With further increase of growth temperature from 650 to 950 °C, the morphology of SnS nanostructures becomes trivial, and their growth on both the substrates gradually reduced. It can be seen in Fig. SI6,† which presents FESEM images of SnS nanostructures grown at 700, 800, and 950 °C. On the other hand, the structures grown at above 700 °C showed tapering on the surface of nanowires, which could be due to uncatalyzed growth of SnS over the sidewalls of nanowires. In this region, the length of nanowires also gradually decreases with the increase of growth temperature, whereas their diameters increase. To explore the impact of growth temperature on the diameter of SnS nanowires, the nanowires' diameters were extracted by analyzing FESEM images (recorded at 60k magnification) with ImageJ software.[35,36]

Variation of average diameter (AD, see SI7†) of SnS nanowires, grown on sapphire (SA) and silicon (Si) substrates, as function of growth temperature (GT) along with its demonstrative FESEM images is shown in Fig. 2. It clearly reveals that at all growth temperatures, the nanowires grown on Si substrates have slightly larger diameters than that of nanowires on SA substrates, which is probably attributed to the size of Au grains (or crystals) on different substrates (see SI2†).[37] The nanowires grown at the growth temperature of 550 °C consist of an average diameter of 17 nm (19 nm in case of Si). With the increase of growth temperature from 550 to 650 °C, AD of nanowires gradually decreases and reaches a low value of 13 (14) nm at 650 °C, which is highlighted with a green line in Fig. 2a. Above this temperature, AD increases exponentially with increasing growth temperature. As discussed in the literature about the growth of nanostructures by CVD technique, the variation in diameter of nanowires strongly attributed to growth kinetics of nanostructures.[38] It reveals that the growth rate along the axial direction of SnS could be high at around 650 °C due to lower nucleation barrier on the top facet of nanowires than the vertical sidewalls. This greatly lengthens the nanowires much faster along their axial direction.[39] However, above this temperature, the increase in diameter of nanowires attributed to the competing growth on the sidewalls (radial) of nanowires through uncatalyzed deposition.[37] Similar changes in the
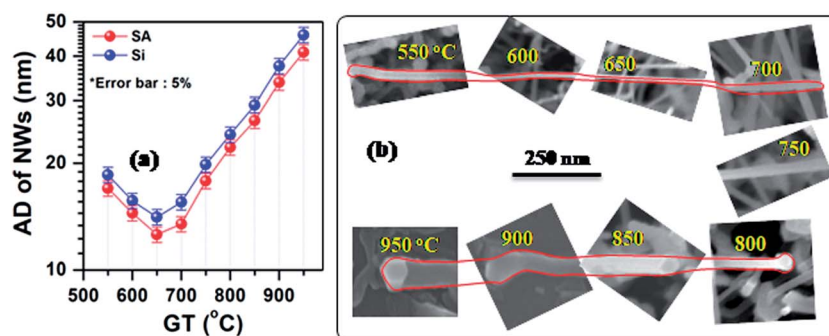

Fig. 2 (a) Variation of average diameter (AD) of SnS nanowires, grown on sapphire (SA) and silicon (Si) substrates, as a function of growth temperature (GT) (hint: error bar represents error in percent of data) and (b) its pictorial representation by selected portion of FESEM images of SnS nanowires grown on Si substrates.

diameter of InAs nanowires, grown by metal–organic CVD system, have been observed by Li *et al.*[40]

The SnS structures grown on Si substrates at a growth temperature of 650 °C consist of smooth, long, and denser nanowires, and have an average diameter of 14 nm. These unique nanostructures, therefore, have been chosen for further studies.

Chemical composition analysis by EDS (see SI8†) reveals that the as-grown SnS nanowires consist of ~53 atomic% of Sn and 47 atomic% of S, and the Sn/S atomic% ratio is found to be 1.13. This indicates that the as-grown SnS nanowires have nearly stoichiometric chemical composition between the constituents. XRD profile of SnS nanowires grown at 650 °C is shown in Fig. 3(a). This indicates that SnS nanowires consist of a predominant peak at 32.86° along with a several minor peaks diffracted at different angles. All the diffraction peaks are indexed to cubic and orthorhombic structured SnS (PDF # 892755 and 831758). It implies that the as-grown SnS nanowires at 650 °C not contain any other Sn–S phases like SnS_2 and Sn_2S_3. As presented in Fig. 3(a), first, second, fourth, and seventh peaks belong to orthorhombic SnS, whereas the dominant peak along with third peak belongs to cubic structured SnS. Presence of a sharp and narrow (200) peak clearly indicates that the as-grown nanowires are highly crystalline in quality and grown along (100) planes of cubic structured SnS. Presence of minor

diffraction peaks of orthorhombic SnS probably arose either from orthorhombic structured SnS thin film or nanowires, which could be developed along with cubic structured SnS nanowires. Nearly similar to our results, Seo *et al.* have observed cubic as well as hexagonal crystal structures in zinc selenide (ZnSe) nanowires grown by chemical vapor deposition on gold nanoparticles dispersed ITO substrates.[41]

The Raman spectrum of SnS nanowires grown at 650 °C, shown in Fig. 3(b), exhibits three distinguishable peaks, which are assigned to three different single-phonon oriented longitudinal optical (LO) vibrational modes, *i.e.* $B_{2g}(LO)$, $A_g(LO_1)$ and $A_g(LO_2)$.[42] As compared to the Raman spectra of SnS thin films[31,42] or orthorhombic nanostructures,[15,43,44] the cubic structured SnS nanowires peculiarly consist of $A_g(LO_2)$ peak as sharp and dominant, which is probably attributed the preferential growth of structures. This clearly reveals that the as-grown SnS nanowires consist of pure single phase.

Fig. 4 shows TEM, HRTEM, and SAED images of SnS nanowires grown on Si substrate at 650 °C. Fig. 4(a) reveals that the as-grown SnS nanowires consist of low diameter of about 18 nm, and are uniform along their length. The results are consistent with the FESEM data. Fig. 4(b) shows HRTEM image of SnS nanowire. The lattice fringes of SnS nanowire in all the directions are very clear and periodic, which indicate the as-grown SnS nanowires are single crystalline crystallites, and
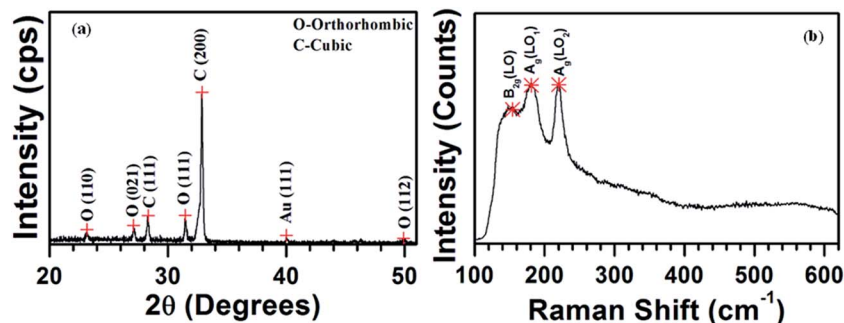

Fig. 3 (a) XRD pattern and (b) Raman spectrum of SnS nanowires grown on Si substrate at the growth temperature of 650 °C.
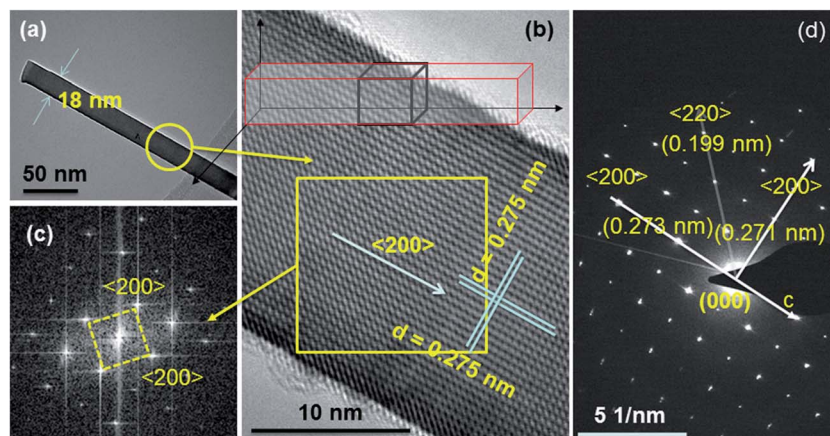

Fig. 4 (a) TEM, (b) HRTEM (inset shows the schematic representation of SnS nanowires growth), (c) FFT taken on HRTEM, and (d) SAED images of SnS nanowires grown on Si substrate at the growth temperature of 650 °C.

have very good crystalline quality. The estimated d-spacing values from two-dimensional fast Fourier transformation (FFT) analysis on HRTEM image (Fig. 4(c)) is ~0.275 nm, which corresponds to the (200) planes of cubic SnS (face-centered cubic, space group: $F\bar{4}3m$, PDF #892755). This reveals that the growth direction of SnS nanowires is parallel to the axis of the (100) planes. The cell parameter(s), calculated using the standard equation for cubic lattices (see SI9†), is found to be $a = b = c = 0.55$ nm, which exactly matches the standard cubic structured SnS data (PDF #892755).

Fig. 4(d) shows SAED image recorded on SnS nanowires at lower magnification TEM object, and the diffraction spots can be indexed to the face-centered cubic (fcc)-type SnS with a lattice constant of 0.55 nm. The presence of regular diffraction spots clearly confirms that the as-grown SnS nanowires are single crystalline cubic crystals, and have growth direction along the (100) planes. The possible reason(s) for the ordered structure in SnS nanowires could be related to anisotropic growth or the presence of periodic vacancies in certain crystallographic sites, as suggested in the development of 3D tungsten oxide nanowires by Zhou et al.[45] These HRTEM and SAED results clearly confirm that the as-grown SnS nanowires have purely cubic crystal structure, and however, the observed orthorhombic structured SnS phase undoubtedly belongs to thin films of SnS. On the other hand, as per the literature data, the preferential crystal growth of SnS nanowires is orthorhombic,[46–48] however, in the present case, SnS nanowires grown by using sulfur rich SnS powders consist of cubic crystal structure. This could be attributed to precursor adopted for the growth of nanostructures.[49] For example, zinc sulfide (ZnS) nanowires developed using Zn powder as precursor adopt hexagonal structure as preferred structure, whereas nanowires adopt cubic structure as preferred structure when zinc chloride ($ZnCl_2$) is used as precursor.[50,51]

XPS spectrum of SnS nanowires grown at 650 °C is shown in Fig. 5. Initially, a survey scan was recorded and corrected for specimen charging through referencing C 1s to 248.6 eV (see SI10†). Fig. 5(a) shows two distinguishable peaks at the binding energies of 487 and 495.5 eV, which are assigned to Sn $3d_{5/2}$ and $3d_{3/2}$ spin-orbital components of SnS. A sharp peak noticed at

the binding energy of 161.5 eV, Fig. 5(b), belongs to S $2p_{3/2}$ spin-orbital component of SnS. These results also indicate that the as-grown nanowires consist of pure single SnS phase.

Fig. 6(a) shows the schematic diagram of SnS nanowire FET device, and its typical FESEM image is shown in Fig. 6(b). Current flow through the device (I_{ds}) as a function of applied bias voltage (V_{ds}) measured at different gate voltages (V_g) is shown in Fig. 6(c). It clearly shows that the current flow through the device increases with the decrease of gate voltage from 0 to −5 V, which reflects the well-known gating effect of the p-type semiconductor. Further, as shown in inset of Fig. 6(c), the variation of device current as a function of gate bias voltage (I_{ds} vs. V_g) at a constant V_{ds} of 2.5 V reveals that the SnS nanowires based FET devices consist of an on/off ratio about 10^3 and a threshold (V_{th}) voltage of 2.3 V. It implies that the as-grown FET device belongs to depletion mode.

In order to explore the electrical properties of SnS nanowires, we have calculated the carrier concentration (n), field effect mobility (μ), and resistivity (ρ) of the nanowires by using the equations described below.[52] The electron concentration (n) of nanowire structures is calculated from the threshold voltage (V_{th}) of the device by using eqn (1):

$$n = \frac{CV_{th}}{\pi e L r^2}. \qquad (1)$$

Where C is the gate capacitance of the nanowire, V_{th} is the threshold voltage of the device at $I_{ds} \sim 0$, e is the charge of the electron, L is the device channel length, and r is the radius of the nanowire. The gate capacitance of the nanowire was estimated by using the equation (eqn (2)) derived from a cylinder on an infinite metal plate model:[53]

$$C = \frac{2\pi\varepsilon\varepsilon_o L}{\ln\left(\frac{2t}{r}\right)}, \qquad (2)$$

where ε is the relative dielectric constant of SiO_2 gate, ε_o is the permittivity of free space, and t is the thickness of SiO_2 layer. In addition, the field effect electron mobility (μ_e) and resistivity of the nanowire(s) are evaluated using eqn (3) and (4), respectively.[54]
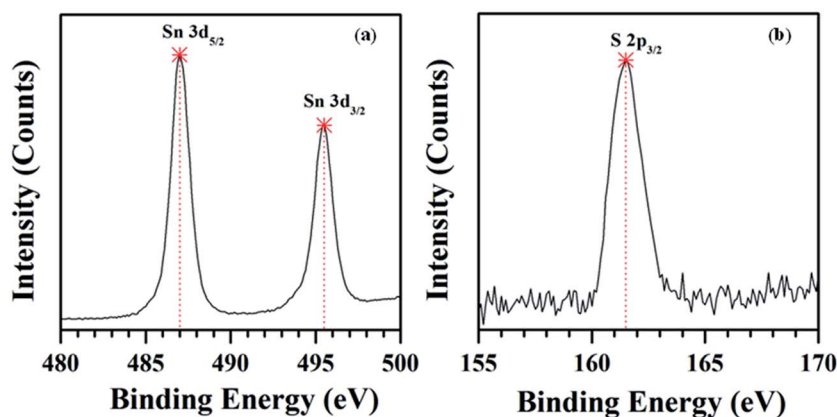

Fig. 5 XPS spectra of SnS nanowires grown on Si substrate at the growth temperature of 650 °C: (a) Sn and (b) S elements.
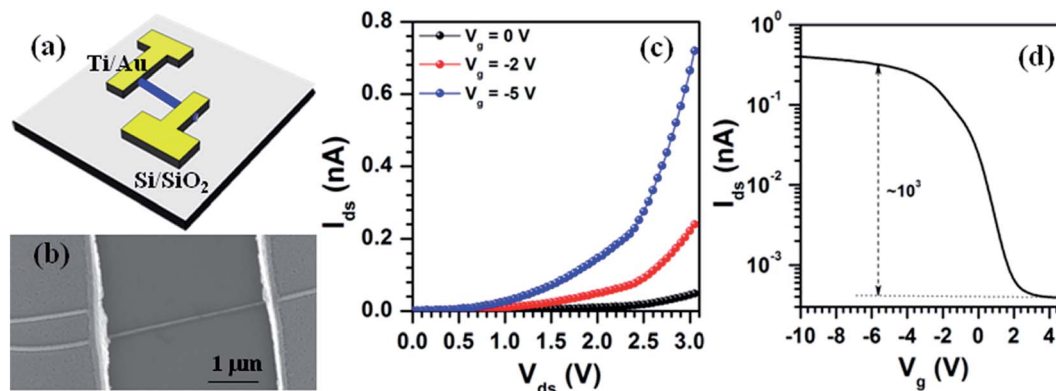
Fig. 6 (a) Schematic diagram and (b) FESEM image of SnS nanowire FET device, (c) I_{ds} versus V_{ds} plots measured at different V_g values, and (d) variation of I_{ds} as a function of V_g at a constant V_{ds} of 2.5 V.

$$\mu_e = \frac{g_m L}{2\pi\varepsilon\varepsilon_o V_{ds} / \ln\left(\frac{2t}{r}\right)} \quad \because \ g_m = \frac{dI_{ds}}{dV_g}, \tag{3}$$

and

$$\rho = 1/en\mu_e. \tag{4}$$

Here, we considered V_{th} at $V_g = 0$ is 2.3 V, L is 2.5 μm, r of SnS nanowire is 7 nm, ε of SiO$_2$ is ~3.9, ε_o is 8.85×10^{-12} F m^{-1}, and t of SiO$_2$ layer is 100 nm. From these calculations, the carrier density, mobility, and resistivity of SnS nanowires are found to be 6.03×10^{18} cm^{-3}, 1.47×10^{-2} cm^2 V^{-1} s^{-1}, and 70.1 Ω cm, respectively. These values are quite different than that of electrical properties of ultrathin SnS films obtained from the Hall-effect measurements,[55] which is probably attributed to phonon scattering and surface roughness of the nanostructures.[56]

Growth mechanism

In the present study, SnS nanostructures have been realized using gold as catalyst and SnS powder as source. Further, the overall experimental results show that nanostructures grown on either Si or sapphire substrates consist of gold particle as tip, and their diameters are smaller than the diameter of gold particles. These nanowires are single crystalline crystallites, and have a preferential growth direction along the (100) planes. On the other hand, the growth of SnS nanowires is completely independent of the substrate material, since the changes in morphology, density, or the crystal-structure of SnS nanowires grown on sapphire or Si substrates are marginal. Therefore, the plausible growth mechanism of SnS nanowires could be a vapor–liquid–solid (VLS) process, which is schematically represented in **Fig. 7**. Similar concept has been applied for explaining the growth of gallium arsenide (GaAs) nanowires under VLS growth process.[57] As per the Wagner and Ellis demonstration, Au catalyst forms a liquid-alloy particle (eutectic formation) upon chemically reacting with source material supplied in the form of vapor.[58] For continuous supply of the source, at above the saturation, the material gets precipitate as solid nanowire at the bottom of the particle, which is schematically represented in Fig. 7(a).

Au deposited substrates consist of granular surface morphology, which uniformly covers the entire substrate (first
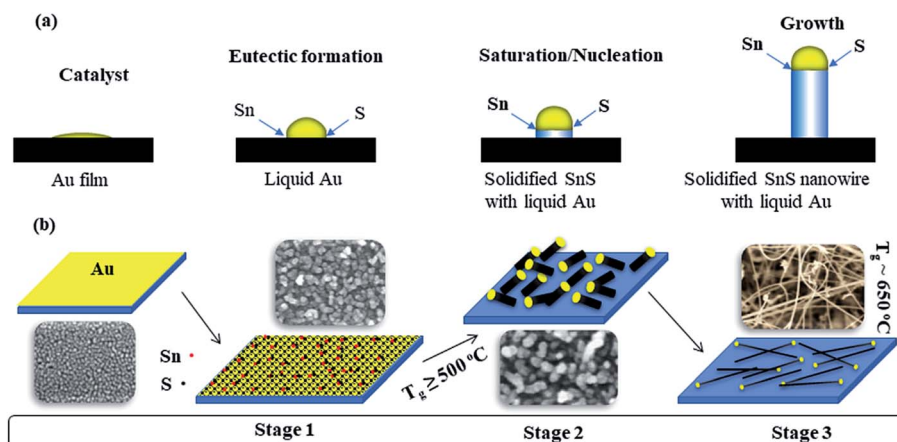

Fig. 7 Schematic representation of (a) various steps in VLS growth of SnS nanowires, and (b) SnS nanowires growth at different temperatures: (stage 1) Nucleation of vaporized Sn and S atoms, (stage 2) nano features having Au NP as tip, and (stage 3) growth of long nanowires.

image in Fig. 7(b)). When the growth temperature was carried out at 500 °C, the formation of SnS–Au structures is observed (@stage 1). It indicates that upon heating, the source SnS powder decomposes as Sn and S, and travels along the tube as a vapor with carrier gas. At above 450 °C, the SnS–Au structures become droplets and act as energetically favored centers for adsorption of Sn and S vapors, since we have noticed flakey films growth over substrates at a growth temperature of 450 °C (see SI11†). The Sn and S vapors accumulate around SnS–Au droplets and forms stable SnS phase *via* the vapor–liquid–solid (VLS) mechanism when it reaches the supersaturation concentration. Formation of typical SnS crystallites is observed particularly at the growth temperature of 500 °C, Fig. SI3(a) & (b),† (@stage 1). With increase of density of SnS nuclei, SnS crystallizes along its preferential direction, and pushes the gold droplet at above the growth temperature of 500 °C, Fig. SI3(c) & (d),† (@stage 2). Upon increasing the growth temperature, the SnS forms as nanowires, Fig. SI3(e) & (f),† (@stage 3). On the other hand, the presence of atoms on the surface of nanofragments (*i.e.* button-mushroom shaped crystals) induces compressive stress, and leads to increase in length.[59–61] This could be the reason for the growth of longer nanowires under eutectic temperature of SnS and Au. Finally, under an optimum growth temperature (∼650 °C), the formation of ultralong SnS nanowires with uniform morphology is taken place.

Conclusions

The growth of SnS nanostructures was performed on gold catalyst coated sapphire and Si substrates by a chemical vapor deposition at different temperatures varying from 500 to 950 °C. Freestanding high-density SnS nanowires are found at the growth temperature of around 650 °C, which have smooth and uniform surface morphology with thinnest diameter of 13 nm (14 nm in case of Si). These SnS nanowires are single crystalline, and have preferential growth direction along the (100) planes. These structures also consist of nearly stoichiometric chemical composition of its constituents (*i.e.* the Sn/S atomic% ratio is about 1.13). These interesting results emphasize that the reported methodology for the growth of high quality 1D SnS nanowires allow us to develop various efficient and sustainable SnS based devices, including batteries, solar cells, and field emission devices.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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