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Electrode buffer layers producing high performance nonvolatile organic write-once-read-many-times memory devices

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CuI and Bphen are adopted as the electrode buffer layers for a PbPc/F_{16}CuPc heterojunction based nonvolatile organic write-once-read-many-times memory device, which improve the ON/OFF ratio up to one order of magnitude while significantly reducing the threshold voltage compared to the non-buffer-layer counterpart.

Organic resistive memory devices have attracted a lot of attention due to their simple device structure, good scalability, low-cost, low-power consumption, large data storage capacity, and high cycling endurance.[1–5] Depending on their memory characteristics, organic memory devices can be simply classified into three types: random access memory, read-write-erase-rewritable memory, and write-once-read-many-times (WORM) memory. Among these memory devices, WORM memory is an important type of nonvolatile memory which can hold data permanently and be read from repeatedly. WORM memory devices have been extensively investigated due to their potential applications for wireless identification tags, smart cards, and personal data depositories. A typical organic resistive memory device usually has a sandwich structure where the switchable organic material is inserted between two electrodes. Organic switchable materials used for these devices range from small molecular materials to polymers and organic/inorganic composites. Correspondingly, a lot of mechanisms have been proposed to account for the transition between the high conductivity (ON) and low conductivity (OFF) states, for example, charge carrier trapping and detrapping,[6–8] filament formation and destruction,[9,10] conformation change,[11] oxidation/reduction reaction,[12,13] and charge-transfer complex formation.[14,15]

Recently, Wang *et al.* have demonstrated that the interfacial dipole layer in an indium tin oxide (ITO)/hexadecafluoro-copper-phthalocyanine (F_{16}CuPc) interface and copper phthalocyanine (CuPc)/F_{16}CuPc interfaces can control the conductivity state of WORM memory devices.[16,17] Meanwhile, a high ON/OFF current ratio in the order of 10^4 is achieved in the CuPc/F_{16}CuPc heterojunction based device.[17] However, the switch threshold voltage of this device is about −8 V. Such a high switch threshold voltage is not economical from the energy consumption point of view. Lead phthalocyanine (PbPc) is a member of the metal phthalocyanine family with the similar chemical and physical stability to CuPc, and it has been applied for organic solar cells[18–20] and photodetectors.[21–23] On the other hand, electrode buffer layer has been widely adopted in organic electronic devices, such as organic light-emitting diodes and organic solar cells.[24] The introduction of buffer layer can alter the energy level alignment, material growth pattern, and chemical reaction in the interface. Improved performance has been demonstrated in organic light-emitting diodes and organic solar cells by using suitable electrode buffer layer. However, such a strategy has not been exploited in organic memory devices.

In this work, nonvolatile organic WORM memory devices based on PbPc/F_{16}CuPc heterojunction has been demonstrated. The PbPc/F_{16}CuPc bilayer heterojunction WORM memory device shows a high switch threshold voltage of −4.4 V and a low ON/OFF current ratio of 10^3. However, by inserting CuI and 4,7-diphenyl-1,10-phenanthroline (Bphen) as the anode and cathode buffer layer, respectively, the device exhibits a low switch threshold voltage of −2.2 V and a high ON/OFF ratio in the order of 10^4.

ITO coated glass substrates with a sheet resistance of 15 Ω sq^{-1} were used as the substrates. These substrates were cleaned sequentially with deionized water, acetone, and ethanol in an ultrasonic bath. Before loading into the high vacuum chamber, they were treated in an ultraviolet-ozone environment for 15 min. All organic layers and Al cathode were deposited onto the substrates *via* thermal evaporation under a pressure of 5×10^{-4} Pa. The bilayer heterojunction device has a structure of ITO/PbPc (60 nm)/F_{16}CuPc (60 nm)/Al (100 nm) (Device A). To improve the performance, a device with a structure of ITO/CuI (4 nm)/PbPc (60 nm)/F_{16}CuPc (60 nm)/Bphen (5 nm)/Al (100 nm) (Device B) was also fabricated, as shown in Fig. 1 with the energy level data from reports.[18,25–27] The top Al cathode was deposited through a shadow mask and the area of the devices is

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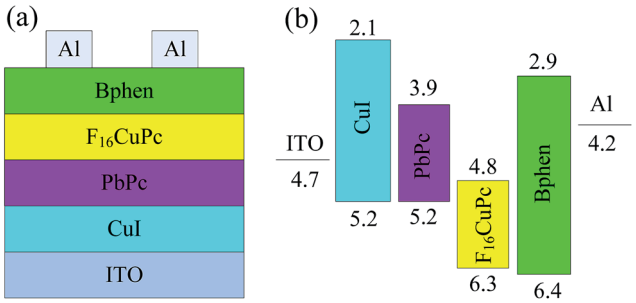

Fig. 1 (a) Structure and (b) schematic energy level diagram of Device B.

3×3 mm^2 defined by the overlap of ITO and Al electrodes. Deposition rates and thickness of the layers were monitored *in situ* using oscillating quartz monitors. The evaporating rates were kept at 1 Å s^{-1} for CuI and organic layers and 10 Å s^{-1} for Al cathode, respectively. Current–voltage (*J–V*) characteristics of the devices were measured with a Keithley 2400 sourcemeter. The measurements were carried out at room temperature under ambient conditions without encapsulation.

Fig. 2 shows the *J–V* curves of Device A with different voltage sweep directions. It can be found that it is on its ON state for the first voltage sweep and the first stage of the second voltage sweep. For the second voltage sweep, the current decreases with the increase of negative voltage after the voltage higher than −4.4 V, indicating that a distinct negative differential resistance (NDR) region appears. This suggests that the device transits from ON state to OFF state. Such a transition corresponds to the "writing" process of a digital memory cell. It should be pointed out that the switch threshold voltage (−4.4 V) is dramatically lower than that reported in the device based on CuPc/F_{16}CuPc heterojunction (−7.6 V).[17] This indicates that the device may be more favorable for application in low-power-consumption memory device. After this voltage sweep, the device is permanently turned to its OFF state for the latter voltage sweeps in both the positive and negative voltage regions (the third and forth voltage sweeps), and it cannot be recovered to ON state again even a high voltage of ±20 V is applied to this device. These properties suggest that it can be used as a WORM memory device. However, the maximum ON/OFF current ratio of this device in positive and negative voltage regions is only about 10^3 and 10, respectively. Such a character is insufficiently for practical applications.

A higher ON/OFF ratio of the device can be expected if the ON state current of the device were increased and/or the OFF state current were decreased. To satisfy these hypotheses, CuI and Bphen are adopted as the anode and cathode buffer layers, respectively. Fig. 2 shows the *J–V* curves of this device (Device B). Similar WORM memory properties are found in Device B. It can be found that both the OFF state currents at positive and negative voltage regions are little affected by the buffer layers, especially at lower voltage. However, both the ON state currents at positive and negative voltage regions are dramatically increased. Fig. 3 illuminates the ON/OFF current ratio of Device B in both positive and negative voltage regions. It can be found that the maximum ON/OFF current ratios in both positive and negative voltage regions can reach up to the order of 10^4, which are comparable to that in CuPc/F_{16}CuPc based WORM memory device reported by Wang *et al.*[17] The significant boosted ON/OFF ratio is primary attributed to the increased ON state current. Besides, the ON/OFF current ratio of Device B is higher than 10^3 in a large voltage region. This would significantly eliminate the memory error and elevate the reliability of the device for practical applications.

More interesting, it can be found from Fig. 2 that the switch threshold voltage is −2.2 V for Device B, which is only half to that of Device A. This indicates that Device B can be operated at a lower voltage, which can reduce the power consumption of the memory device. We have fabricated 8 devices in the same batch, and all these devices display obvious WORM memory characters. The switch threshold voltage and ON/OFF ratio of these devices vary from −2.0 to −2.8 V and 6×10^3 to 1.4×10^4, respectively, indicating high reproducibility of these devices. Resistance transition of a memory device is related to either the

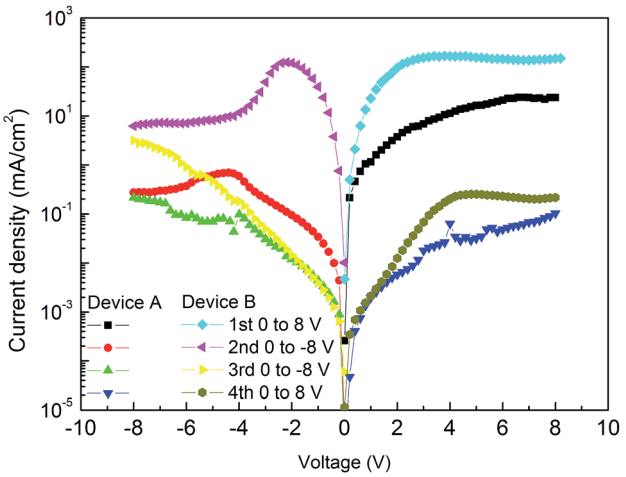

Fig. 2 *J–V* curves of the devices with (Device B) and without (Device A) electrode buffer layers.

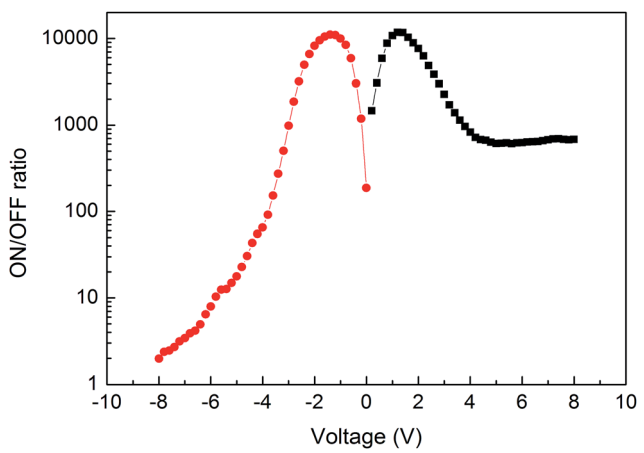

Fig. 3 ON/OFF current ratio of Device B in positive and negative voltage regions.

bulk or the interfacial properties. In view of that both Devices A and B exhibit WORM memory properties, it can be concluded that the WORM memory of these devices is not related to the interfaces of ITO/PbPc, ITO/CuI, CuI/PbPc, F_{16}CuPc/Bphen, F_{16}CuPc/Al, and Bphen/Al.

To further understand the mechanism of the devices, another device with a structure of ITO/PbPc/Bphen/F_{16}CuPc/Al (Device C) was fabricated. Surprisingly, no conductivity transition is observed in this device. This suggests that the bulk properties of PbPc and F_{16}CuPc related mechanisms, such as charge carrier trapping and detrapping, can be ruled out. Thus we come to the conclusion that the WORM memory of Devices A and B is related to the interfacial property of PbPc/F_{16}CuPc. These can well explain that no conductivity transition is observed in Device C as there is no direct contact between PbPc and F_{16}CuPc.

In the CuPc/F_{16}CuPc based WORM memory device, the working mechanism was attributed to the interfacial dipole layer formation in the CuPc/F_{16}CuPc interface.[17] In view of that PbPc has an analogous molecular structure and similar energy level to that of CuPc, we propose that the WORM memory characters are related to the PbPc/F_{16}CuPc interfacial dipole layer formed with the direction from PbPc to F_{16}CuPc due to electron transfer from PbPc to F_{16}CuPc. The energy barriers for hole and electron injection from Al and ITO electrodes are 2.2 and 2.6 eV, respectively, when judging from the schematic energy level diagram of the device shown in Fig. 1(b), which are higher for hole and electron injections. However, the formatted interfacial dipole layer at PbPc/F_{16}CuPc interface may form a space electrical field in the device, which will reduce the charge carrier injection barriers.

It has been reported that a dipole layer is found in the ITO/CuI interface due to electron transfer from ITO to CuI, which increases the workfunction of ITO surface by about 0.7 eV.[28] On the other hand, Shen *et al.* have demonstrated that a strong chemical reaction occurs between F_{16}CuPc and Al during the thermally evaporation of Al cathode, which forms an insulating $(F_{16}CuPc)_3Al$ layer.[29] Thus the higher ON state currents at both positive and negative voltage of Device B can be attributed to the improved charge carrier injection from the electrodes due to the inserting of CuI and Bphen buffer layers. This suggests that the electrode buffer layers are essential for resistive memory devices to tune the carrier injection property. However, such a role has not been exploited in previous reports.

To further confirm the conduction mechanisms of the WORM device, the *J*–*V* characteristics of Device B are fitted with different current transport models. It can be found that a linear relation between log *J* and $V^{1/2}$ is observed in both the ON and OFF states current at low positive voltage, as shown in Fig. 4(a), where the currents subject to the Schottky emission model with the equation of:

$$J = A^{*}T^{2}\exp\left[\frac{-\left(\phi_{b} - \sqrt{q^{3}V/4\pi\varepsilon_{0}\varepsilon_{r}d}\right)}{k_{b}T}\right] \quad (1)$$

where A^{*} is the effective Richardson constant, T is the temperature, ϕ_b is the barrier height, q is the electron charge, ε_0 is the permittivity of the vacuum, ε_r is the relative permittivity of the organic semiconductor, d is the thickness of the organic layer, and k_b is the Boltzmann constant. This indicates that the currents are injection but not bulk transport limited, suggesting that there are not ohmic contacts in the ITO/CuI interface and especially in the Bphen/Al interface. On contrast, a linear relation between log *J* and log *V* is found for both the ON and OFF states current at high positive voltage, as shown in Fig. 4(b). This implies that the current is bulk transport limited and complies with a trap-limited space charge limited current (SCLC) model with the equation of:

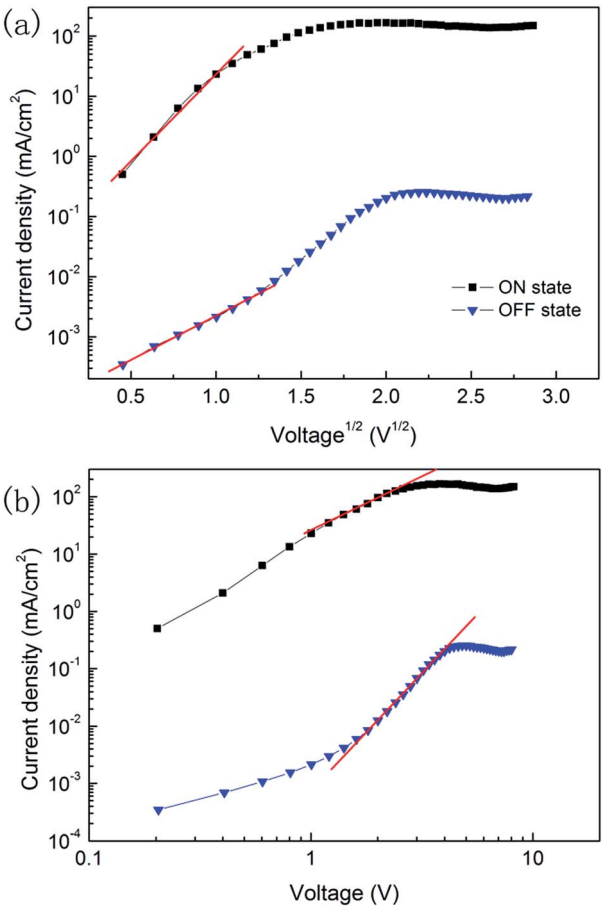

Fig. 4 (a) *J verses* $V^{1/2}$ plots of ON and OFF states current of Device B at positive voltage. (b) Log–log plots of the ON and OFF states current of Device B at positive voltage. The lines present the linear fitting of the data.

$$J = q\mu_{0}N_{c}\left(\frac{\varepsilon_{0}\varepsilon_{r}}{qN_{t}}\frac{l}{l+1}\right)^{l}\left(\frac{2l+1}{l+1}\right)^{l+1}\frac{V^{l+1}}{d^{2l+1}} \quad (2)$$

where μ_0 is the trap-free mobility, N_c is the effective density of states in the transport level, N_t is the total trap density, and $l = E_b/kT$ where E_b is the characteristic energy. These findings suggest that both the ON and OFF states current transit from the Schottky emission model at low bias to the trap-limited SCLC model at high bias. This is because the carrier injection barrier becomes thinner at higher voltage, allowing more carriers to be injected from the electrode through tunnelling. In such a case, the current is not still injection limited.

The ON state current in negative voltage before conductivity transition also shows a linear relation between $\log J$ and $\log|V|$, indicating that it obeys the trap-limited SCLC model, as shown in Fig. 5. This finding indicates that the ON state current at negative voltage is not injection but bulk transport limited. Such a character reverses the charge carrier injection barriers as found in Fig. 1(b) if only the energy levels of the materials were concerned. However, this can be well understood if we take the PbPc/F_{16}CuPc interfacial dipole layer into account. The interfacial dipole layer would lower the hole and electron injection barriers from the Al cathode and ITO anode, respectively, as discussed before.

After the device transition from the ON state to OFF state, the interfacial dipole layer of PbPc/F_{16}CuPc is destructed. Then the current transient from bulk limited to injection limited. In term of the large carrier injection barriers under negative bias, the current should follow the tunnelling model. If the shape of the tunnel barrier were trapezoidal, then the current follows direct tunnelling model with the equation of:[30,31]

$$\ln\left(\frac{J}{V^2}\right) \propto \ln\left(\frac{1}{V}\right) - \frac{2d\sqrt{2m\phi_b}}{\hbar} \quad (3)$$

where m is the effective mass of the charge carrier and $\hbar$ is Planck's constant divided by 2π. On contrast, if the shape of the tunnel barrier were triangular, then the current follows Fowler–Nordheim (F–N) tunnelling model with the equation of:[30,31]

$$\ln\left(\frac{J}{V^2}\right) \propto -\left(\frac{1}{V}\right)\left(\frac{4d\sqrt{2m\phi_b}^3}{3\hbar q}\right) \quad (4)$$

It can be found from Fig. 6 that a linear relation between $\ln(J/V^2)$ and $\ln(|1/V|)$ is observed at low voltage, while between $\ln(J/V^2)$ and $|1/V|$ at high voltage. These indicate that the shape of the tunnel barrier is trapezoidal at low voltage, while it turns to triangular at high voltage. Thus the current model transits from a direct tunnelling model at low voltage to an F–N tunnelling model at high voltage.

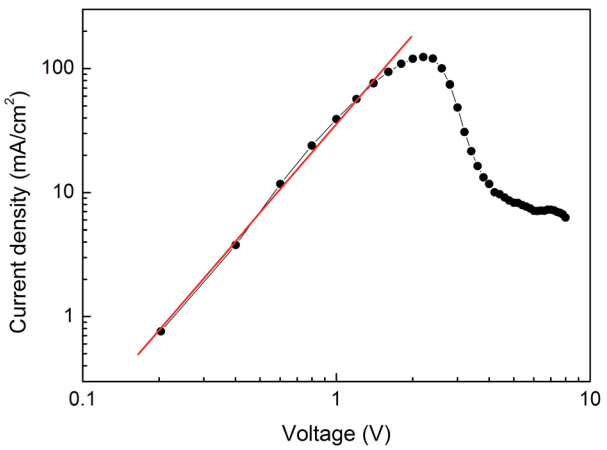

Fig. 5 Log–log plot of the ON state current of Device B at negative voltage, the line presents the linear fitting of the data.

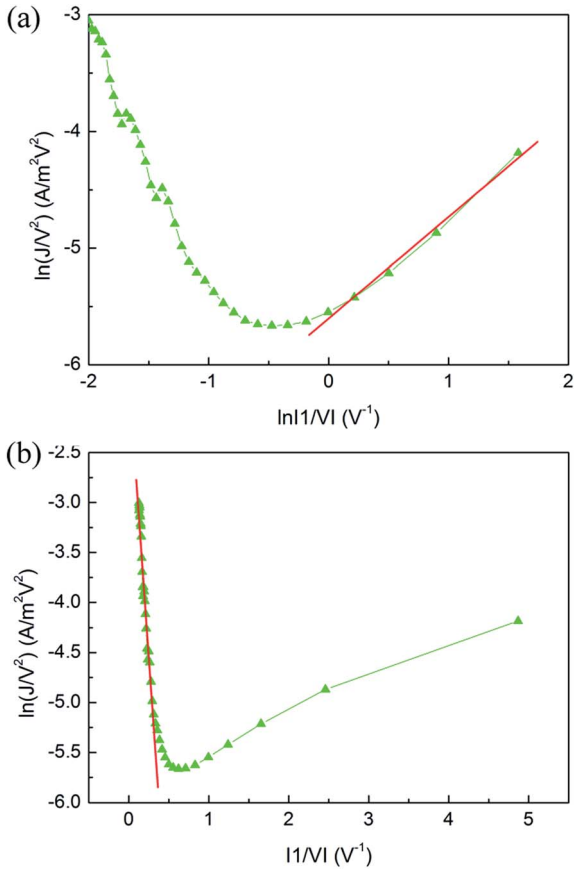

Fig. 6 (a) A $\ln(J/V^2)$ *versus* $\ln|1/V|$ plot and (b) $\ln(J/V^2)$ *versus* $|1/V|$ plot of the OFF state current of Device B. The lines present the linear fitting of the data.

According to the results found above, the ON state of the device at positive voltage region is attributed to the lower charge carrier injection barrier due to the introduction of the electrode buffer layers, while the ON state at negative voltage is attributed to the interfacial dipole layer formed at PbPc/F_{16}CuPc. The OFF state is attributed to the destruction of this interfacial layer and formation of an insulting layer. It should be noted that slight NDR regions are also found in the ON and OFF states at high voltage of positive voltage region, as shown in Fig. 2(b). This should also be attributed to a slight destruction of the interfacial dipole layer. At a low voltage, the injected holes and electrons are primarily recombination at the PbPc/F_{16}CuPc interface. However, at a high voltage, more holes and electrons are injected, the excess holes or electrons will destroy the interfacial dipole layer.

It is found in Fig. 2 that the switch threshold voltage of Device B is lower that Device A and CuPc/F_{16}CuPc based WORM device.[17] For a WORM memory device with an interfacial dipole layer controlled resistive states, the switch threshold voltage depends on the strength of the interfacial dipole and/or the electrical filed across the interface. The electron injection barrier from ITO to PbPc is 0.8 eV (Fig. 1), while it is 1.6 eV from ITO to CuPc.[17] From these energy levels, we cannot gain the reasons for the lower threshold voltage of Device B than CuPc/

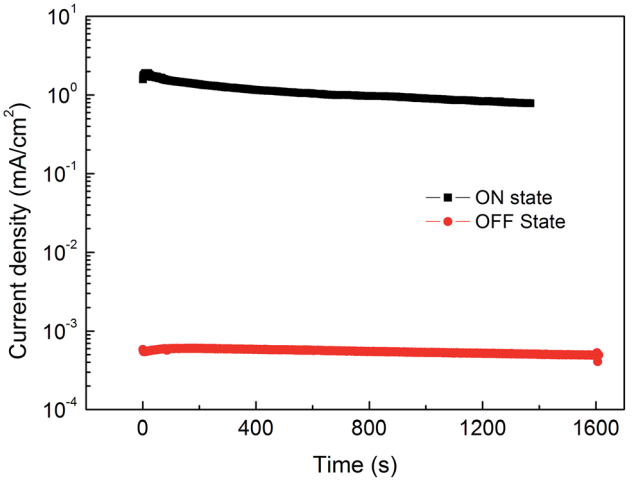

Fig. 7 Retention stability of the ON and OFF states of Device B under bias of 0.5 V.

F_{16}CuPc based WORM device. To address this issue, another device with the structure of ITO/CuI/PbPc/F_{16}CuPc/Al (Device D) was fabricate. Although the electron injection barrier is increased to 2.6 eV from ITO, this device shows a switch threshold voltage of only −5.0 V, which is still lower than CuPc/F_{16}CuPc based device. Such a lower switch threshold voltage may indicate that a lower strength of the PbPc/F_{16}CuPc interfacial dipole than CuPc/F_{16}CuPc, thus the interfacial dipole layer can be destroyed at a lower voltage. On the other hands, the lower switch threshold voltage of Device B than Device A can be attributed to a higher voltage across the PbPc/F_{16}CuPc interface due to the introduced Bphen layer restricting the formation of $(F_{16}CuPc)_3Al$ insulating layer. Similar result has been found in CuPc/F_{16}CuPc based WORM device when a poly (ethylene oxide) cathode buffer layer was used.[17] These findings suggest that the lower switch threshold voltage of Device B can be attributed to both the lower intrinsic strength of the PbPc/F_{16}CuPc interfacial dipole and the higher voltage across the PbPc/F_{16}CuPc interface. Still, substantial future experimental work is required to understand these phenomena and their mechanisms, especially the exact energy level alignment of the device before and after conductivity transition.

Retention stability is another figure-of-merit for memory devices. The ON and OFF states retention times of Device B are depicted in Fig. 7. Both the ON state and OFF state current densities were measured by applying a constant voltage of 0.5 V to the device. During the 1000 s time, the ON state current decreases from 1.6 to 0.9 mA cm^{-2}, while the OFF state current only decreases from 5.7×10^{-4} to 5.3×10^{-4} mA cm^{-2}, corresponding to a slight decrease of ON/OFF ratio from 2.8×10^3 to 1.7×10^3. More importantly, an ON/OFF ratio higher than 10^3 can also be achieved even after 10^4 s by tracing the evolution trend of the currents.

Conclusions

In summary, a nonvolatile organic WORM memory device is demonstrated based on PbPc/F_{16}CuPc heterojunction. By using CuI and Bphen as the anode and cathode buffer layers, the device shows a low switch threshold voltage of −2.2 V and a high ON/OFF current ratio in the order of 10^4 as well as a high retention stability. The lower switch threshold voltage can be attributed to both the lower intrinsic strength of the PbPc/F_{16}CuPc interfacial dipole and the higher voltage across the PbPc/F_{16}CuPc interface. These results suggest that the buffer layers play important roles in organic WORM memory devices, and this work provides a strategy to construct high performance and low-power-consumption nonvolatile organic WORM memory devices.

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