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Metal-insulator-semiconductor field-effect transistors (MISFETs) using p-type SnS and nanometer-thick Al₂S₃ layers†

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Novel and cost-effective metal-insulator semiconductor field-effect transistor (MISFET) devices were fabricated using non-toxic tin mono sulfide (SnS) as the active layer sandwiched between aluminium and silver contacts with an unintentionally grown aluminium sulfide (Al₂S₃) interface layer. MISFET devices exhibit a high turn-on voltage of 5.13 V and excellent rectifying diode characteristics. These devices also show a high rectification factor of 1383 at a bias voltage of 6 V and series resistance of 3.4 M Ω , along with a very low leakage current of ~10⁻⁹ A@-10 V. The overall results reveal that it could be possible to fabricate cost-effective and non-toxic MISFET devices by using SnS as an active layer for various power-electronic applications.

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Introduction

In recent years, tin mono sulfide (SnS) semiconductor material has received considerable attention as an absorber material particularly for photovoltaic applications.¹⁻³ In general, SnS thin films exhibit a direct optical band gap of 1.35 eV and high absorption coefficient of $\sim 10^5$ cm⁻¹.⁴⁻⁶ Thin films of SnS have been prepared using various chemical and physical methods,⁷⁻²⁰ and their electrical properties are easily tailored by doping appropriate dopants.²¹⁻²⁴ Orthorhombic structured SnS exhibits stable structural and optical properties up to a maximum temperature of 600 °C.^{18,25} Compared to other efficient absorber materials, the toxicity and cost of SnS are low,²⁶ and the achievable maximum light conversion efficiency with SnS is about 25%.²⁷



Although the studies on SnS thin films based devices are still

at a preliminary level, a wide range of interesting and important applications have been made, including in photovoltaics,

On the other hand, Schottky diodes, developed with different conventional semiconductor materials (Si, GaAs, GaN, InP and SiC)^{35–39} play a crucial role as detectors, rectifiers, light converters, switches and couplers. Although these devices have

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better performance and excellent durability, today researchers are looking for a new class of materials due to high fabrication cost and toxicity of the existing materials. As stated above, SnS is one of the cost-effective and nontoxic materials and can be synthesized using different low-cost techniques. Thus, it facilitates the production of low-cost and toxic-free Schottky devices. However, up to now, only minimal work has been carried out on the development of SnS based Schottky diodes.40-43 For example, the Safak group have explored the Schottky device properties and noticed an increase in barrier height (0.47-0.52 eV) of Ag/ SnS devices with the increase of temperature from room temperature (RT) to 100 °C.44 Further, while decreasing temperature from RT to low, a gradual decrease in barrier height and increase in series resistance have been observed.43,45 More recently, Das and colleagues as well as Mathews have studied the electrical behavior of SnS films with Al contacts. Here, Das and colleagues observed nearly ohmic characteristics from the Al/SnS/In structures even for annealed SnS films,41 whereas Mathews observed Schottky barrier properties from ITO/SnS/Al structures.⁴⁰ On the other hand, our group noticed typical properties such as crystallinity, preferential growth, and optical quality from SnS films deposited on latticed matched Al substrates.46 These interesting features of SnS films motivated us to investigate the electrical properties of SnS films by depositing them over Al coated substrates.

In this study, we fabricated p-type SnS nanocrystals based Schottky devices with the configuration of Al/SnS/Ag, and realized MISFET device characteristics due to the unintentionally grown Al₂S₃ layer between Al and SnS as the interface layer. The morphology, crystal structure and quality of SnS structures deposited on Al coated glass substrates were studied and compared with the properties of SnS structures deposited on bare glass substrate. The performance of MISFET devices was investigated at room temperature. The as-grown devices exhibited high turn-on voltage of 5.13 V and very low leakage current (10^{-9} A@-10 V), which are highly desirable parameters for different applications including high power devices, microwave devices and optoelectronic devices.

Experimental procedure

SnS nanostructures based devices with an Al/ $(Al_2S_3)/SnS/Ag$ sandwich configuration were fabricated on glass substrates using thermal evaporation technique and the charge transport characteristics were studied with the probe-station as described below.

Fabrication of devices

As shown in the schematic diagram in Fig. 1, initially a thin layer (~100 nm) of high pure aluminium (Al with 4N purity) was deposited on cleaned glass substrates (Step-I). The deposition was carried out in a thermal evaporation system, without any applied heating, under a vacuum of ~10⁻⁶ Torr. The rate of deposition was maintained at 2 nm s⁻¹. SnS nanostructures were grown with a deposition rate of 0.2 nm s⁻¹ and thickness of 250 nm at a substrate temperature of 350 °C on bare glass



Fig. 1 Schematic representation of fabrication of Al/(Al_2S_3)/SnS/Ag MISFET device.

substrates (used for comparison) and Al coated glass substrates (Step-II).⁴⁷ In the case of glass/Al substrates, a piece of glass was used as a mask to protect the small portion of the Al layer from SnS deposition. Without breaking the vacuum, the structures were kept under the same condition for 10 min and cooled down to room temperature. Then, point-shaped silver (Ag with 4N purity) contacts were deposited at RT on glass/Al/SnS structures with a gap of 5 mm (thickness ~100 nm) by using a mask under the same vacuum condition (Step-III).

Characterization

The surface morphology and chemical composition of SnS structures grown on both the substrates were analyzed using field emission scanning electron microscopy (FESEM, ZEISS ULTRA 55, Gemini), noncontact optical profilometer (TalySurf CCI MP) and energy dispersive X-ray spectroscopy (EDS, Oxford Instruments) attached with FESEM. The crystal structure and phase purity of SnS structures were studied using an X-ray diffractometer (XRD, Phillip's XPERT PRO, PANalytical B.V., The Netherlands) with Cu $K_{\alpha 1}$ radiation ($\lambda = 0.1541$ nm) and micro Raman spectroscopy (Lab RAM HR (HORIBA JOBI-NYUON)). The electrical resistance of SnS nanostructures grown on Al coated glass substrates, and the carrier transport properties of the Al/(Al2S3)/SnS/Ag devices were estimated by measuring the current-voltage (I-V) characteristics with a probe station attached to a semiconductor parameter analyzer (Agilent Device Analyzer B1500A).

Results and discussion

The SnS structures deposited on Al coated glass substrates appear to be light-brown in color, whereas the structures on bare glass appear to be dark-brown in color. The physical properties (surface morphology, composition, crystal structure and optical vibrational modes) of SnS structures deposited on Al coated glass substrates are described here by comparing with the data obtained from the structures deposited on bare glass substrates.

Basic properties

FESEM studies (Fig. 2) show that the surface features of the SnS structures developed on the two different substrates are almost



Fig. 2 FESEM images of SnS structures grown on (a) Al coated and (b) bare glass substrates, (c) cross-section FESEM image of SnS structures on Al coated glass substrates and (d) elemental composition of SnS structures grown on (top) Al coated and (bottom) bare glass substrates.

similar. However, the surface of the SnS structures on glass is comparatively rougher than that of the structures grown on Al layers (see ESI-1a and b[†]), which is probably attributed to the variation of the adatom mobility of the evaporated atoms on different surfaces.⁴⁸ Compared to earlier results,⁴⁷⁻⁴⁹ the present SnS structures consist of a unique surface morphology, which is mainly attributed to the post-annealing of structures. On the other hand, the cross-section FESEM image (Fig. 2c) shows that SnS structures consist of nanocrystalline crystals, which have almost orthorhombic crystal shapes. These results are very close to those of our earlier reported work.47 EDS studies show that the SnS structures grown on both the substrates have an almost stoichiometric chemical composition (see ESI-2† for EDS spectra). However, the Sn to S atomic percentage ratio of SnS structures grown on Al coated and bare glass substrates is found to be 1.06 and 1.03, respectively. This reveals that comparatively, the SnS structures on the Al coated glass substrates consist of a slightly tin-rich (or sulfur deficient) chemical composition.

XRD profiles of SnS structures grown on Al coated and bare glass substrates are shown in Fig. 3, and all diffracted peaks are indexed with corresponding planes of SnS and Al. The profile of SnS structures grown on Al layers (Fig. 3b) shows three dominant peaks diffracted at $2\theta = 32.03$, 44.8 and 66.3°, which belong to SnS (040), SnS (141) and/or Al (200), and Al (220), respectively, since the calculated *d*-spacing values of these peaks exactly match the orthorhombic SnS and cubic Al (JCPDS: 39-0354 and 04-0787). The remaining weak diffraction peaks belong to SnS, implying that SnS crystallites on Al coated glass substrates are preferentially orientated along the (010) direction. Compared to the SnS structures grown on glass substrate (Fig. 3a), the intensity of the preferential peak of the SnS structures on the Al layer is higher and broader. To determine the reason for the broadness of the preferential peak, the elaborated XRD spectrum of SnS structures grown on Al layers was fitted with multi-peak Gaussian function. This reveals that the broad peak consists of an additional diffraction peak along with the SnS (040) peak at $2\theta = 31.56^{\circ}$ (ESI-2 and 3[†]), which probably belongs to aluminium sulfide (Al₂S₃).⁵⁰ This Al₂S₃ might have formed as an interfacial layer at the time of the growth of the SnS structures on the Al coated glass substrate, which can be expressed by a chemical equation as:

$$2Al + 3S \xrightarrow{\Delta} Al_2S_3$$

Micro Raman spectroscopy studies (Fig. 4) show that the SnS structures grown on both substrates consist of four distinguishable Raman peaks at 94, 159, 185 and 217 cm⁻¹. These peaks can be attributed to the first order single-phononoriented transverse or longitudinal optical (TO and LO) vibration modes, and are assigned to $A_g(TO)$, $B_{2g}(LO)$, $Ag(LO_1)$ and $Ag(LO_2)$, respectively. However, the Raman peaks that observed at higher wavenumbers, *i.e.* 255 and 478 cm⁻¹, belong to the Al_3S_3 phase.^{51,52} On the other hand, compared to the Raman spectrum of the SnS structures grown on glass substrates (Fig. 4a), the nanostructures grown on Al coated substrates consist of sharp lines and exhibit considerable shifts in positions, which can be attributed to surface smoothness and/or



Fig. 3 XRD profile of SnS structures grown on (a) bare and (b) Al coated glass substrates.



g. 4 Raman spectrum of SnS nanostructures deposited on (a) bare and (b) Al coated glass substrates

crystalline quality of the SnS structures.^{47,53} For example, Akgul *et al.* noticed sharp Raman peaks with low full width at half maximum (FWHM) values from highly crystalline copper oxide films,⁵⁴ whereas the increase in sharpness of Raman peaks was noticed by Zgheib *et al.* while fabricating silicon carbide thin films over germanium modified substrates.⁵⁵ Furthermore, these results are consistent with our earlier results of SnS structures grown with slow-rate of deposition over glass substrates at different temperatures.⁴⁶

Therefore, the XRD and Raman studies along with chemical composition analyses clearly emphasized that Al_2S_3 was formed as an interfacial layer between the Al and SnS structures, which probably acts as an insulating layer between metal (Al) and semiconductor (SnS) structures.

Device characteristics

I–V plots measured between Ag–Ag and Ag–Al contacts are shown in Fig. 5. Measurements between Ag and Ag circular contacts show that these silver contacts have ohmic characteristics with SnS nanostructures grown on Al coated glass substrates (Fig. 5a). The resistivity of SnS columnar structures, from the linear slope of the *I–V* curve, is found to be 6.7 Ω cm.

This value is very low compared to the electrical resistivity of SnS structures deposited on glass substrates.⁵⁶ On the other hand, *I–V* measurements between Ag and Al contacts exhibit non-ideal and rectifying characteristics (Fig. 5b), which is discussed in detail at the end of the section using energy band diagram of the device. This noticeable rectification behavior of the device is probably attributed to the unintentionally formed insulating Al_2S_3 layer between the Al and SnS structures as the interfacial layer, since the Al contacts deposited on SnS films at the substrate temperature of 50 °C exhibited ohmic characteristics.⁵⁷

Under both bias conditions, the current flow through the devices, although the magnitudes differ, starts at above a certain bias voltage (± 3.2 V), which can be clearly observed in Fig. 6. This typical voltage is treated as an interfacial barrier potential ($V_{\rm IB}$). Above $V_{\rm IB}$, the changes in current flow of the device in reverse-bias condition are marginal, whereas in forward-bias, they are significant. These devices exhibit a turn-on voltage of 5.13 V and high rectification factor of 1383 at a bias voltage of ± 6 V (Fig. 6a) since the magnitude of current in the device at ± 6 V is about 0.26 and 1.88×10^{-4} A, respectively.⁵⁸ Further, the overall current flow through the device in forward-bias condition is significantly high, which is in the



Fig. 5 Current–voltage plots of SnS nanocrystalline structures measured between (a) Ag and Ag contacts (inset shows a photograph of Ag contacts deposited on SnS structures over Al coated glass substrates) and (b) Al and Ag contacts.



Fig. 6 (a) ln(current) versus voltage plot measured in reverse and forward bias conditions (-10 to 10 V) and (b) dV/d/versus voltage plot measured only in forward bias condition (0-10 V) of $Al/(Al_2S_3)/SnS/Ag$ structures.

order of μA , whereas in reverse bias, it is in the order of nA. These results clearly reveal that the devices fabricated with the configuration of Al/(Al₂S₃)/SnS/Ag consist of MISFET device characteristics.

Variation in *in situ* series resistance (R_s) of the device ($R_s = dV/dI$) with the increase of forward-bias voltage (Fig. 6b) shows three distinguishable regions (<3.2, 3.2–6 and >6 V).⁵⁹ As discussed in the literature, the device resistance at below 3.2 V is too high ($\sim 10^9 \Omega$), which reflects an insulator capacitor characteristic, whereas at higher voltages, >6 V, the resistance of the device is nearly constant at $10^6 \Omega$, which is similar to a Schottky type capacitor. Under moderate bias voltages, the device behavior includes both the insulator and Schottky capacitor. Therefore, the presence of the Al₂S₃ layer as an interfacial barrier between the Al and SnS nanostructured layers (since Al₂S₃ is a wide band gap material,⁶⁰ and most of the other parameters are not yet known) probably acts as an insulating layer and strongly influences the device properties.⁶¹

To understand the transport mechanism of charge carriers, the experimental data was fitted to the diode equation given below.⁴⁰

$$I = I_{\rm o} \left[\exp\left(\frac{q(V - IR_{\rm s})}{nkT}\right) - 1 \right]$$

where I_0 is the saturation current $[=AA^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right), A$ is the effective area of the diode, A^* is the effective Richardson constant (25 A cm⁻² K⁻² for SnS since the effective mass of the electron is about $0.22m_0$), *T* is the absolute temperature, *q* is the charge of electron, ϕ_b is the barrier height, *k* is the Boltzmann constant $(1.38 \times 10^{-23} \text{ J K}^{-1})$], *V* is the applied bias voltage, R_s is the series resistance and *n* is the ideality factor of the diode. The nature of the $\ln(I)$ versus voltage curve of the device in reverse and forward bias conditions is shown in Fig. 6a. It is clearly revealed that at above 3.2 V, the current flow through the device follows three different mechanisms. Initially, it increases sharply with the increase of forward bias voltage up to 4 V and follows simple $I \propto V$ relation. This implies that between 3 and 4 V, the device consists of a thermionic emission or field

emission transport mechanism (ohmic conduction). Based on the above equation, the device parameters ideality factor (n) and saturation current (I_0) of the device are found to be 2.35 and 10^{-35} A, respectively. Further, the barrier height $\phi_{\rm b}$ of the device is found to be 2.37 V.43 Compared to previous results on SnS Schottky diodes, the ideality factor and barrier height of the present device are too high, which can be attributed to the presence of the Al₂S₃ interfacial layer.⁶² At moderate voltages (4-6 V), the current flow through the device varied exponentially with the increase of bias voltage (*i.e.* $I \propto \exp(-C_1 V)$, where $C_1 = 0.94$). This implies that the carrier transport mechanism gradually changes with an increase of bias-voltage from thermionic emission to recombination-tunneling. On the other hand, at higher voltages, >6 V, the current flow through the device is strongly determined by the thermionic emission as well as by the spacecharge limited current transport mechanism, since $I \propto (C_2 V +$ $C_3 V^2$), where C_2 and C_3 are 1.77 and -0.09, respectively. Here, the observed exponential constant under recombination-tunneling characteristics (*i.e.* $C_1 = 0.94$) is low and thus the injection of carriers, and thereby recombination of trap states in the device is moderate. At higher voltages, the negative sign of C_3 constant (-0.09) indicates that the influence of space-charge carriers on the current flow of the device gradually increases with increase of bias voltage. These results are very similar to those of the MISFET devices fabricated with GaAs structures.59

Carrier transport mechanism

The MISFET device behavior with bias voltage can be understood with the help of the schematic energy band diagram of the Al/Al₂S₃/SnS/Ag structure, as shown in Fig. 7 along with individual elements. When the applied bias voltage at Al is negative, the electrons move towards SnS and the holes move in the opposite direction. Thus, the recombination of the carriers increases at around the Al₂S₃ interface and thereby increases the barrier height (eV_{bi}), which creates immobilized cations. Therefore, the current flow through the device is mainly attributed to diffusion with the recombination of a few carriers. Consequently, the current flow through the device in reverse bias conditions is significantly low.



When the applied bias voltage at Al is positive, both carriers (*i.e.* holes and electrons) move in the opposite direction and thus, the barrier height of the device decreases with the increase of bias voltage. At moderate voltage, the successful recombination of electrons with holes dominates the device current flow, as noticed above. Thus, the device fabricated with Al/SnS/Ag with an unintentionally grown Al_2S_3 interface layer works as a MISFET. However, to understand the device properties of Al/ $(Al_2S_3)/SnS/Ag$ structures in detail, further studies need to be carried out such as capacitance–voltage, interface analysis and temperature dependent *I–V* properties of the device. Further, a detailed investigation is needed on Al_2S_3 structures.

Conclusions

SnS nanostructures based Schottky devices were fabricated using Al and Ag contacts and the electrical transport characteristics were investigated at room temperature. The as-grown SnS structures on Al coated glass substrates consist of stoichiometric chemical composition and exhibited an electrical resistivity of 6.7 Ω cm. Al/SnS/Ag devices exhibited metalinsulator-semiconductor FET characteristics with a high turnon voltage of +5.13 V due to the presence of the unintentionally grown Al₂S₃ layer as the interfacial layer between Al and SnS. The leakage current under reverse bias-voltage is extremely low, $\sim 10^{-9}$ A at 10 V, and the rectification factor of the device at a bias voltage of 6 V is found to be 1383. These overall outcomes strongly emphasize that SnS based MISFET devices could have applications in different fields including power, microwave and optoelectronic devices where high turn-on voltage and high breakdown voltages are prerequisites.

Note added after first publication

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References

- 1 G. A. Tritsaris, B. D. Malone and E. Kaxiras, *J. Appl. Phys.*, 2013, **113**, 233507.
- 2 M. Steichen, R. Djemour, L. Gutay, J. Guillot, S. Siebentritt and P. J. Dale, *J. Phys. Chem. C*, 2013, **117**, 4383–4393.
- 3 R. W. Miles, O. E. Ogah, G. Zoppi and I. Forbes, *Thin Solid Films*, 2009, **517**, 4702–4705.
- 4 M. Devika, K. T. R. Reddy, N. K. Reddy, K. Ramesh, R. Ganesan, E. S. R. Gopal and K. R. Gunasekhar, *J. Appl. Phys.*, 2006, **100**, 023518.
- 5 K. T. R. Reddy, P. P. Reddy, R. Datta and R. W. Miles, *Thin Solid Films*, 2002, **403**, 116–119.
- 6 R. E. Banai, H. Lee, M. A. Motyka, R. Chandrasekharan, N. J. Podraza, J. R. S. Brownson and M. W. Horn, *IEEE Journal of Photovoltaics*, 2013, 3, 1084–1089.
- 7 S. Y. Cheng and G. Conibeer, *Thin Solid Films*, 2011, **520**, 837-841.
- 8 E. Guneri, F. Gode, C. Ulutas, F. Kirmizigul, G. Altindemir and C. Gumus, *Chalcogenide Lett.*, 2010, 7, 685–694.
- 9 E. Guneri, C. Ulutas, F. Kirmizigul, G. Altindemir, F. Gode and C. Gumus, *Appl. Surf. Sci.*, 2010, 257, 1189–1195.
- 10 A. Tanusevski, Semicond. Sci. Technol., 2003, 18, 501-505.
- 11 L. K. Khel, S. Khan and M. I. Zaman, *J. Chem. Soc. Pak.*, 2005, 27, 24–28.
- 12 N. Sato, M. Ichimura, E. Arai and Y. Yamazaki, Sol. Energy Mater. Sol. Cells, 2005, 85, 153–165.
- 13 K. Takeuchi, M. Ichimura, E. Arai and Y. Yamazaki, *Sol. Energy Mater. Sol. Cells*, 2003, 75, 427–432.
- K. Hartman, J. L. Johnson, M. I. Bertoni, D. Recht, M. J. Aziz, M. A. Scarpulla and T. Buonassisi, *Thin Solid Films*, 2011, 519, 7421–7424.

- 15 J. Henry, K. Mohanraj, S. Kannan, S. Barathan and G. Sivakumar, *Eur. Phys. J.: Appl. Phys.*, 2013, 61, 10301.
- 16 A. Tanusevski and D. Poelman, *Sol. Energy Mater. Sol. Cells*, 2003, **80**, 297–303.
- 17 N. K. Reddy and K. T. R. Reddy, *Thin Solid Films*, 1998, **325**, 4–6.
- 18 N. K. Reddy, Y. B. Hahn, M. Devika, H. R. Sumana and K. R. Gunasekhar, *J. Appl. Phys.*, 2007, **101**, 093522.
- 19 A. Sanchez-Juarez, A. Tiburcio-Silver and A. Ortiz, *Thin Solid Films*, 2005, **480**, 452–456.
- 20 N. Koteeswara Reddy, K. Ramesh, R. Ganesan, K. T. Ramakrishna Reddy, K. R. Gunasekhar and E. S. R. Gopal, *Appl. Phys. A: Mater. Sci. Process.*, 2006, 83, 133–138.
- 21 K. S. Kumar, A. G. Manohari, S. Dhanapandian and T. Mahalingam, *Mater. Lett.*, 2014, **131**, 167–170.
- 22 M. Reghima, A. Akkari, C. Guasch, M. Castagne and N. Kamoun-Turki, *J. Renewable Sustainable Energy*, 2013, 5, 063109.
- 23 H. Y. He, J. Fei and J. Lu, *Mater. Sci. Semicond. Process.*, 2014, 24, 90–95.
- 24 P. Sinsermsuksakul, R. Chakraborty, S. B. Kim, S. M. Heald,
 T. Buonassisi and R. G. Gordon, *Chem. Mater.*, 2012, 24, 4556–4562.
- 25 N. K. Reddy, M. Devika, M. Prashantha, K. Ramesh and K. R. Gunasekhar, *Eur. Phys. J.: Appl. Phys.*, 2012, **60**, 10102.
- 26 N. K. Reddy, M. Devika and E. S. R. Gopal, *Crit. Rev. Solid State Mater. Sci.*, 2015, **40**, 359–398.
- 27 J. J. Loferski, J. Appl. Phys., 1956, 27, 777-784.
- 28 H. Noguchi, A. Setiyadi, H. Tanamura, T. Nagatomo and O. Omoto, Sol. Energy Mater. Sol. Cells, 1994, 35, 325–331.
- 29 M. Gunasekaran and M. Ichimura, *Sol. Energy Mater. Sol. Cells*, 2007, **91**, 774–778.
- 30 D. Avellaneda, G. Delgado, M. T. S. Nair and P. K. Nair, *Thin Solid Films*, 2007, 515, 5771–5776.
- 31 B. Ghosh, M. Das, P. Banerjee and S. Das, Semicond. Sci. Technol., 2009, 24, 025024.
- 32 Y. Wang, H. Gong, B. H. Fan and G. X. Hu, *J. Phys. Chem. C*, 2010, **114**, 3256–3259.
- 33 A. Stavrinadis, J. M. Smith, C. A. Cattley, A. G. Cook, P. S. Grant and A. A. R. Watt, *Nanotechnology*, 2010, 21, 185202.
- 34 T. Ikuno, R. Suzuki, K. Kitazumi, N. Takahashi, N. Kato and K. Higuchi, *Appl. Phys. Lett.*, 2013, **102**, 193901.
- 35 J. Eriksson, N. Rorsman and H. Zirath, *IEEE Trans. Microwave Theory Tech.*, 2003, **51**, 796–804.
- 36 J. Beichler, W. Fuhs, H. Mell and H. M. Welsch, J. Non-Cryst. Solids, 1980, 35–6, 587–592.
- 37 O. Vural, Y. Safak, A. Turut and S. Altindal, J. Alloys Compd., 2012, 513, 107–111.
- 38 D. Donoval, A. Chvala, R. Sramaty, J. Kovac, J. F. Carlin, N. Grandjean, G. Pozzovivo, J. Kuzmik, D. Pogany, G. Strasser and P. Kordos, *Appl. Phys. Lett.*, 2010, 96, 223501.
- 39 D. Korucu and T. S. Mammadov, J. Optoelectron. Adv. Mater., 2012, 14, 41–48.

- 40 N. R. Mathews, Semicond. Sci. Technol., 2010, 25, 105010.
- 41 B. Ghosh, M. Das, P. Banerjee and S. Das, *Solid State Sci.*, 2009, **11**, 461–466.
- 42 M. Sahin, H. Safak, N. Tugluoglu and S. Karadeniz, *Appl. Surf. Sci.*, 2005, 242, 412–418.
- 43 S. Karadeniz, M. Sahin, N. Tugluoglu and H. Safak, *Semicond. Sci. Technol.*, 2004, **19**, 1098–1103.
- 44 H. Safak, M. Sahin and O. F. Yuksel, *Solid-State Electron.*, 2002, **46**, 49–52.
- 45 S. Karadeniz, N. Tugluoglu, M. Sahin and H. Safak, *Microelectron. Eng.*, 2005, **81**, 125–131.
- 46 M. Devika, N. Koteeswara Reddy, M. Prashantha, K. Ramesh,
 S. Venkatramana Reddy, Y. B. Hahn and K. R. Gunasekhar, *Phys. Status Solidi A*, 2010, 207, 1864–1869.
- 47 N. K. Reddy, ECS J. Solid State Sci. Technol., 2013, 2, P259– P263.
- 48 M. Devika, N. K. Reddy, K. Ramesh, H. R. Sumana, K. R. Gunasekhar, E. S. R. Gopal and K. T. R. Reddy, *Semicond. Sci. Technol.*, 2006, 21, 1495–1501.
- 49 M. Devika, N. K. Reddy, K. Ramesh, R. Ganesan, K. R. Gunasekhar, E. S. R. Gopal and K. T. R. Reddy, *J. Electrochem. Soc.*, 2007, **154**, H67–H73.
- 50 P. F. Smet, D. Poelman and R. L. Van Meirhaeghe, *J. Appl. Phys.*, 2004, **95**, 184–190.
- 51 H. Haeuseler, A. Cansiz and H. D. Lutz, *Z. Naturforsch., B: J. Chem. Sci.*, 1981, **36**, 532.
- 52 P. Zhou, J. Wang, F. Cheng, F. Li and J. Chen, *Chem. Commun.*, 2016, **52**, 6091–6094.
- 53 B. Balamurugan, B. R. Mehta, D. K. Avasthi, F. Singh, A. K. Arora, M. Rajalakshmi, G. Raghavan, A. K. Tyagi and S. M. Shivaprasad, *J. Appl. Phys.*, 2002, **92**, 3304–3310.
- 54 F. A. Akgul, G. Akgul, N. Yildirim, H. E. Unalan and R. Turan, Mater. Chem. Phys., 2014, 147, 987–995.
- 55 C. Zgheib, L. E. McNeil, M. Kazan, P. Masri, F. M. Morales, O. Ambacher and J. Pezoldt, *Appl. Phys. Lett.*, 2005, 87, 041905.
- 56 M. Devika, N. Koteeswara Reddy, D. Sreekantha Reddy, Q. Ahsanulhaq, K. Ramesh, E. S. R. Gopal, K. R. Gunasekhar and Y. B. Hahn, *J. Electrochem. Soc.*, 2008, 155, H130–H135.
- 57 M. Devika, N. K. Reddy, F. Patolsky and K. R. Gunasekhar, *J. Appl. Phys.*, 2008, **104**, 124503.
- 58 C. C. Wang, H. K. Huang, Y. H. Wang, M. P. Houng, C. L. Wu and C. S. Chang, *Solid-State Electron.*, 2004, **48**, 1683–1686.
- 59 F. Ren and E. S. E. Division, Proceedings of the Symposium on High Speed III–V Electronics for Wireless Applications and the Twenty-Fifth State-of-the-Art Program on Compound Semiconductors (SOTAPOCS XXV), Electrochemical Society, 1996.
- 60 S. K. Oh, H. J. Song, W. T. Kim, M. S. Jin, T. Y. Park, H. G. Kim and S. H. Choe, *Semicond. Sci. Technol.*, 1999, 14, 848–851.
- 61 L. C. Zhang, Q. S. Li, L. Shang, Z. J. Zhang, R. Z. Huang and F. Z. Zhao, *J. Phys. D: Appl. Phys.*, 2012, 45, 485103.
- 62 C. P. Chen, Y. A. Chang, J. W. Huang and T. F. Kuech, *Appl. Phys. Lett.*, 1994, **64**, 1413–1415.