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High-performance non-volatile field-effect transistor memories using an amorphous oxide semiconductor and ferroelectric polymer

Transistor memories using a ferroelectric polymer and an inorganic oxide have been constructed. The interfacial charge transfer is beneficial to the improvement in device performance, exhibiting a record-high electron mobility of 84 cm^2 V^{-1} s^{-1}.

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PAPER

High-performance non-volatile field-effect transistor memories using an amorphous oxide semiconductor and ferroelectric polymer†

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Ferroelectric field-effect transistors (Fe-FETs) are of great interest for a variety of non-volatile memory device applications. High-performance top-gate Fe-FET memories using ferroelectric polymers of poly-(vinylidene fluoride–trifluoroethylene) (P(VDF–TrFE)) and the inorganic oxide of InSiO were fabricated. The extracted electron mobility was as high as 84.1 cm^2 V^{-1} s^{-1} in a low-frequency state. The interfacial charge transfer between the P(VDF–TrFE) and InSiO during annealing of the P(VDF–TrFE) layer benefits improvement in the device performance. The results show the potential of our Fe-FET memories for next-generation electronics.

Introduction

Field-effect transistors (FETs) based on amorphous oxide semiconductors have been the focus of considerable interest for various applications, such as drivers for active-matrix displays with ultrahigh resolution.[1–4] In recent years, hybrid ferroelectric non-volatile memories, which use oxide semiconductor materials and ferroelectric polymers as the conducting and dielectric layers, respectively, have been recognized as a promising strategy for the achievement of high electrical performance.[5–7] Many studies involve amorphous oxide semiconductor ferroelectric FET memory.[7–10] Among various ferroelectric polymer memories, those based on poly(vinylidene fluoride) and its copolymers are the most popular because of their easy solution processing, low annealing temperature, and excellent chemical stability.[11,12] However, using poly(vinylidene fluoride–trifluoroethylene) (P(VDF–TrFE)) as an insulating layer for the ferroelectric transistors does not allow for high mobility. This issue also causes a slow charge accumulation process and storage speed.[11] Therefore, a hybrid inorganic/organic structure using an amorphous oxide semiconductor is proposed to improve electrical performance.

In our previous studies, we have investigated the relationship between the carrier mobility of the amorphous oxide semiconductor and interfacial charge carrier density.[13,14] Carrier mobility can be improved with an increase in conducting charge density. For amorphous oxide semiconductor materials, electrical conduction is often the result of the existence of oxygen vacancies (V_O) and interstitial metal atoms, which can act as electron donors and acceptors, respectively.[15] InO$_x$-based oxide materials are typical n-type oxide semiconductors, in which V_O allows electrons to be available at the conduction band.[15–21] In various studies involving InO$_x$-based amorphous oxide semiconductors, doping of rare metals such as tin, zirconium, and gallium, always exists.[20–25]

This study proposes a strategy for fabricating high-performance ferroelectric field-effect transistor (Fe-FET) memory with P(VDF–TrFE) as the dielectric layer and InSiO (In$_2$O$_3$/SiO$_2$ = 90 : 10 wt%) as the n-type semiconductor layer. InSiO is an n-type InO$_x$-based oxide material without the second-time and rare-metal doping. The extracted field-effect mobility (μ_{FET}) is as high as 84.1 cm^2 V^{-1} s^{-1} and was detected through capacitance measurement at low frequency, 200 Hz. The enhanced mobility is mainly dominated by the increase in charge carrier density, which is due to the existence of interfacial charge transfer from the P(VDF–TrFE) layer to the semiconducting channel. Our work reveals that Fe-FET memories using hybrid organic/inorganic structure are promising for next-generation electronics.

Experimental

Fabrication of Fe-FET memories

Heavily-doped Si wafers with 250 nm-thick SiO$_2$ on top were subsequently cleaned with acetone and isopropanol and then

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treated with UV-ozone. Ten nanometer-thick InSiO films were deposited on the wafer by DC magnetron sputtering using the InSiO$_x$ target, with a weight ratio of 90 to 10 between In$_2$O$_3$ and SiO$_2$, through a shadow mask at room temperature. The channel width was set to 1000 μm. The InSiO films were annealed at 250 °C for 30 min under ambient atmosphere. Au (30 nm) was deposited by thermal evaporation through a shadow mask as the source and drain electrodes. Thereafter, 3 wt% P(VDF–TrFE) in a methyl ethyl ketone solution was spin-coated on the sample to obtain 240 nm-thick polycrystalline P(VDF–TrFE) films. The composition ratio between VDF and TrFE of copolymer P(VDF–TrFE) is 70 : 30. The sample was baked on a hotplate at 90 °C for 30 min and annealed at different temperatures (120 °C, 125 °C, 130 °C, and 140 °C) for 2 h. The entire process of the P(VDF–TrFE) layer fabrication was completed in a nitrogen glove box. Finally, 50 nm-thick Au was thermally evaporated on the P(VDF–TrFE) layer at a low speed of 0.01 nm s^{-1} through a shadow mask to form the top-gate electrodes.

Fabrication of Au/P(VDF–TrFE)/Au capacitors

A 25 nm-thick Au electrode was thermally evaporated on the substrate with 10 nm InSiO on top. Then, the P(VDF–TrFE) layer was spin-coated on the InSiO films. Finally, the Au (30 nm) electrode was deposited on the ferroelectric layer through the shadow mask. The structure is shown in the inset of Fig. S1 (ESI†).

Fabrication of InSiO-based FETs

The heavily-doped Si wafer with 250 nm-thick SiO$_2$ on top was used as the bottom gate and dielectric. An InSiO film with a 10-nm thickness was deposited on the SiO$_2$ film by DC magnetron sputtering using the InSiO$_x$ target, and the weight ratio between

In$_2$O$_3$ and SiO$_2$ was 90 to 10. Then, the InSiO film was annealed at 250 °C for 30 min under ambient atmosphere. Finally, the source and drain electrodes of Au (30 nm) were deposited by thermal evaporation.

Fabrication of FETs using PMMA as the dielectric

An InSiO film with a 10-nm thickness were deposited on the SiO$_2$/Si substrate. After annealing for 30 min at 250 °C, the source and drain electrodes of Au (25 nm) were thermally deposited through a shadow mask. Then, 300 nm-thick PMMA was spin-coated to form the dielectric layer. Finally, the electrode, 30 nm-thick Au, was evaporated to fabricate the top-gate transistor.

Memory characterizations

Electrical performance was characterized under ambient conditions using an Agilent 4156C semiconductor parameter analyzer. The Agilent 4980a LCR parameter analyzer and HIOKI LCR IM3533-01 meter were used for the C–V measurements.

Results and discussion

Top-gate Fe-FET memories using P(VDF–TrFE) and InSiO as the dielectric and semiconductor layers, respectively, were fabricated (Fig. 1a). The channel length and width are 200 μm and 1000 μm, respectively. Fig. 1b presents a typical transfer curve as the gate voltage (V_G) is swept from −30 V to 30 V and then back. From the slope of the transfer curve, electron mobility is estimated to be as high as 84.1 cm^2 V^{-1} s^{-1} with the gate capacitance typically measured at a low-voltage-frequency state of 200 Hz. To estimate the carrier mobility, we selected the transfer curves when V_G was
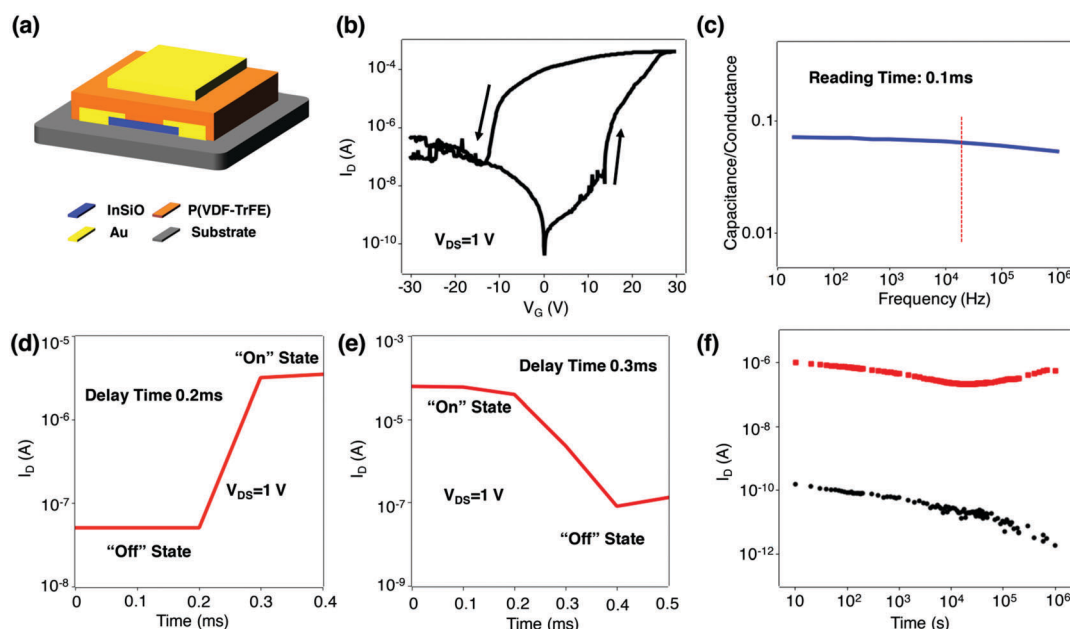
Fig. 1 (a) Schematic of a Fe-FET with a top-gate top-contact structure. (b) Typical transfer curve of the Fe-FET. For InSiO channel, after sputtering the InSiO film, the film was thermally annealed at 250 °C. (c) Dependence of capacitance divided by the channel conductance on V_G frequency. (d and e) Pulse responses of the Fe-FET memory from the off state to the on state and from the on state to the off state, respectively. (f) Shows that the retention measurements of on and off currents, indicating a good non-volatile property of our Fe-FET memories.

swept in a reverse manner from 25 V to 5 V, in order to avoid the switching process of the ferroelectric layer. Although there is a large ferroelectric hysteresis in the curve, both forward and backward curves showed large mobility. To the best of our knowledge, this value represents the highest mobility for Fe-FETs using P(VDF–TrFE) and amorphous oxide semiconductors.[7,8,26–29] The anticlockwise direction of the current hysteresis reveals that the charge-switching behavior is attributed to the dipolar polarization of P(VDF–TrFE) instead of charge trapping in the semiconductor layer.[30] Thus, when V_G is set to 0 V, our FET device exhibits two states with different electrical conductions, namely, the off and on states. Moreover, the on/off ratio and memory window obtained from the transfer curve were 10^6 and 27 V, respectively, which also denote good memory performance. Generally, a high carrier mobility in the semiconducting channel can lead to a fast operating speed, which is an important parameter for the evaluation of FET memory operation.[31] We performed a frequency response measurement to represent the "reading" process (Fig. 1c). The measurement shows a negligible decrease until the frequency increases to 10^4 Hz, indicating a short "reading" time of approximately 0.1 ms. Moreover, the abrupt switching of the drain current reveals a fast pulse response to the V_G pulse, which represents the "programming"

process (Fig. 1d and e). The pulse responses, as measured by adding a voltage pulse, show short delay times of approximately 0.2 and 0.3 ms from the off state to the on state and from the on state to the off state, respectively (Fig. 1d and e). The sub-millisecond delay time indicates a fast switching behavior close to the speed of the polarization switching of P(VDF–TrFE).[32,33] In addition, the sustainability of a memory operation is also an important feature for the industry. Fig. 1f shows the retention measurements of on and off currents for 10^6 s, indicating a good non-volatile property of our Fe-FET memories. A slight increase in the on current was observed from $\sim 10^5$ s, which can be attributed to the enhancement of the interaction between P(VDF–TrFE) and InSiO by Joule's heat. Besides, the devices can maintain a high on/off ratio of $>10^5$ after cycling 1000 times (see ESI,† Fig. S2).

As mentioned previously, the FET carrier mobility of our hybrid-memories is estimated in the linear region using the following equation:

$$\mu_{line} = \frac{Lg_m}{WCV_{DS}} \quad (1)$$

where μ_{line} is the linear-region field-effect mobility, W and L are the width and length of the semiconducting channel, respectively,
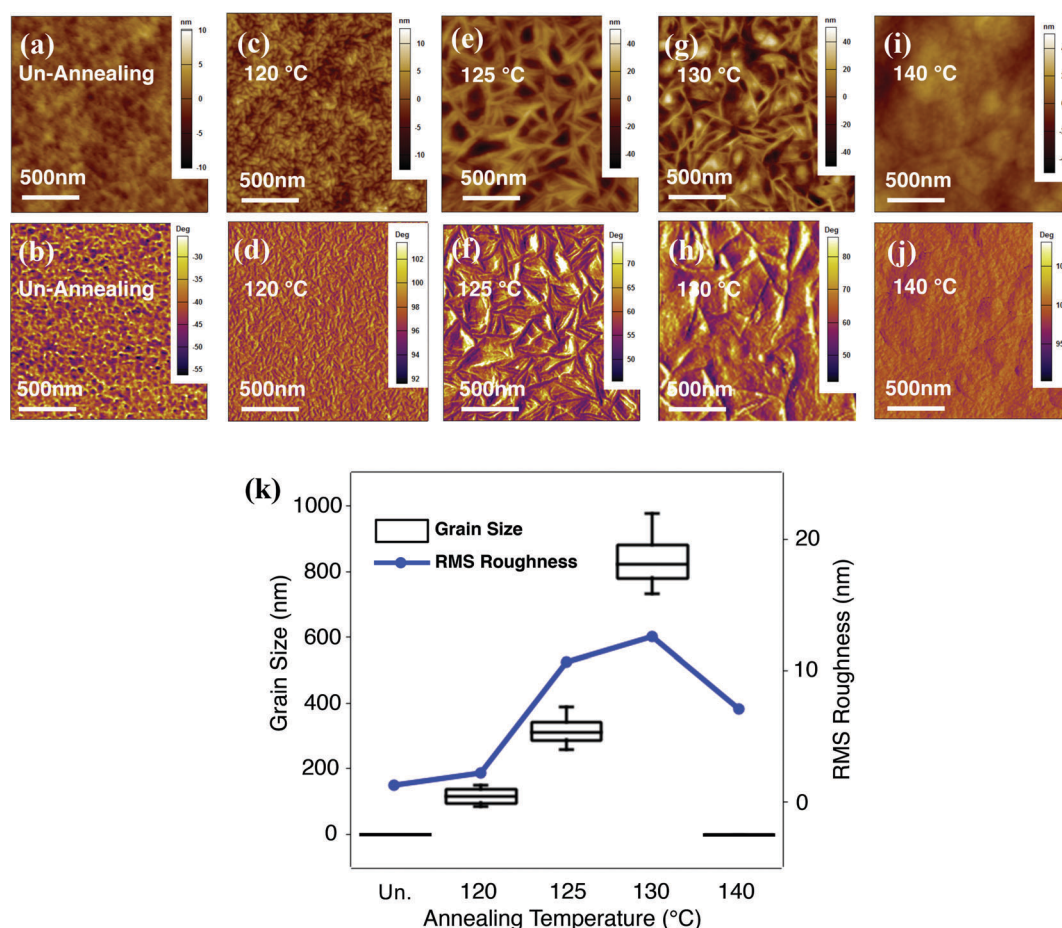

Fig. 2 (a–j) AFM morphology and phase images of P(VDF–TrFE) films deposited on InSiO layers with different annealing temperatures. (k) Root-mean-square roughness values and grain sizes of P(VDF–TrFE) films annealed at different temperatures.

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g_m is the transconductance of the transistor, V_{DS} is the drain voltage applied at 1 V, and C is the unit area capacitance of the gate insulator layer of P(VDF–TrFE). In measuring the capacitance (C) of P(VDF–TrFE), an Au/P(VDF–TrFE)/Au device was fabricated. The capacitance was measured by applying a sweeping voltage (from −30 V to 30 V and then back) at a low frequency of 200 Hz, and the spectrum exhibited a typical butterfly shape (see ESI,† Fig. S1). The capacitance represented irreversible ferroelectric polarization, in which dipole switching occurs in the bias voltages of approximately 10 and −10 V. Similar to most of the previous studies, this study estimated carrier mobility using the dielectric constant measured at a low voltage frequency of ≥ 20 Hz. Recently, studies have demonstrated that the capacitance of ferroelectric materials increased rapidly as the frequency decreased to < 1 Hz, and the extraction of carrier mobility should use the capacitance measured at the quasi-static frequency.[34] The studies also revealed that the typical procedure commonly used in the literature for mobility calculation utilizing a capacitance value measured at ≥ 20 Hz would result in an overestimated mobility.[34,35] Therefore, we also present the extracted mobility of 29.1 cm^2 V^{-1} s^{-1} using the capacitance measured at a quasi-static frequency of 0.1 Hz for voltage.

In our previous study, InSiO-based FETs using SiO$_2$ as the dielectric layer exhibited a significantly low carrier mobility of 7.7 cm^2 V^{-1} s^{-1} (the channel length and width were 350 μm and 1000 μm, respectively) when the ratio between In$_2$O$_3$ and SiO$_2$ was similar to that in the present Fe-FETs (also see ESI,† Fig. S3).[20]

Thus, we consider that the significant enhancement in the field-effect mobility of our Fe-FETs should be attributed to the interfacial effect between InSiO and P(VDF–TrFE). The ferroelectric property of P(VDF–TrFE) stems from the flexibility of the molecular axis, enabling change in the dipole moment direction. Ferroelectricity originates from the crystalline phase. Thus, the annealing treatment of P(VDF–TrFE) is necessary to increase the degree of crystallinity.[36,37] Therefore, we first examined the surface property of P(VDF–TrFE) under different annealing temperatures by using atomic force microscopy (AFM) measurements. Fig. 2a and b show the morphology and phase images of the P(VDF–TrFE) thin film without annealing treatment, respectively, and both exhibit an amorphous phase. The glass transition temperature of P(VDF–TrFE) is 118 °C.[31] Therefore, P(VDF–TrFE) film annealed at a temperature above this value forms highly crystalline phases with needle-like grains that enhance the ferroelectric property (Fig. 2c–h). Moreover, the grain sizes and surface roughness increase with the annealing temperature (Fig. 2k). As the annealing temperature further increases to the melting point of P(VDF–TrFE) (140 °C),[31] the film mainly exhibits an amorphous phase (Fig. 2i and j).

Subsequently, we investigated the electrical performances of our Fe-FETs under different annealing conditions. We fabricated 10 memories for the P(VDF–TrFE) layers annealed at different temperatures. The estimated FET mobility and memory window of the un-annealed memory are 0.79 ± 0.59 cm^2 V^{-1} s^{-1} and 6 ± 1 V, respectively (Fig. 3a). For the annealed sample, the carrier mobility
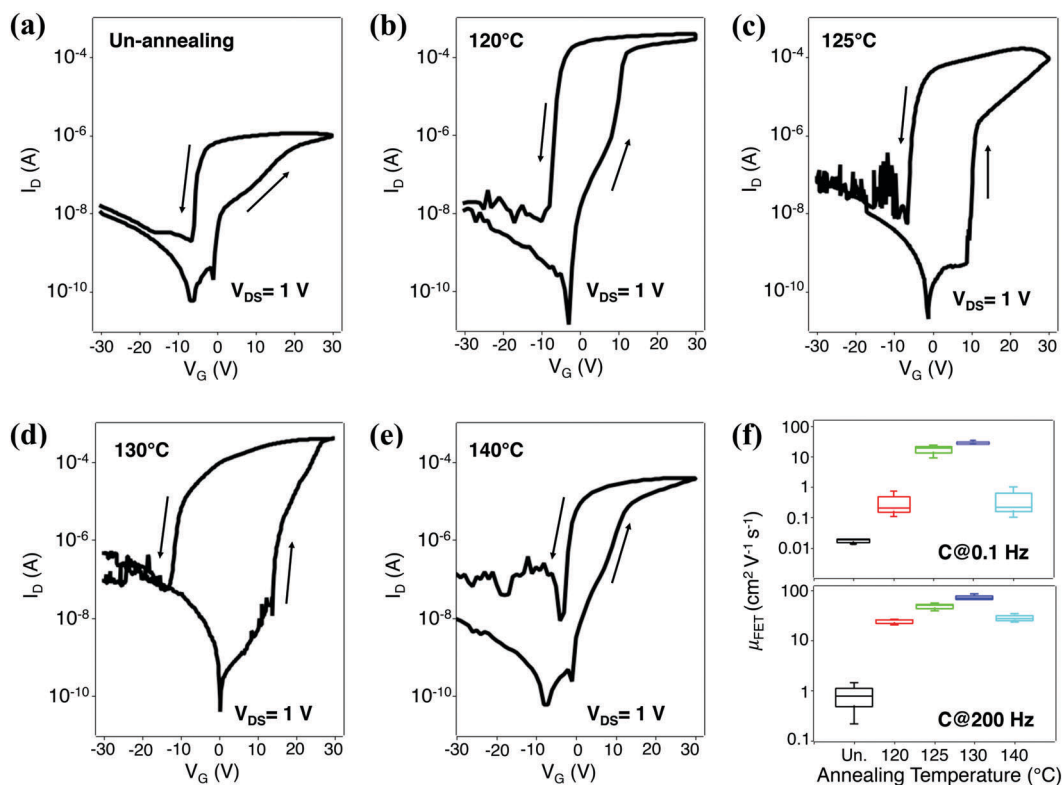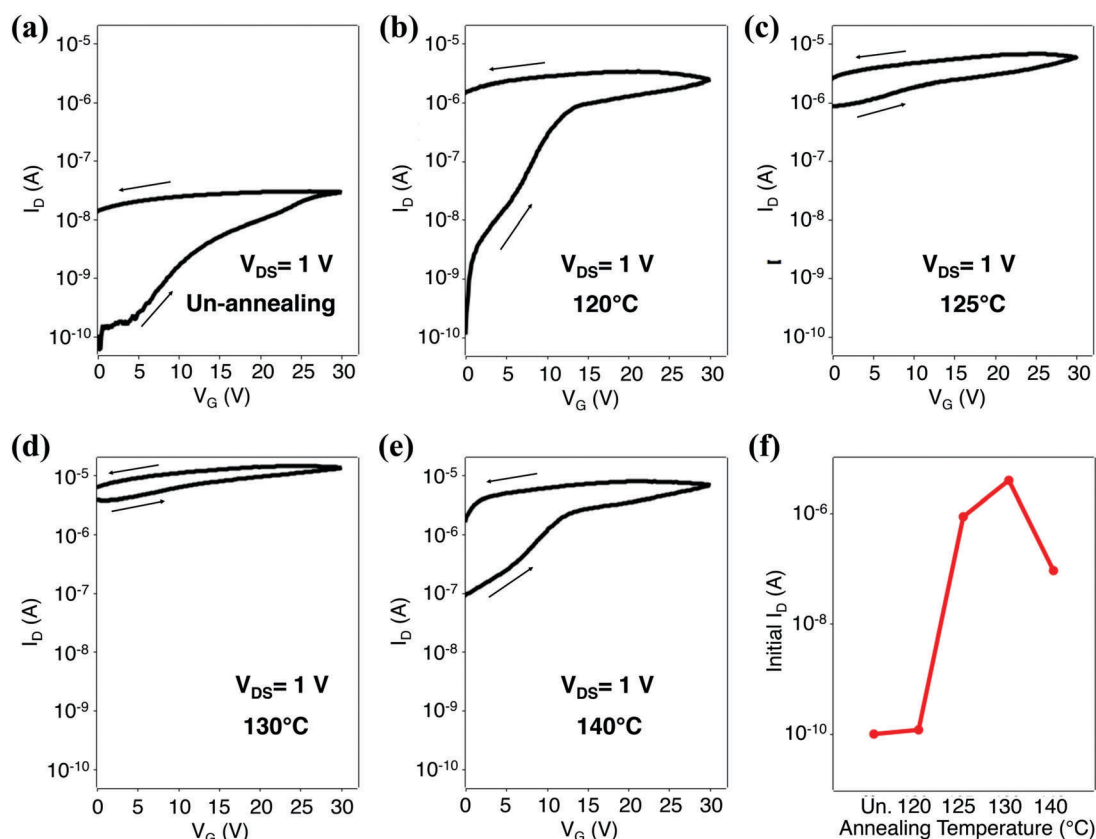

Fig. 3 (a–e) Transfer characteristics of Fe-FETs with different annealing conditions for P(VDF–TrFE). (f) Summary of the values of carrier mobility at different annealing temperatures.

and memory window were enhanced from 120 °C to 130 °C (Fig. 3b–d). In particular, the device annealed at 130 °C yielded an enhanced carrier mobility of 75.40 ± 9.54 cm^2 V^{-1} s^{-1} and a large memory window of 21 ± 6 V. The highest carrier mobility obtained was 84.1 cm^2 V^{-1} s^{-1}. Moreover, when the annealing temperature increased to the melting point of P(VDF–TrFE) at 140 °C, the carrier mobility and memory window decreased to 27.90 ± 5.42 cm^2 V^{-1} s^{-1} and 4 ± 2 V, respectively (Fig. 3e). Fig. 3f and Table S1 (ESI†) summarize the carrier mobility, on/off ratio, and memory window under different voltage frequencies for the capacitance measurements. In particular, the capacitance measurements showed a similar change in carrier mobility at a low frequency of 200 Hz and quasi-static frequency of 0.1 Hz. Consequently, the results strongly imply that the interfacial effect that exists at the ferroelectric/InSiO interface during the annealing treatment can improve the electrical characteristics of Fe-FETs.

For the InSiO semiconducting films, the conduction band where the electrons are transported is formed by unoccupied indium s orbitals, and the valence band is formed by fully occupied oxygen 2p orbitals.[38] The In atoms with dangling bonds, that is, V_O, have energy levels near the conduction band edge; these states act as shallow donors. Thus, the fully oxidized In atoms are regarded as insulators, and the In atoms with V_O

are utilized as conductors.[38] At the P(VDF–TrFE)/InSiO interface, charge transfer occurs, increasing the charge density (see ESI,† Fig. S4). Consequently, the polarization-bound charges in P(VDF–TrFE) will be screened by the mobile charges in InSiO, resulting in a charge accumulation layer at the surface of the semiconductor layer.[39] Therefore, the charge concentration in InSiO is increased, leading to a shift of the zero-gate-bias Fermi level toward the conduction band and to an enhancement in the electrical performance. In order to avoid the influence of the negative voltage on the charge distribution in the semiconductor channel, we examined the initial drain currents ($V_G = 0$ V) of as-fabricated Fe-FETs using P(VDF–TrFE) under different annealing conditions with the same structure to verify the results. The values of the initial drain currents were extracted from the transfer curves at the starting point of V_G sweeping (Fig. 4a–e). The high temperature applied during the annealing process can enhance the interfacial interaction between P(VDF–TrFE) and InSiO, leading to a high charge concentration in the conducting channel. As shown in Fig. 4f, the initial drain current increases from 10^{-10} A for the unannealed device to 10^{-6} A for the annealed device at 130 °C. The decrease in initial drain current for the device annealed at 140 °C is due to the loss of crystallinity in P(VDF–TrFE). Moreover, the change in the initial drain current along with the annealing temperature is similar to that

Fig. 4 To avoid the impact of the negative voltage on charge distribution in semiconductor channel, we examined the initial drain currents ($V_G = 0$ V) of as-fabricated Fe-FETs using P(VDF–TrFE) with different annealing conditions under the same structure. (a–e) Transfer characteristics of Fe-FETs with different annealing temperatures for P(VDF–TrFE), with V_G swept from 0 V to 30 V and then backwards. (f) Initial drain currents at the starting point ($V_G = 0$ V) of the V_G sweeping process for Fe-FETs with different annealing temperatures for P(VDF–TrFE).

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of carrier mobility, as shown in Fig. 3f. This indicates that the enhancement of electrical performance should be devoted to the interfacial interaction between P(VDF–TrFE) and InSiO. Finally, we further confirm this interfacial effect by fabricating top-gate devices using poly(methyl methacrylate) (PMMA) as the top-gate dielectric (see ESI,† Fig. S5). A typical transfer curve exhibited a value carrier mobility (10.1 cm^2 V^{-1} s^{-1}) similar to that of FETs using SiO_2 as the bottom-gate dielectric (9.1 cm^2 V^{-1} s^{-1}); and both are significantly lower than that of devices using annealed P(VDF–TrFE).

Conclusions

In summary, we fabricated a high-performance Fe-FET memory using InSiO and P(VDF–TrFE) as the semiconductor and dielectric layers, respectively. The interfacial interaction between the P(VDF–TrFE) and InSiO layers during the annealing treatment of P(VDF–TrFE) led to an increase in charge density in the conducting channel. A high mobility of 84.1 cm^2 V^{-1} s^{-1} in the low-frequency state was obtained. Based on the enhanced mobility, a fast operating speed was achieved for our Fe-FETs.

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