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Few-layered titanium trisulfide (TiS_3) field-effect transistors†

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Titanium trisulfide (TiS_3) is a promising layered semiconductor material. Several-mm-long TiS_3 whiskers can be conveniently grown by the direct reaction of titanium and sulfur. In this study, we exfoliated these whiskers using the adhesive tape approach and fabricated few-layered TiS_3 field-effect transistors (FETs). The TiS_3 FETs showed an n-type electronic transport with room-temperature field-effect mobilities of 18–24 $cm^2 V^{-1} s^{-1}$ and ON/OFF ratios up to 300. We demonstrate that TiS_3 is compatible with the conventional atomic layer deposition (ALD) procedure for Al_2O_3. ALD of alumina on TiS_3 FETs resulted in mobility increase up to 43 $cm^2 V^{-1} s^{-1}$, ON/OFF ratios up to 7000, and much improved subthreshold swing characteristics. This study shows that TiS_3 is a competitive electronic material in the family of two-dimensional (2D) transition metal chalcogenides and can be considered for emerging device applications.

The recently discovered remarkable properties of graphene stimulated interest in other two-dimensional (2D) atomic crystals.[1–3] Many of the actively studied 2D materials belong to the family of transition metal chalcogenides (TMCs).[4–6] A large number of TMCs in bulk form have a layered structure with weak interlayer van der Waals interactions.[2–6] The layers of TMCs can be exfoliated by different approaches to produce mono- and few-layered sheets that can be used for electrical and optical measurements.[1–7] So far, the experimental studies have been mostly focused on TMCs with MX_2 composition (M = Mo, W; X is a chalcogen), such as MoS_2, $MoSe_2$, WS_2 and WSe_2.[4,5] However, the TMC family is very rich and contains many other layered materials with interesting properties that have received limited attention from the researchers.[8,9]

One such TMC material is titanium trisulfide (TiS_3). In the bulk form, TiS_3 has been studied for several decades.[10–23] It was shown that millimeter-long whiskers of TiS_3 can be synthesized by a direct reaction of metallic titanium and elemental sulfur in evacuated ampules at 500–600 °C.[11,12,15,18,22–24] These whiskers were used for physical property measurements,[10,12,15,17,18,22,23] which revealed that bulk TiS_3 is an n-type semiconductor with an energy bandgap of about 1 eV,[10,12,17,22,23] and a room-temperature Hall mobility of about 30 $cm^2 V^{-1} s^{-1}$.[18]

While previous studies have mostly focused on the bulk properties of TiS_3, the introduction and extensive use of the micromechanical exfoliation approach[1] have opened the possibility of accessing the properties of monolayered and few-layered TiS_3 flakes. According to a recent theoretical study,[25] in a certain crystallographic direction a monolayer of TiS_3 is expected to have higher electron mobility than a single layer of MoS_2. An experimental attempt to exfoliate TiS_3 whiskers into few-layered nanoribbons and study their electronic and optoelectronic properties was reported by Island *et al.*[9] TiS_3 nanoribbons were shown to have high photoresponse and fast switching times, which makes nanostructured TiS_3 a promising material for applications in optoelectronics and photovoltaics.[9] However, the room-temperature charge carrier mobilities reported for the set of field-effect transistors (FETs) based on few-layered TiS_3 nanoribbons did not exceed 2.6 $cm^2 V^{-1} s^{-1}$,[9] while comparable bottom-gated FETs based on trilayered and thicker MoS_2, the most studied 2D TMC material, exhibited significantly higher mobilities of 10–20 $cm^2 V^{-1} s^{-1}$,[26,27] and reached up to 27 $cm^2 V^{-1} s^{-1}$ in devices with optimized contact resistances.[28] Therefore, in order to demonstrate that TiS_3 is a competitive TMC material for electronic applications, it is necessary to improve its field-effect mobility by at least an order of magnitude.

In this study, we report bottom-gated FETs based on few-layered TiS_3 nanoribbons that have room-temperature field-effect mobilities of 18–24 $cm^2 V^{-1} s^{-1}$. Furthermore, according to theoretical predictions, charge carrier mobilities of 2D semiconductor nanostructures can be significantly improved by modifying their dielectric environment.[29,30] Previously, the dielectric screening approach has been successfully applied to

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graphene[30,31] and MoS_2.[32–35] Here we demonstrate the validity of this approach for mobility improvement in few-layered TiS_3 FETs by coating the devices with a thin layer of a high-κ dielectric, Al_2O_3, which results in measured field-effect mobilities up to 43 $cm^2\ V^{-1}\ s^{-1}$ as well as much improved subthreshold swing (S) characteristics. These results demonstrate that TiS_3 is a competitive electronic material in the 2D TMC family and can be considered for emerging device applications.[3,4,6]

Following previous studies, we have grown TiS_3 whiskers *via* the direct reaction of titanium and sulfur.[11,12,15,18,24] In a typical synthesis, ~0.1 g piece of a 0.25 mm thick Ti foil and ~0.2 g of S are sealed in an evacuated ($p \sim 200$ mTorr) quartz ampule. The ampule is placed in a tube furnace, where it is heated up to 500 °C and annealed for 3 days. During the reaction sulfur exists in a gaseous phase, as can be seen by the orange-brown vapor inside the ampule (Fig. 1a); three pieces of Ti foil are indicated by the blue arrow. Fig. 1b demonstrates the optical photograph of the reaction ampule after the synthesis. The arrow (1) shows one of the pieces of Ti foil; it is covered by dense forest of TiS_3 whiskers that are typically 100–200 μm long. Interestingly, the whiskers grow not only on Ti foil, but also on the surface of the quartz ampule, as shown by the arrow (2) in Fig. 1b. These whiskers generally grow longer than the whiskers on Ti foil and often exceed 5 mm in length after 3 days of growth. At the end of the synthesis the ampule is moved away from the center of the furnace to create an ~100 °C temperature gradient, such that the end of the ampule containing the pieces of Ti foil remains at ~500 °C while the opposite end of the ampule is cooled below the boiling point of sulfur (444.7 °C). As a result, TiS_3 whiskers are cleaned from unreacted sulfur, which condenses in the cold end of the ampule. One hour later the ampule is cooled down to room temperature and TiS_3 whiskers are collected for materials characterization and electrical measurements.

Fig. 1c shows scanning electron microscopy (SEM) images at different magnifications of the TiS_3 whiskers grown on a Ti substrate. These whiskers have a shape of thin ribbons that are typically over 100 μm long, a few μm wide and less than half a micrometer thick; these dimensions are in accord with previously reported observations for similarly prepared samples.[9,22] The ribbon shape of TiS_3 whiskers is illustrated in the second panel of Fig. 1c, which shows several bent whiskers (two of them are indicated by the blue arrows). Additional SEM data for TiS_3 whiskers grown on a Ti substrate is provided in Fig. S1.† Based on the data presented in Fig. 1c, S1a† and similar SEM images we prepared a width distribution of TiS_3 whiskers, which is shown in Fig. S1b.† The size distribution is quite broad with a maximum at $w \sim 7$ μm; a substantial number of whiskers are wider than 20 μm. TiS_3 whiskers were also characterized by Raman spectroscopy; the results presented in Fig. S2† are in agreement with the previously reported data.[36]

For the device fabrication and electrical measurements we used TiS_3 whiskers grown on quartz (see the arrow (2) in Fig. 1b), which were easier to handle because of their larger size. The inset in Fig. 1d shows the optical microscopy image of one of these larger TiS_3 whiskers, which had a length of about 0.6 mm and a width of about 8 μm. This whisker was

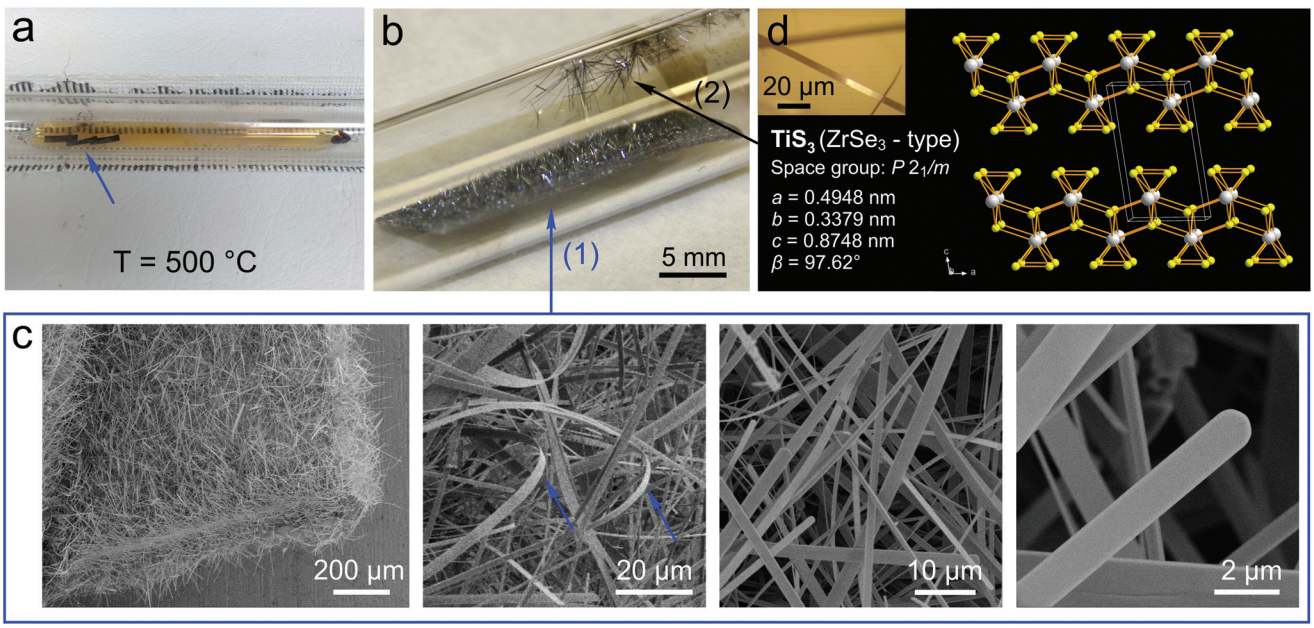

Fig. 1 Synthesis and characterization of TiS_3 whiskers. (a) Optical photograph of the reaction ampule during the synthesis. The ampule is filled with orange-brown sulphur vapour. The arrow shows three pieces of Ti foil. (b) Optical photograph of the reaction ampule after the synthesis. Arrows show (1) a piece of Ti foil covered with a forest of TiS_3 whiskers and (2) larger TiS_3 whiskers that have grown on the surface of quartz. (c) SEM images of TiS_3 whiskers grown on Ti foil, see (1) in panel (b), at different magnifications. The arrows in the second panel show bent TiS_3 whiskers. (d) Crystal structure of TiS_3 with the lattice parameters. Inset: optical photograph of one of the TiS_3 whiskers shown by the arrow (2) in panel (b).

studied by the single-crystal X-ray diffraction (XRD). A single crystal had a monoclinic symmetry with the space group $P2_1/m$ and lattice parameters a = 0.4948(7), b = 0.3379(5), c = 0.8748(12) nm, and β = 97.62(2)°. Direct methods yielded a completely ordered atom arrangement isotypic with the structure type of $ZrSe_3$;[37] the results of XRD measurements are summarized in Tables S1 and S2 in the ESI.† The crystal structure of TiS_3 can be described as a stack of 2D layers formed by one-dimensional (1D) chains of TiS_3 prisms, see Fig. 1d. TiS_3 can be viewed as $Ti^{4+}S^{2-}S_2^{2-}$, containing both sulfide and disulfide units; these units form trigonal prisms with Ti^{4+} centers.

For the device fabrication, one of the TiS_3 whiskers grown on a quartz surface was mechanically exfoliated using an adhesive tape[1] and transferred to a p-type silicon substrate covered with a 300 nm thick layer of SiO_2 (SQI). Because of the quasi-1D structure of TiS_3, the whiskers not only exfoliate into 2D sheets but also break longitudinally along the b-axis, resulting in thin TiS_3 nanoribbons that are much narrower than the original whiskers. Few-layered TiS_3 nanoribbons with thicknesses of 9–11 nm were found on the surface of a Si/SiO_2 substrate by optical microscopy. Electronic devices with few-layered TiS_3 nanoribbons bridging Cr/Au (3 nm/20 nm) electrodes were fabricated by standard electron-beam lithography followed by electron-beam evaporation; the details of the device fabrication and materials characterization can be found in the ESI.† The schematic of a typical TiS_3-based device with Cr/Au source (S) and drain (D) electrodes on a p^{++}-Si/SiO_2 substrate (the heavily doped p-type silicon was used as the back gate electrode, G) is shown in Fig. 2a.

Fig. 2b shows the SEM image of one of the four TiS_3 FETs that were fabricated and tested in this study; SEM and AFM images of other devices are shown in Fig. S3 in the ESI.† Fig. 2c shows the AFM image of the central portion of the TiS_3 nanoribbon channel of the device. The height profile measured across this TiS_3 nanoribbon shows a step of ~9.5 nm; see the black line in Fig. 2d. For comparison, we also show the height profiles measured for the other three devices (Fig. 2d) to demonstrate that all TiS_3 nanoribbons measured in this work had comparable thicknesses.

Electrical measurements of TiS_3 FETs were performed under vacuum ($p \sim 1 \times 10^{-6}$ Torr). Prior to the measurements the devices were evacuated for ~24 h to minimize the effect of surface adsorbates.[38] Fig. 2e shows that all four TiS_3 devices exhibited very similar electronic behavior. For all devices the drain–source current (I_{DS})–drain–source voltage (V_{DS}) dependencies at different gate voltages (V_G) were linear, indicating Ohmic contacts between TiS_3 nanoribbons and Cr/Au electrodes; a representative set of data for one of the TiS_3 FETs is shown in the inset in Fig. 2e. This figure also shows conductivity (σ)–gate voltage (V_G) dependencies for all devices, demonstrating the electronic behavior typical for FETs with n-type channels. These dependencies are also hysteretic, which is likely caused by the charge traps at the SiO_2/TiS_3 interface similar to SiO_2/MoS_2.[27] From the linear regions in the σ–V_G dependencies we estimate that the few-layered TiS_3 FETs have field-effect mobilities of 18–23 $cm^2\ V^{-1}\ s^{-1}$, which is comparable with the mobilities reported for few-layered MoS_2 devices.[26–28] The ON/OFF ratios defined as the ratios of the largest and smallest I_{DS} values in V_G dependencies were in the range of 30–300.

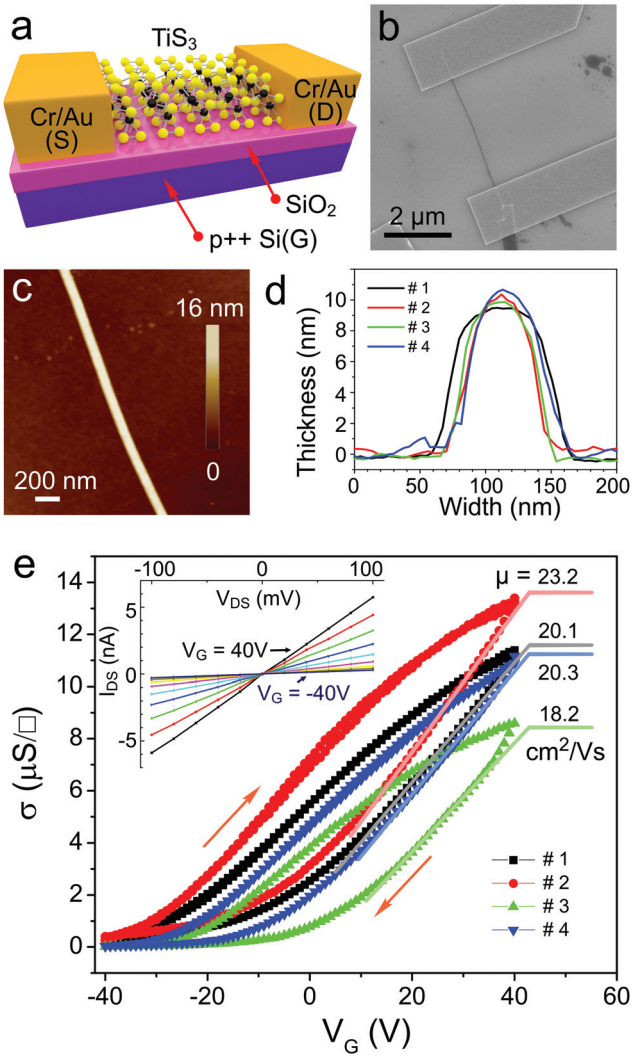

Fig. 2 Few-layered TiS_3 FETs. (a) Scheme of a TiS_3-based device on a Si/SiO_2 substrate; see text for details. (b) SEM image of a typical TiS_3 FET. Dark strip in the image is a TiS_3 nanoribbon that connects two Cr/Au electrodes. (c) Atomic force microscopy (AFM) image of the fragment of the TiS_3 nanoribbon shown in (b). (d) Representative height profiles measured across the TiS_3 nanoribbon shown in (c), see device #1, and three other TiS_3 nanoribbons used in this study; see text for details. (e) Conductivity (σ)–gate voltage (V_G) dependencies for all four TiS_3 FETs measured in this study. V_{DS} = 0.1 V. The mobility (μ) values are extracted from the linear regions (solid lines) in these dependencies. The inset shows drain–source current (I_{DS})–drain–source voltage (V_{DS}) dependencies for the device shown in panel (b) (device #1) measured at different V_G ranging from −40 to 40 V with a 10 V step.

The conductivities presented in Fig. 2e were measured using a two-contact method and therefore include a contribution from the contact resistances. In order to evaluate the intrinsic electronic properties of exfoliated TiS_3 whiskers we fabricated and tested two multiterminal devices and used

them for four-point probe conductivity measurements, see Fig. S4 and S5† and associated comments in the ESI.† The field-effect mobilities measured for multiterminal TiS_3 devices using a four-point probe method to exclude the contact resistance contribution were 21.1 and 24.2 $cm^2\ V^{-1}\ s^{-1}$. These values are in a great agreement with the mobilities measured for two-terminal devices (Fig. 2e). While a more detailed investigation of contact resistance effects could be the subject of a separate study,[39] our results show that contact resistances appear not to have a dominant effect on the electronic characteristics of TiS_3 FETs.

As we indicated earlier, dielectric screening is a very effective approach to improve charge carrier mobilities of 2D semiconductor nanostructures.[29–35] In order to demonstrate the effectiveness of this approach for the mobility enhancement in few-layered TiS_3 FETs, we used atomic layer deposition (ALD) to coat the devices with a 30 nm layer of Al_2O_3. Trimethylaluminum and water were used as Al_2O_3 precursors; additional details on ALD are given in the ESI.† Since TiS_3 has not been long considered as a material for electronics, nothing has been reported so far about its compatibility with conventional ALD procedures. For example, preparation of uniform dielectric layers on graphene has proved to be a challenge,[40–42] as graphene has no functional groups, which hinders the surface modification with common ALD precursors (the direct ALD of Al_2O_3 using the same precursors results in oxide nucleation only at the edges of graphene).[40] In contrast, the standard ALD procedure for Al_2O_3 growth worked well for TiS_3. Fig. 3a and b shows the same area of a TiS_3 nanoribbon channel of one of the devices before and after ALD of Al_2O_3, respectively. In the process, the color of the Si/SiO_2 substrate changed from purple to green. However, on the nanoscale the morphology of the TiS_3 nanoribbon and the substrate barely changed, suggesting a very uniform growth of Al_2O_3 by ALD (Fig. 3a and b). This conclusion is further confirmed by the representative height profiles shown in Fig. 3c. Before ALD of Al_2O_3 the height profile measured across the TiS_3 nanoribbon along the yellow line in Fig. 3a showed a step height of about 10 nm. After the growth of 30 nm of Al_2O_3 the height profile measured in the same place is nearly the same, suggesting that alumina layers of comparable thicknesses have grown on the TiS_3 and Si/SiO_2 substrate. Thus, this work demonstrates the compatibility of TiS_3 with conventional ALD procedures, which is important for the future studies of TiS_3 electronic devices.

Fig. 3d–g shows I_{DS}–V_G dependencies in linear and semi-logarithmic coordinates for two TiS_3 FETs before and after ALD of Al_2O_3; other devices showed similar behavior. These I_{DS}–V_G plots show that Al_2O_3 deposition may have different effects on the hysteresis of electronic transport observed in alumina-coated TiS_3 FETs. The Al_2O_3-coated device shown in Fig. 3d and e exhibits a considerable hysteresis, while in the other Al_2O_3-coated FET (Fig. 3f and g) the hysteresis visibly shrinks compared to the as-made TiS_3 FET before Al_2O_3 ALD. As in the case of as-made TiS_3 FETs we attribute this hysteretic behavior to interfacial charge trapping.[27] While we did not

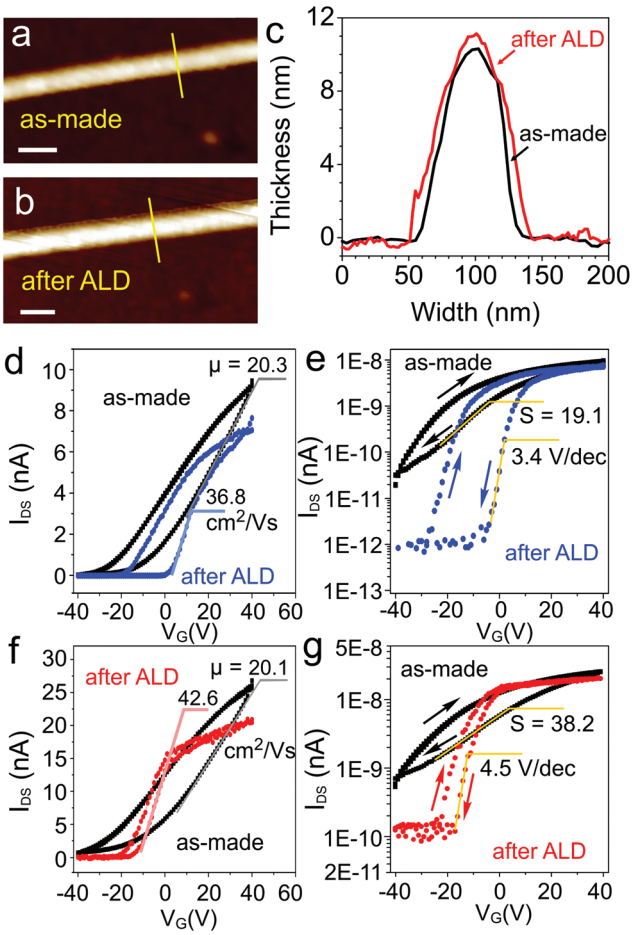

Fig. 3 ALD of Al_2O_3 on TiS_3 FETs. (a) AFM image of a fragment of TiS_3 nanoribbon channel of a device. (b) AFM image of the same area as in (a) after ALD of 30 nm of Al_2O_3. Scale bars in (a,b) are 100 nm. (c) Height profiles measured across the TiS_3 nanoribbon along the yellow lines in (a) and (b). (d, e) Comparison of the drain–source current (I_{DS})–gate voltage (V_G) dependencies for the same device (# 4) before and after ALD of Al_2O_3 shown in (d) linear and (e) semi-logarithmic coordinates. V_{DS} = 0.1 V. (f, g) Comparison of the drain–source current (I_{DS})–gate voltage (V_G) dependencies for another device (# 1) before and after ALD of Al_2O_3 shown in (f) linear and (g) semi-logarithmic coordinates. V_{DS} = 0.1 V.

investigate this effect in detail, it is interesting to note that the alumina or another high-κ dielectric layer on top of TiS_3 may provide another interface for charge-trap engineering. The data presented in Fig. 3d–g suggest that with a proper optimization of the deposition procedure it may be possible to either minimize the hysteretic behavior of TiS_3 FETs or create devices with large σ–V_G hysteresis loops, which may be of interest, for example, for memory applications.[43] The optimization of the ALD procedure using high-κ dielectrics, not limited to Al_2O_3, will be the subject of our future studies.

Other than the different features in the shape of I_{DS}–V_G hysteresis loops, the effect of Al_2O_3 deposition on the electronic properties of TiS_3 devices was quite consistent. Fig. 3d–g shows that the Al_2O_3 deposition has an overall positive effect

on the electronic properties of TiS_3 FETs. For the TiS_3 FET shown in Fig. 3d the dielectric screening resulted in the field-effect mobility improvement from 20.3 to 36.8 $cm^2\ V^{-1}\ s^{-1}$, and for the other device the mobility improved from 20.1 to 42.6 $cm^2\ V^{-1}\ s^{-1}$ (Fig. 3f). Interestingly, the Al_2O_3 ALD also improved the ON/OFF ratios of TiS_3 FETs, which can be seen in logarithmic I_{DS} coordinates (Fig. 3e and g). For the device shown in Fig. 3e, the ON/OFF ratio improved from 300 to 7100, and for the other device (Fig. 3g) it improved from 40 to 170. The other two Al_2O_3-coated TiS_3 FETs exhibited ON/OFF ratios of 155 and 180. The positive effect of alumina ALD on the device characteristics of TiS_3 FETs can be further illustrated by the subthreshold swing (S) change. As can be seen in Fig. 3e and g and S6,† the as-prepared TiS_3 FETs had S values ranging from 19.1 to 44.3 V dec^{-1}. After Al_2O_3 ALD the S values decreased to 3.4–4.8 V dec^{-1}; the S values for all four devices before and after alumina ALD are summarized in Fig. S6c.† With these device properties TiS_3 appears to be a promising electronic material that can be positively compared with other more intensively studied members of the 2D TMC family.[4]

In summary, we have fabricated few-layered TiS_3 FETs and tested their electronic properties. The TiS_3 FETs showed an n-type electronic transport with room-temperature field-effect mobilities of 18–24 $cm^2\ V^{-1}\ s^{-1}$ and ON/OFF ratios up to 300. We also demonstrate that TiS_3 is compatible with the conventional ALD procedure for Al_2O_3. ALD of alumina on TiS_3 FETs resulted in mobility improvement up to 43 $cm^2\ V^{-1}\ s^{-1}$ and ON/OFF ratios of up to ~7000; S values after Al_2O_3 ALD decreased from 19.1–44.3 to 3.4–4.8 V dec^{-1}. This study shows that TiS_3 is a promising 2D TMC material that can be further explored in the future device studies.

Note added in proof: After the submission of this paper we became aware of the recently published study, which shows that the TiS_3 growth temperature could be a promising tool to tune the material's morphology and electronic properties, possibly through the change in the concentration of sulfur vacancies.[44]

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