Single layer graphene nano-gaps are fabricated by applying the method of feedback-controlled electroburning to notched ribbon devices, which are plasma etched from CVD grown graphene that is wet-transferred onto pre-patterned metal electrodes. Electrical and structural characterizations show that nanometer size gaps form at the center of the notch. We have processed a total number of 1079 devices using this method with a fabrication yield of 71%. Our results demonstrate precise control over the size and position of the nano-gaps, and open up the possibility of graphene electrodes for large-scale integrated molecular devices.

Integrated circuits where each functional unit is formed by only one molecule will be the ultimate form of electronic device scaling. Experimental demonstrations of molecular device functionality include rectifiers,2,3 switches4 and transistors,5,6 and effects of quantum interference have been observed in a single molecule.7 To harness the full potential of individual molecules, technological progress towards robust and identical three-terminal devices is necessary, including alternative electrode materials that are stable at room temperature. Graphene is a promising candidate for the replacement of metal electrodes because of the high-temperature stability of the covalent bond-structure (the strongest C–C bond is the three fold coordinated sp2 bond in graphene), the ability to anchor diverse molecules covalently or using π–π stacking and the reduced screening of the gate-field due to the extreme thinness of the electrodes (a single atomic layer). Wafer-scale growth8 and integration of graphene with conventional silicon electronics9 have recently been demonstrated.

Recent studies have reported two distinct approaches towards the fabrication of graphene-based molecular junctions based on electroburning10,11 and plasma etching.12 The former approach relies on the current induced breakdown of graphene. The size of the nano-gaps can be controlled by either varying the partial pressure of oxygen11 or by feedback-controlled electroburning,10 a method similar to feedback-controlled electromigration.13,14 The feedback allows for precise control over the gap size which is typically 1–2 nanometers. Although the fabrication yield of electroburning is high (92%10 to 95%11), the position of nano-gaps fabricated is not well controlled due to the random nature of the electroburning process. The latter approach is based on plasma etching of chemical vapour deposition (CVD) grown graphene point contacts. Over-etching the lithographically defined pattern produces nano-gaps that are less than or equal to nanometer. The use of large area CVD graphene enables the fabrication of nano-gaps on a wafer scale with precise control over the position of the nano-gaps, however the yield of the plasma etched devices is only 33%. In this letter we present a method of fabricating arrays of single layer graphene nano-gaps that combines these two approaches and provides a viable route for achieving high-yield fabrication on a wafer scale.

The nano-gap fabrication strategy comprises a lithography process where the minimum feature size is 200 nm followed by a feedback-controlled electroburning process which results in 0.5–2.5 nm sized gaps. We have processed a total number of 1079 devices resulting in 776 nano-gaps. In this paper we characterized the devices before and after the electroburning process and studied the geometry of individual nano-gaps using atomic force microscopy (AFM). We have further investigated the nano-gap formation by modelling the current density in our device geometry.

We fabricated the graphene devices using a passive-first active-last process flow, where the graphene is transferred onto a pre-patterned silicon chip as illustrated in Fig. 1(a–d). This passive-first active-last fabrication process enables integration of graphene into conventional silicon logic circuits.9 Single layer graphene (SLG) was prepared using a 1% CH4:Ar gas mixture at atmospheric pressure on liquid copper in a CVD furnace at 1090 °C. This method produces large area single layer graphene.15 PMMA was spun across the SLG/copper stack...
condition, which is set at a drop $/C0$ the devices is ramped up at a rate of 0.75 V s$^{-1}$. Each chip contains 540 pairs of Cr/Au electrodes that were patterned using electron beam lithography and metal evaporation. After the SLG is transferred onto the metal electrodes it is p-doped, with holes being the majority carriers throughout the entire channel. When the source–drain voltage $V$ is increased, the current starts to saturate as the electrochemical potential at the drain end of the channel moves towards the Dirac point. At a particular voltage $V_{\text{sink}}$, the electrochemical potential at the drain end corresponds to the Dirac point resulting in a pinch-off at the drain contact. By increasing $V$ beyond $V_{\text{sink}}$ the pinch-off is moved through the channel until the entire channel switches to electron carriers and the current will increase again. The value for $V_{\text{sink}}$ is dependent on the relative position of the Fermi level from the Dirac point for the graphene electrodes, and is therefore dependent on the doping level. We observe a shift of $V_{\text{sink}}$ towards lower source–drain voltages with each electroburning voltage ramp event. We attribute this to the removal of residual resist from current annealing. The removal of residual resist shifts the Fermi level closer towards the Dirac point which corresponds to the shift of $V_{\text{sink}}$ towards lower voltages. This increase in conductance has previously been observed in electroburning of few-layer graphene flakes and is attributed to the removal of residual resist by Joule heating of the graphene. From the AFM image of the device in Fig. 3, it can be observed that close to the notched region, the graphene is much cleaner compared to regions further away. This is an indication of residual resist removal from current annealing during our electroburning process.

The geometry of the nano-gaps is characterized by measuring the current–voltage curves using the same setup used for the feedback controlled electroburning. Fig. 2 shows a typical $I–V$ trace of a SLG nano-gap after completion of the electroburning process, i.e. after the low-bias resistance becomes larger than $R_{\text{set}}$. The non-ohmic $I–V$ traces measured after the electroburning process are characteristic of transport through a single tunnel junction. The size of the tunnel-barrier can be estimated by fitting the $I–V$ traces to the Simmons model using the barrier height, width and asymmetry as fitting parameters. The controllability and reproducibility of the nano-gap fabrication process were investigated by fitting 307 devices to the Simmons model. The average gap-size of 140 devices that underwent the electroburning process with a stop condition $R_{\text{crit}}=300 \text{ M}\Omega$ is $d=1.42 \pm 0.56 \text{ nm}$. For the 167 devices that were processed with a stop condition $R_{\text{crit}}=500 \text{ M}\Omega$, the gap-size is $d=1.39 \pm 0.46 \text{ nm}$. 94.8% of 307 devices fitted return a gap size within the range of $0.5–2.5 \text{ nm}$, which make these graphene nano-gaps appealing for contacting single molecules in molecular devices. The average fitted barrier heights is $0.24 \pm 0.11 \text{ eV}$. Similar barrier heights have previously been observed in electroburned few-layer graphene nano-gaps and in electromigrated metal electrodes.

To further investigate the formation of the nano-gaps, we performed AFM on several devices after the electroburning
The electroburning process, Fig. 3(a and b), shows an AFM image of an electroburned nano-gap. The AFM images show that the nano-gap forms at the narrowest part of the notch. The formation of the nano-gap at the narrowest part of the notch can be understood from the fact that the current density, and therefore the Joule heating, will be largest at this point. We determine the breakdown current as the current at which the feedback heating, will be largest at the this point. We determine the breakdown current as the current at which the feedback heating, will be largest at the this point.

We have investigated the nano-gap formation by calculating the current density profile in the graphene notch. To calculate the current density \( \langle j \rangle = \nabla \rho(r) \), where \( \rho(r) \) is the charge density as function of position \( r \), the Laplace equation \( \nabla^2 \rho(r) = 0 \) was solved using conformal mapping (see ESI†). The current density is highest at the apex of the notch (see Fig. 3(c)), which is where experimentally observe the formation of the nano-gap. Fig. 3(d) shows the current flow around a crack extending from the apex of each notch, which was calculated using a Schwarz transformation. Since the current is forced to flow around the cracks, the current density is highest at the crack-tip. Once a crack forms at the apex of the notch, it is therefore expected to propagate through the material, rather than becoming wider, in accordance with our observations. Our calculations and experimental findings demonstrate the ability to lithographically control the position of the nano-gaps, which allows for the precise alignment of the nano-gaps with other lithographically defined structures.

We identified three ways in which the electroburning process can fail: (i) the current required to start the electroburning process is larger than the maximum current supplied by our voltage source; (ii) the feedback-control did not ramp the voltage back to zero fast enough, resulting in a nano-gap with an infinite resistance (> 100 GΩ); (iii) the feedback-control is too sensitive and ramps the voltage before electroburning occurs. Whereas the second and third failures are intrinsic to the feedback-controlled electroburning process, the first failure occurs if the lithographically defined notch is too wide. Because the first failure is not intrinsic to the electroburning process and could be overcome by using a different voltage source, we define the yield of the electroburning process by only considering those devices where the threshold current is within the range of our setup. Using this definition, we find that the yield of the electroburning process is 85%. The total fabrication yield is 71%.
In this work, we have demonstrated the large scale fabrication of CVD graphene nano-gaps with a yield of 71%, through a combined approach of conventional lithographically defined plasma etching and feedback-controlled electroburning. AFM images display a nano-gap located at the narrowest part of the graphene notch. Fits of $(I-V)$ data of 307 devices to the Simmons model yield a gap size of 0.5–2.5 nm for 94.8% of the devices. The ability to controllably fabricate and position nanogaps of 0.5–2.5 nm makes this technique an attractive technique for contacting single molecules with lithographically aligned gates. Our use of CVD graphene means that this technique can be scaled up using wafer-scale grown graphene. The passive-first-active-last process adopted in this technique enables integration into conventional silicon logic circuits. This scalable approach paves the way towards employing graphene electrodes for large-scale integrated molecular circuits.

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