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Recent progress in HfO_2-based ferroelectric devices with oxide semiconductor channels: a comprehensive review

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With conventional silicon-based devices approaching their physical scaling limits and traditional perovskite ferroelectrics facing complementary metal–oxide-semiconductor (CMOS) compatibility challenges, the development of alternative material integrations is essential for next-generation semiconductor systems. Among these, the synergistic integration of oxide semiconductors (OSs) with HfO_2-based ferroelectrics has emerged as a particularly promising approach, leveraging the superior interfacial properties, excellent uniformity, and compatibility with low-temperature fabrication processes inherent to OS channels. However, realizing the full potential of this technology requires a comprehensive understanding of its synergistic benefits across diverse applications and overcoming the challenges of scaling from individual devices to complex and large-scale arrays. In this review, we provide a comprehensive overview of recent progress in OS-based ferroelectric field-effect transistors (FeFETs) across five key application domains: flash memory, dynamic random-access memory (DRAM), neuromorphic computing, logic, and displays. We examine how the unique advantages of this integration address the fundamental limitations of conventional technologies in each area and conclude by discussing the remaining technical barriers and future research directions for practical implementation of the technology.

1 Introduction

The semiconductor industry has reached a pivotal inflection point as the scaling trajectory defined by Moore's law encounters fundamental physical limits. As device dimensions approach the atomic scale, silicon-based architectures face

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severe bottlenecks in scalability and performance, necessitating a paradigm shift toward alternative materials and non-conventional device geometries.[1–3]

These limitations are pervasive across the memory and logic landscapes: NAND flash is hampered by structural scaling and thermal budget constraints;[4–7] DRAM faces capacitor scaling hurdles that compromise retention characteristics; and logic devices are increasingly plagued by leakage currents (I_L) and stochastic variability.[8–10] Furthermore, the rise of edge computing and AI necessitates ultra-low power consumption and massive integration density-requirements that incumbent technologies struggle to satisfy.[3,11]

A transformative milestone occurred in 2011, when Böscke *et al.* reported robust ferroelectricity in Si-doped HfO_2.[12] This discovery was particularly significant as it demonstrated that ferroelectric behaviour could be elicited in a simple binary oxide through stabilization of the non-centrosymmetric orthorhombic phase ($Pca2_1$),[13,14] rather than requiring complex perovskite structures. Unlike conventional perovskite ferroelectrics such as $PbZr_xTi_{1-x}O_3$ (PZT) and $BaTiO_3$ (BTO)-which suffer from CMOS incompatibility, lead toxicity, and critical thickness limitation (>100 nm)[12,15–19] -HfO_2-based materials offer seamless integration into existing fabrication lines. Notably, HfO_2 maintains stable ferroelectric polarizations at ultrathin scales (2.9–4.5 nm), significantly undercutting the physical limits of the perovskite system.[12,20–26] The stabilization of this metastable o-phase is governed by a sophisticated interplay of factors, including dopant selection (*e.g.*, Zr, Al, Y, Si, and Gd),[13,27–30] electrode-induced mechanical strain (*e.g.*, TiN, W, or Mo capping)[31,32] and the precise modulation of oxygen vacancies (V_O).[33] Rigorous thermal processing is essential to navigate crystallization kinetics, bypassing the thermodynamically stable monoclinic phase in favor of the non-centrosymmetric structure.[34] Despite challenges such as "wake-up" effects and polarization fatigue,[35,36] the high coercive field (0.8–2.0 MV cm^{-1}) of HfO_2-based ferroelectrics enables a wide memory window (MW) even in scaled layers.[24–26,37] These attributes position HfO_2-based ferroelectrics as the leading candidates for next-generation non-volatile memory and logic applications.

Silicon-based ferroelectric transistors have faced fundamental material constraints that would limit their practical implementation. Despite extensive optimization efforts with HfO_2-based ferroelectrics, these inherent limitations have persisted, prompting the exploration of OS channels, which could offer a potential solution to circumvent these silicon-specific constraints through fundamentally different material properties and superior interfacial characteristics.

To address these silicon channel limitations, OSs such as InGaO (IGO), InGaZnO (IGZO), and InGaSnO (IGTO), among various others, offer fundamentally different material properties that address silicon-specific constraints (Fig. 1a and b). Silicon's sp^3 orbitals exhibit strong directional bonding, making carrier transport highly sensitive to bond angle variations.

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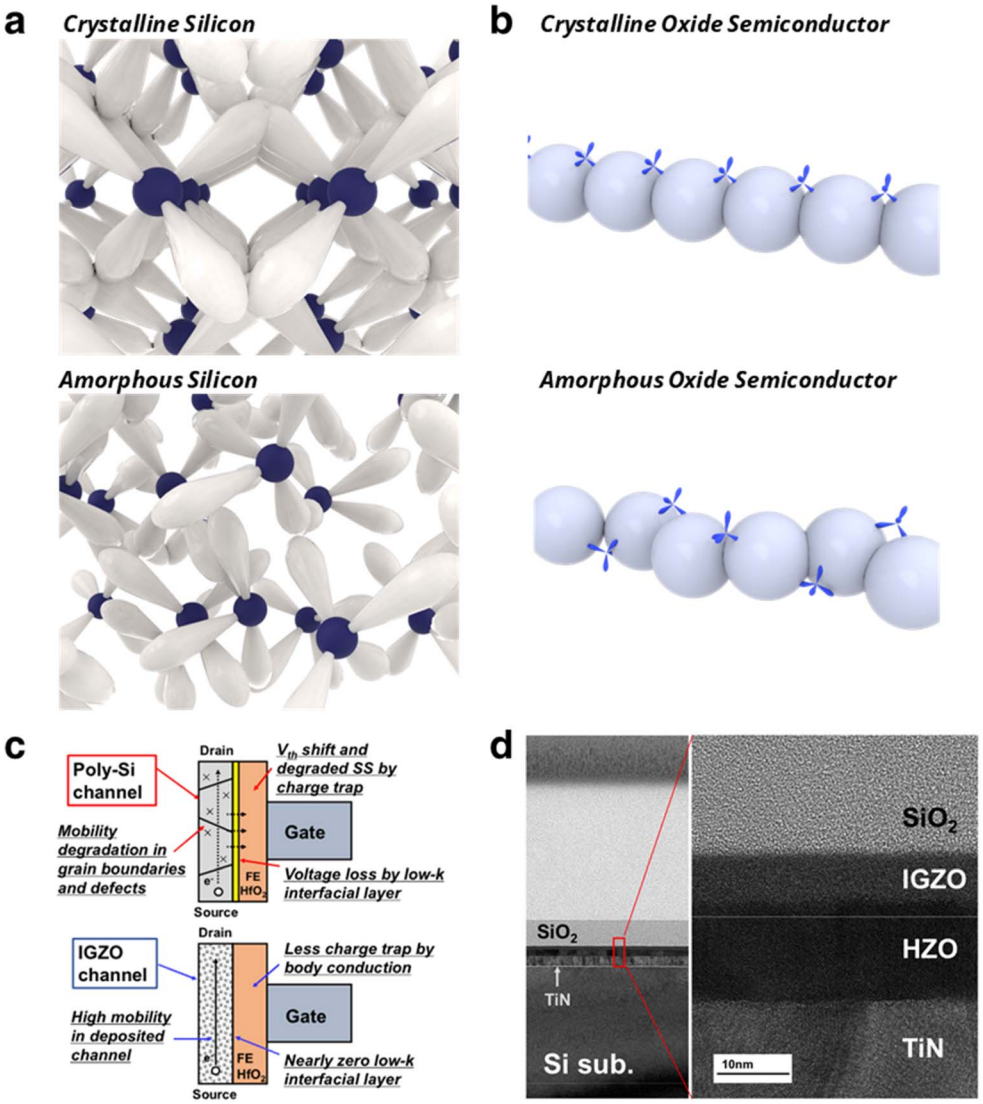

Fig. 1 Electronic structure and device characteristic comparison between Si and OS ferroelectric channels. (a) Orbital structures in Si channels. (upper) Crystalline Si showing highly directional sp^3 bonding. (lower) Amorphous-Si showing disrupted sp^3 bonds sensitive to structural disorder, causing mobility degradation and increased charge trapping. (b) Orbital structures in OS-based channels. (upper) Crystalline OSs. (lower) Amorphous OSs showing spatially extended metal ns-orbitals with isotropic symmetry, enabling high carrier mobility even in the amorphous state. (c) Schematic comparison between poly-Si channel and IGZO channel FeFETs. (d) Cross-sectional TEM images of the IGZO-based FeFET with no IL between IGZO and HZO.[13] Reproduced with permission from Mo *et al.*, *IEEE J. Electron Devices Soc.* **8**, 717 (2020). Copyright 2020 IEEE.

Grain boundaries (GBs) and structural disorder create localized trap states, limiting poly-Si to <100 $cm^2\ V^{-1}\ s^{-1}$ through GB scattering and charge trapping,[38] and *a*-Si to ~1 $cm^2\ V^{-1}\ s^{-1}$ *via* hopping-dominated transport.[39,40] In contrast, OSs employ spatially spread metal ns-orbitals with an isotropic shape that enable direct orbital overlap insensitive to bond distortions—a characteristic generic to multi-cation oxides with heavy post-transition metals ($n \geq 5$). This enables amorphous OSs to achieve 10–50 $cm^2\ V^{-1}\ s^{-1}$ mobility through band conduction without requiring crystallization.[39–44]

Regarding interfacial characteristics, silicon channels form SiO_x interfacial layers (ILs) during HfO_2 integration, causing voltage loss and retention degradation.[45] OSs, by contrast, exhibit negligible low-*k* IL formation with HfO_2-based ferroelectrics, minimizing voltage loss and preserving ferroelectric properties.[46] Furthermore, OS channels—particularly in the amorphous state—demonstrate superior large-area uniformity without poly-Si GB variability, while their low-temperature processing (200–400 °C) enables back-end-of-line (BEOL)-compatible monolithic 3D (M3D) integration compared to poly-Si (>600 °C).[47–50] OSs can be deposited through various methods including sputtering and atomic layer deposition (ALD), with tunable electrical properties achieved through composition control.[51,52]

These characteristics—including extremely low off-current (I_{OFF}) (<10^{-12} A μm^{-1}), large-area uniformity, and low-

temperature compatibility—make OSs particularly suitable for HfO_2-based ferroelectric devices where CMOS compatibility, 3D integration, and scalability are critical requirements.[47–50] The inherent composition tunability of OSs also offers potential for application-specific optimization, as the diverse requirements across NAND, DRAM, logic, neuromorphic, and display applications may benefit from different material properties.

The combination of OSs and HfO_2-based ferroelectrics offers pathways to address fundamental limitations of Si-based channels and conventional ferroelectric integration. While silicon channels suffer from IL formation and processing constraints that compromise device performance, OSs exhibit negligible IL formation with HfO_2-based ferroelectrics, leading to improved retention properties (Fig. 1c and d).[46,53] This integration enables low-power operation through the extremely low I_{OFF} of OS channels and negligible ILs that minimize voltage losses, as well as non-volatile characteristics that eliminate standby power consumption.

OS based FeFETs have been explored for diverse applications, with their potential for high-density 3D integration attracting significant attention. The emergence of advanced architectures, such as those for 3D vertical NAND (V-NAND) (Fig. 2a), stacked DRAM (Fig. 2b), and neuromorphic systems (Fig. 2c), underscores the critical need to understand the unique advantages of this integrated technology. Despite a wealth of literature dedicated to HfO_2-based ferroelectrics and OSs independently,[14,41,43,44,54–60] a significant knowledge gap persists regarding their combined implementation in FeFET technology. Given the rapid advancements in OSs as silicon channel alternatives,[61–65] a comprehensive review of OS-HfO_2 FeFET integration is timely and essential.[66] This work addresses this gap through systematic analysis across five key applications: NAND flash memory (Section 2.1), DRAM (Section 2.2), neuromorphic computing (Section 2.3), logic and computing applications (Section 2.4), and display technologies (Section 2.5). For each application, we provide quantitative performance comparison highlighting OS advantages over silicon-based devices, evaluate current progress against system-level integration requirements, and identify critical challenges for practical realization. Finally, in Section 3 (Perspectives and Future Directions), we discuss interface reliability mechanisms, channel engineering approaches, and material optimization directions for advancing of OS-FeFET technology.

2 Key applications of OS-FeFETs

2.1 NAND flash memory

Conventional floating-gate-based NAND technology has faced cell-to-cell interference due to increased parasitic capacitance[4,67,68] and increased I_L that resulted from reduced tunnel oxide thickness in sub-20 nm scaling.[5] Moreover, the polysilicon channels in 3D NAND have exhibited limitations including electrical characteristic non-uniformity due to grain boundaries[7] and requirements for high processing temperatures exceeding 900 °C.[6,69] Additionally, currently commercialized Quad-Level Cell (QLC) NAND requires four distinguishable threshold voltage states for 4-bit-per-cell storage, which necessitates sufficient MW and precise programming control.[70]

OS-based FeFETs have gained considerable attention as promising next-generation memory technologies that can provide pathways to overcome these bottlenecks. OS channels offer critical advantages for NAND application. While Si channels suffer from IL formation that would compromise retention characteristics, negligible IL formation with HfO_2-based

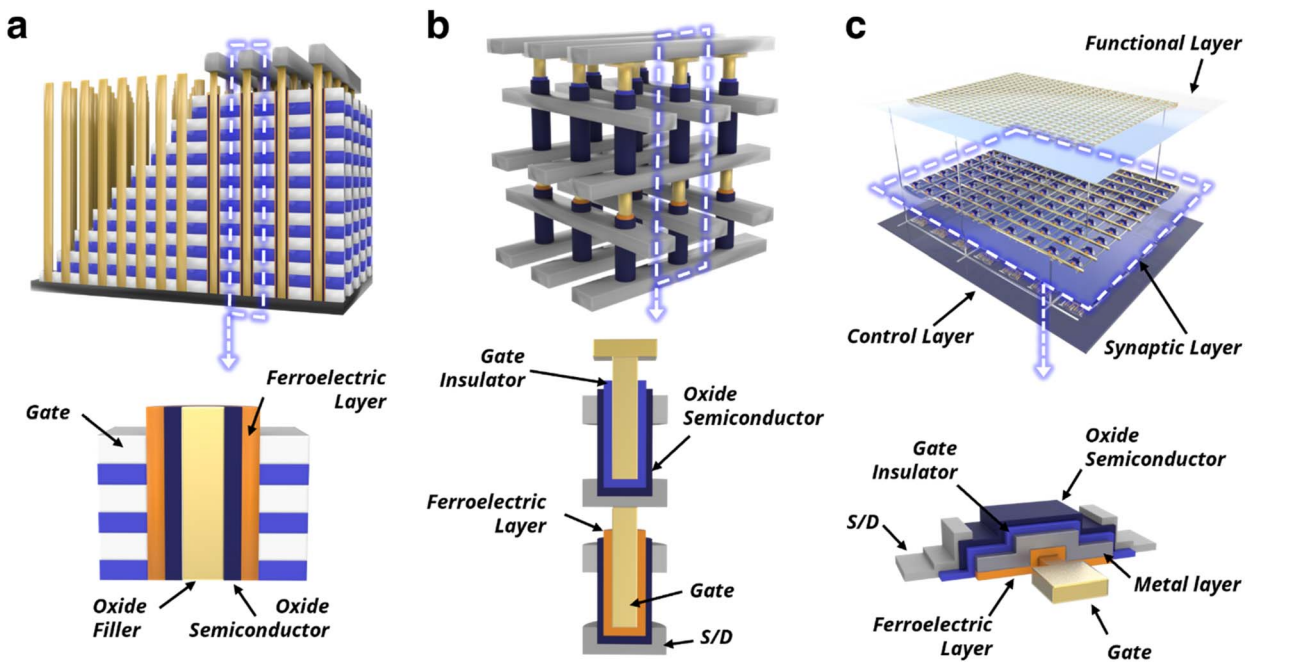

Fig. 2 Device schematics of (a) 3D Fe VNAND, (b) 3D Fe DRAM, and (c) FeFET-based neuromorphic computing architecture.

Table 1 Summary of device performance for OS-based ferroelectric NAND reported in the literature

Key feature	OS (deposition method)	Structure	MW (V)	*P*/*E* voltage (V)	Endurance	Retention	Ref.
Back gate control	IGZO (sputter)	MFS	0.5	2.5/−3	$>10^8$ (capacitor)	1 year (capacitor)	13
Vertical structure	IZO (ALD)	MFS	2.5[a]	5/−5	$>10^8$	N/A	79
Double gate structure	IGZO (sputter)	MIFSIM	5[b]	8/−8	$>10^4$	N/A	75
SCM and CDE	IZO (ALD)	MINFIS(IM)	14.3	20/−18	$>10^4$	10 years (ext.)	76
O-deficient and GIL	IGZO (sputter)	MIFS	17.8	11/−15	$>10^4$	$>10^3$ s	77
Separated write/read	Al:IZTO (sputter)	MFS	10	8	$>10^8$	$>10^5$ s	78
Gate stack engineering	Poly Si	GAA-MIFIS	13.2	19/−14	$>10^2$	10 years (ext.)	72

[a] Linear extrapolation. [b] Current constant method.

ferroelectrics in OS channels improves retention characteristics.[46] Furthermore, the IL-free structure, combined with the inherent uniformity of OS channels-arising from the isotropic nature of metal ns-orbitals-contribute to uniform device performance across large arrays.[41,71] While poly-Si FeFETs have demonstrated gate all around (GAA) configurations in 3D ferroelectric NAND (FeNAND) structures, they suffer from high operating voltages and severely limited endurance ($>10^2$ cycles).[72] In contrast, OS-based FeFETs achieve significantly lower operating voltages with endurance exceeding 10^4–10^8 cycles (Table 1). Consequently, OS-FeFETs have demonstrated not only low-voltage and high-speed operation but also endurance exceeding 10^8 cycles and scalability down to sub-10 nm nodes.

Despite their potential, early demonstrations of OS-FETs were hampered by a limited MW of ~0.5 V, uncovering fundamental challenges intrinsic to their operation.[46] Because OSs are predominantly n-type with a negligible concentration of minority holes,[43] erase operations-which typically necessitate polarization switching *via* hole accumulation-are fundamentally constrained. This scarcity of holes, exacerbated by the floating body effect, results in incomplete polarization erasure, thereby capping the overall device performance. While floating body phenomena limit the MW, substrate potential control using back gates was proposed to enable proper operation (Fig. 3a).[46] To address the erase operation limitations originating from insufficient hole carriers in n-type OSs, the insertion of a p-type CuO_x layer between the n-type channel and ferroelectric HZO was demonstrated to supply hole carriers, achieving a 4 V MW through enhanced polarization switching.[73] In addition, various structural approaches have been proposed to address these fundamental issues. Technology computer-aided design (TCAD) simulations comparing single-gate and double-gate configurations in both 2D and 3D structures demonstrated that the double-gate structure could effectively mitigate floating body effects and enable improved MW (Fig. 3b).[74] Subsequently, experimental demonstrations of the dual-gate structure confirmed enhanced performance through separated read/write operations (Fig. 3c).[75]

A device combining Source-tied Covering Metal (SCM) with Control Dielectric (CDE) achieved a 14.3 V MW (Fig. 3d).[76] Notably, the grounded SCM promotes hole accumulation during erase operations, whereas CDE extended the MW through voltage distribution during read operations, with retention remaining 11.5 V after 10 years. Furthermore, Samsung's research demonstrated a 17.8 V MW through gate stack and channel engineering (Fig. 3e).[77] This advancement incorporated an oxygen-deficient intermediate channel that enabled full-loop polarization switching and a gate interlayer (GIL) that enhanced the MW. With a sub-12 nm gate stack thickness and an operation voltage below 15 V, the device enabled high-density, low-power NAND applications. Moreover, a dual-port FeFET with Al-doped IZTO channels and separated write/read gates achieved a 10 V MW through a double-gate switching operation.[78] As a result, this approach enabled stable QLC programming and achieved negligible disturbance, which satisfied the core requirements for commercial NAND applications.

Beyond individual device optimization, ensuring reliable operation in large-scale 3D arrays represented a critical challenge for practical implementation. The feasibility of 3D FeNAND was investigated by demonstrating vertical FeFETs at the string level, with TCAD simulations confirming the viability of the 3D architecture (Fig. 3f).[79] Further progress was achieved by scaling the vertical FeFET gate length to 10 nm and demonstrating its string-level characteristics, with simulations confirming the viability of a 200-stack FeNAND structure.[80] Subsequently, recent systematic analysis demonstrated that disturb-free program operation can be achieved through optimized pass voltage below 2 V in both 2D and 3D arrays, with a SiO_2 interlayer thickness above 40 nm enabling interference-free operation in 3D configurations.[81]

A MW of up to 17.8 V has been achieved through various structural approaches, including dual-gate structures, SCM designs, dual-port configurations, and channel engineering (Table 1). These advances successfully addressed the fundamental challenges of the erase operation and enabled QLC programming with a disturb-free operation. However, the critical challenge lies in transitioning from optimized individual devices to reliable high-density 3D array architectures that can compete with commercial NAND requirements exceeding 200 layers. Poly-Si FeFETs have already achieved GAA configurations in 3D FeNAND structures but suffer from high operating voltages and severely limited endurance ($>10^2$ cycles). OS-based FeFETs have addressed voltage and endurance limitations through low-voltage operation with 10^4–10^8 cycle endurance,

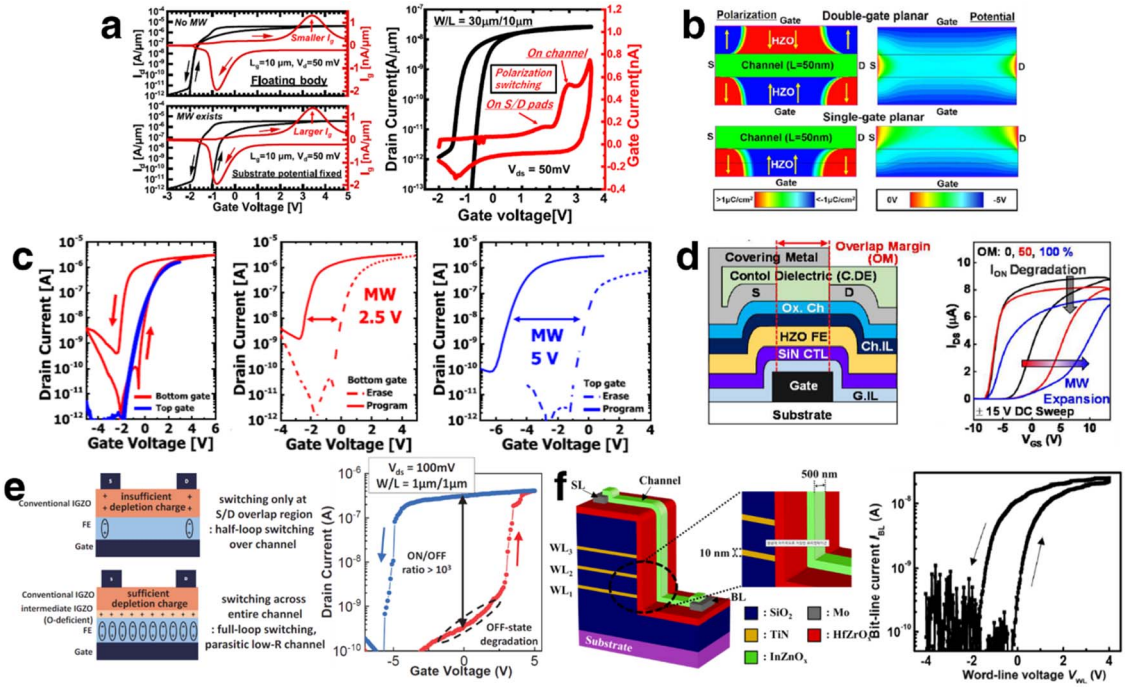

Fig. 3 (a) Simulated I_d–V_g and I_g–V_g characteristics of the IGZO FeFET with and without a top gate. Measured I_d–V_g and I_g–V_g characteristics of the IGZO FeFET with a top gate. Polarization switching in the IGZO channel is confirmed by the displacement current peaks in I_g.[46] Reproduced with permission from Mo *et al.*, *IEEE J. Electron Devices Soc.* **8**, 717 (2020). Copyright 2020 IEEE. (b) Comparison of TCAD simulated ferroelectric polarization charge and electrostatic potential for double gate planar and single gate planar FeFETs.[74] Reproduced with permission from Mo *et al.*, *Jpn. J. Appl. Phys.* **61**, SC1013 (2022). Copyright 2022 The Japan Society of Applied Physics. (c) I_d–V_g characteristic comparison between bottom-gate and top-gate operation and an extracted MW of 2.5 V (BG) and 5 V (TG).[75] Reproduced with permission from Jeong *et al.*, *IEEE Electron Device Lett.* **44**, 749 (2023). Copyright 2023 IEEE. (d) Gate stack schematic of the proposed FeNAND cell with an SCM structure. I_d–V_g characteristics for different SCM overlap margins (0, 50, and 100%).[76] Reproduced with permission from Joh *et al.*, *2024 IEEE Int. Electron Devices Meet. (IEDM)*, **1** (2024). Copyright 2024 IEEE. (e) Schematic illustration of full-loop switching enabled by the intermediate oxygen-deficient IGZO layer. I_d–V_g characteristics of the device with a 3 nm GIL[77] Reproduced with permission from Yoo *et al.*, *IEEE Symp. VLSI Technol. Circuits*, **1** (2024). (f) Schematic of a nanoscale vertical FeTFT array and I_{BL}–V_{WL} transfer characteristics showing ferroelectric hysteresis. V_{WL} was swept on the selected WL electrode while $V_{PASS} = 2$ V was applied to unselected WL electrodes.[80] Reproduced with permission from Kim *et al.*, *Appl. Phys. Lett.* **121**, 042901 (2022). Copyright 2022 AIP Publishing.

while inherent wide bandgap properties provide ultra-low I_L (<10^{-12} A μm^{-1}). However, substantial challenges remain in experimental demonstration of vertical GAA architectures, validation of disturb-free operation in high-density multi-string arrays, and systematic characterization of device-to-device variability across large-area substrates for practical implementation.

2.2 DRAM

Conventional one-transistor-one-capacitor (1T1C) DRAM has faced two critical challenges: capacitor scaling limitations and refresh power consumption. As the capacitor thickness approached ~5 nm, the capacitance reduction from 20 fF to 8 fF degraded the retention and sensing margins.[8–10,82–84] Additionally, the 64 ms retention time required frequent refresh operations that dominated power consumption.[82,84] Two-transistor capacitor-less (2T0C) DRAM, which eliminated the capacitor and stores charge directly in the channel region, emerged to address capacitor scaling. This architecture achieved $4F^2$ area efficiency and dramatically extended retention (400–1000 s) compared to 64 ms.[85–87] In 2T0C, the write transistor (Wtr) needs ultra-low I_{OFF} to suppress I_L during retention, while the read transistor (Rtr) needs high I_{ON} for adequate sensing margin. Table 2 summarizes how OSs provide ultra-low I_{OFF} and Si provides high on current (I_{ON}) for these respective roles. Heterogeneous approaches (Si–MoS_2[88] and IGZO-Si[89]) extended retention to 4800–6000 s. Ferroelectric integration with OSs can employ permanent polarization states to overcome retention limitations, demonstrating refresh-free DRAM.

Ferroelectric integration, which transformed 2T0C into non-volatile 2T0C ferroelectric DRAM (FeDRAM), directly addressed this remaining limitation. The ferroelectric layer enabled permanent polarization states that removed the need for refresh operation. Furthermore, OS-based channels, which provided extremely low I_L and superior HfO_2 interfacial properties, were particularly suited for this integration, enabling stable non-volatile switching. Consequently, this integration approach addressed both original challenges: where capacitor scaling was addressed through structural elimination, and refresh power was removed through non-volatile operation.

Stackable vertical channel-all-around (CAA) structure IGZO FeFETs were investigated through TCAD simulations, which

Table 2 Summary of device performance for OS-based DRAM and FeDRAM reported in the literature

	OS (deposition method)						
Device architecture	Wtr	Rtr	Area per transistor	MW (V)	Rtr I_{ON} (μA μm^{-1})	Retention	Ref.
Planar 2T0C DRAM	IGZO (sputter)		Planar	[a]	~10 (V_{DS} = 0.8 V)	~1000 s	85 and 86
Vertical 2T0C DRAM	IGZO (ALD)		4F^2	[a]	30 (V_{DS} = 1 V)	300 s	87
2T0C FeDRAM (simulation)	IGZO		4F^2	1.76	~1 (−)	N/A	90
2T0C FeDRAM (experimental)	*a*-ITZO (sputter)	*a*-ITZO/*a*-IGZO (sputter)	Planar	1.5	~1 (V_{DS} = 0.1 V)	>2000 s	91
2T-eDRAM	Si	MoS_2 (CVD)	Planar	[a]	165.97 (V_{DS} = 3 V)	~6000 s	88
2T0C DRAM	*a*-IGZO (sputter)	Si	Vertical (3D)	[a]	~1.19 (V_{DS} = 1 V)	~4800 s	89

[a] Non-FeFET device

addressed array-level operation challenges.[90] The study demonstrated a 10^7 on/off ratio ($I_{ON/OFF}$), and the proposed methodology resolved current-sharing issues (Fig. 4a). Moreover, the optimized operation achieved current ratios exceeding 10^5 between the data states while preventing readout interference (Fig. 4b).

Subsequently, the first operational 2T0C FeDRAM using *a*-ITZO FET and *a*-ITZO/*a*-IGZO FeFET was demonstrated.[91] The device achieved a 1.5 V MW with 10^4 s retention (Fig. 4c). Notably, the Rtr exhibited >10^6 $I_{ON/OFF}$ with a stable 19-level multi-bit operation (Fig. 4d), with a 11.5 V MW retention extrapolated after 10 years.

The evolution from 1T1C DRAM to 2T0C addressed capacitor scaling through structural elimination, achieving a 4F^2 area efficiency and extended retention (400–1000 s). Ferroelectric integration further removes the refresh power requirements through non-volatile operation. The demonstrated 2T0C-FeDRAM achieved a 1.5 V MW with 10^4 s retention, >10^6 $I_{ON/OFF}$, and 19-level multi-bit operation with 11.5 V retention extrapolated after 10 years (Table 2). The 2T0C architecture requires ultra-low I_{OFF} for the Wtr to minimize I_L and high I_{ON} for the Rtr to ensure the sensing margin—properties naturally provided by OSs and Si, respectively (Table 2). Heterogeneous approaches (Si–MoS_2 and IGZO-Si) combined these

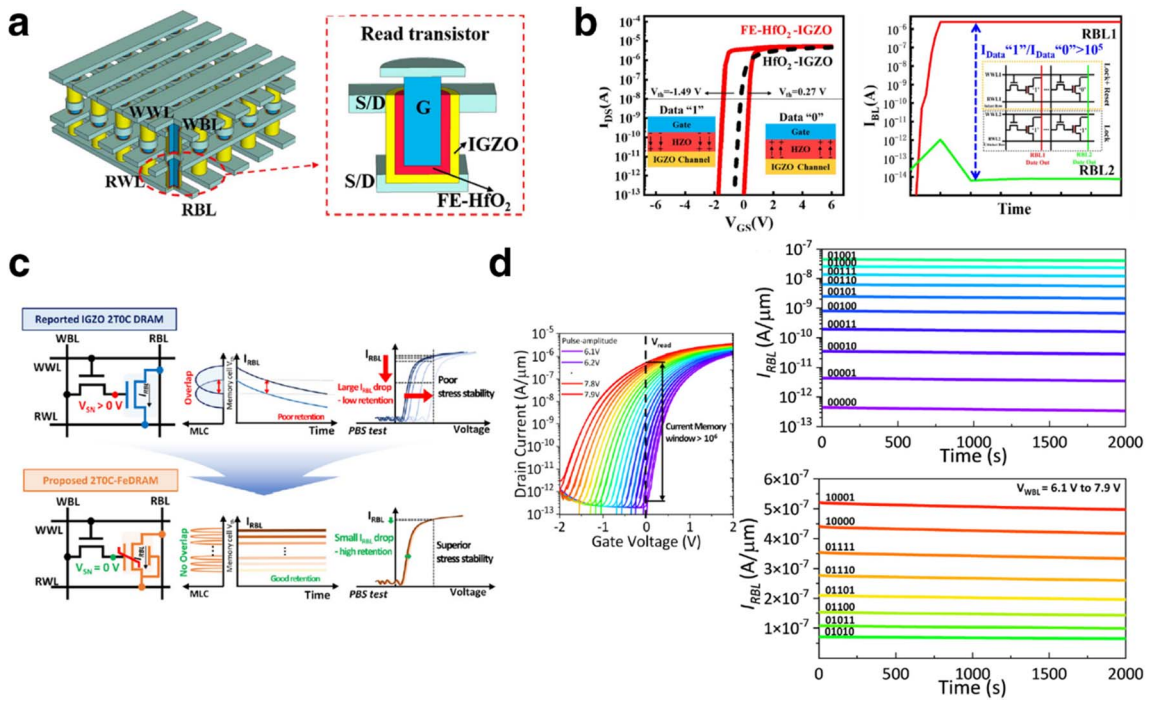

Fig. 4 (a) Schematic of stacked 2T0C memory with CAA-IGZO FeFETs and cross sectional view of the Rtr with ferroelectric HfO_2 (b) Simulated I_d–V_g characteristics comparing IGZO-based FeFETs (red) and conventional IGZO FET (black dashed). Selective readout of RWL1 with an ultra-high current ratio (>10^5) between data "1" and data "0". Unselected cells (RWL2) remain locked, preventing readout interference.[90] Reproduced with permission from Liang *et al.*, *Jpn. J. Appl. Phys.* **63**, 06SP05 (2024). Copyright 2024 The Japan Society of Applied Physics. (c) Schematic comparison of read/write operations in conventional 2T0C DRAM and proposed 2T0C FeDRAM, highlighting programmable V_{TH} (V_{SN} = 0 V operation), non-overlapping I_{RBL} for multi-bit storage, and enhanced stress stability. (d) I_d–V_g characteristics of the Rtr showing >10^6 current MW at V_{read} = 0 V. Retention characteristics demonstrate stable 19-level memory states over 2000 s.[91] Reproduced with permission from Noh *et al.*, *Nanoscale* **16**, 16576 (2024). Copyright 2024 Royal Society of Chemistry.

complementary characteristics, utilizing OSs for low-leakage retention and Si for high-current sensing, achieving 4800–6000 s retention. Ferroelectric integration with OS channels addressed volatility through permanent polarization, demonstrating a 1.5 V MW with 10^4 s retention, $>10^6$ $I_{ON/OFF}$, and 19-level multi-bit operation. However, demonstrations remain at the discrete device level. Progression to array-level feasibility faces critical challenges: current-sharing issues degrade read margins, cross-talk affects multi-cell operations, and the fundamental retention-write speed trade-off—where extended retention requires slower polarization switching—complicates optimization. Validating extrapolated 10-year retention in integrated arrays under realistic conditions remains essential, with cell area *versus* leakage management becoming increasingly critical at scaled dimensions.

2.3 Neuromorphic computing systems

FeFETs exploit HfO_2 polarization to modulate channel conductance, yet poly-Si FeFETs suffer from interface-related instabilities that compromise synaptic precision. In contrast, OS-based FeTFTs provide stable interfaces that enable reliable analog weight updates crucial for neuromorphic learning.[46] As summarized in Table 3, poly-Si FeFETs exhibit a limited conductance dynamic range ($G_{max}/G_{min} \approx 10$) and restricted weight resolution (5-bit), indicating a fundamental trade-off between programming speed and analog controllability.[92]

For neuromorphic applications, critical synaptic functionalities are enabled by OS-based FeFETs: analog weight modulation through partial polarization switching and stable multi-level conductance states essential for neural network operations.[93–96] In contrast, OS-based FeTFTs demonstrate significantly expanded conductance windows (G_{max}/G_{min}: ~50–1400) and enhanced conductance levels exceeding 70 states with up to 8-bit precision.[97] Partial polarization switching generates multiple intermediate states, enabling multi-level conductance modulation (Fig. 5a).[98] This property extends beyond binary memory operation, establishing itself as an analog synaptic device capable of continuous weight modulation, a fundamental requirement for neuromorphic computing. The metal–ferroelectric–metal–insulator–semiconductor (MFMIS) structure introduces an insulating layer and floating metal between the ferroelectric and channel, suppressing interfacial reactions and enabling optimized capacitance matching.[59,99] The MFMIS structure enabled enhanced performance in synaptic applications. The device stack consisting of an IGZO channel, ZrO_2 insulating layer, Mo electrode, and HZO ferroelectric layer ensures efficient coupling of ferroelectric polarization while minimizing interface trap effects (Fig. 5b).[100,101] Low nonlinearity ($\alpha \approx 0.21$), wide G_{max}/G_{min} (≈ 53.2), and highly stable updates with a cycle-to-cycle variation of only ~0.47% were achieved.[101] Crucially, precise analog weight modulation enabled by the MFMIS structure realized a robust analog reservoir computing system, achieving high performance in tasks such as temporal data prediction.[100] This capability is further supported by retention measurements, which demonstrate that multiple programmed states remain stable for over 10^3 s (Fig. 5c),[100] confirming that the MFMIS FeTFT is well-suited for long-term analog weight storage in neuromorphic systems.

FeTFT synaptic arrays enable vector-matrix multiplication (VMM) operations, which are fundamental computations for neural networks.[102] By applying input voltages to the word lines and bit lines and summing the output currents along the source lines, parallel in-memory computation can be achieved (Fig. 5d). Inhibit voltages were applied to unselected cells to suppress unwanted polarization switching, thereby enabling precise cell-level control. The biasing scheme demonstrated that the targeted cells exhibited conductance modulation, whereas the non-selected cells remained unchanged.

3D stacked FeTFT arrays, which address area limitations and sneak-path current issues, have emerged as an essential approach for overcoming the constraints of conventional 2D planar architecture.[103] The structural configurations are composed of TiN, HZO, InZnO (IZO), and Mo layers forming vertically stacked FeTFT cells with independent access (Fig. 5e). A six-layer stacked array has been reported to reach ~93.1% accuracy on Modified National Institute of Standards and Technology (MNIST) digit classification, closely approaching software-level performance.[103] Moreover, hafnia-based FeFET arrays have demonstrated >90% accuracy on CIFAR-10 image classification,[104] evidencing that 3D stacking not only enhances integration density but also provides practical feasibility for deep-learning inference. An endurance exceeding 10^6 cycles and retention over 10^4 s have been confirmed, underscoring the reliability required for large-scale neuromorphic hardware.

Table 3 compares the reported performance. Poly-Si FeFETs exhibit limited G_{max}/G_{min} (≈ 10) and restricted weight resolution (5-bit), indicating a fundamental trade-off between programming speed and analog controllability. In contrast, OS-based FeTFTs demonstrate significantly expanded G_{max}/G_{min} (~50–1400) and enhanced conductance levels exceeding 70 states with up to 8-bit precision. OS-FeFET synaptic devices

Table 3 Summary of device performance for OS-based FeFETs for neuromorphic computing reported in the literature

OS (deposition method)	Structure	G_{max}/G_{min}	Conductance levels	Accuracy	Pulse width	Read bias	Ref.
IZTO (sputter)	MFS	11	64	93.1% (MNIST)	100 μs	$V_{DS} = 0.1$ V	96
IGZO (sputter)	MFS	>10	64	91.1% (MNIST)	50 ms	$V_{DS} = 0.1$ V	98
IGZO (sputter)	MFMIS	~53.2	>70	~97% (MNIST)	100 μs	$V_{DS} = 1.0$ V	100
IGZO (T-ALD)	MFMIS	~183	N/A	> 90% (CIFAR-10)	10 μs	$V_{DS} = 0.1$ V	101
IGZO (sputter)	MFMIS	~1400	256 (8-bit)	96.6% (MNIST)	100 μs	$V_{DS} = 0.1$ V	97
Poly-Si (LPCVD)	MFS	9.96	32 (5-bit)	N/A	150 ns	$V_{DS} = 0.1$ V	92

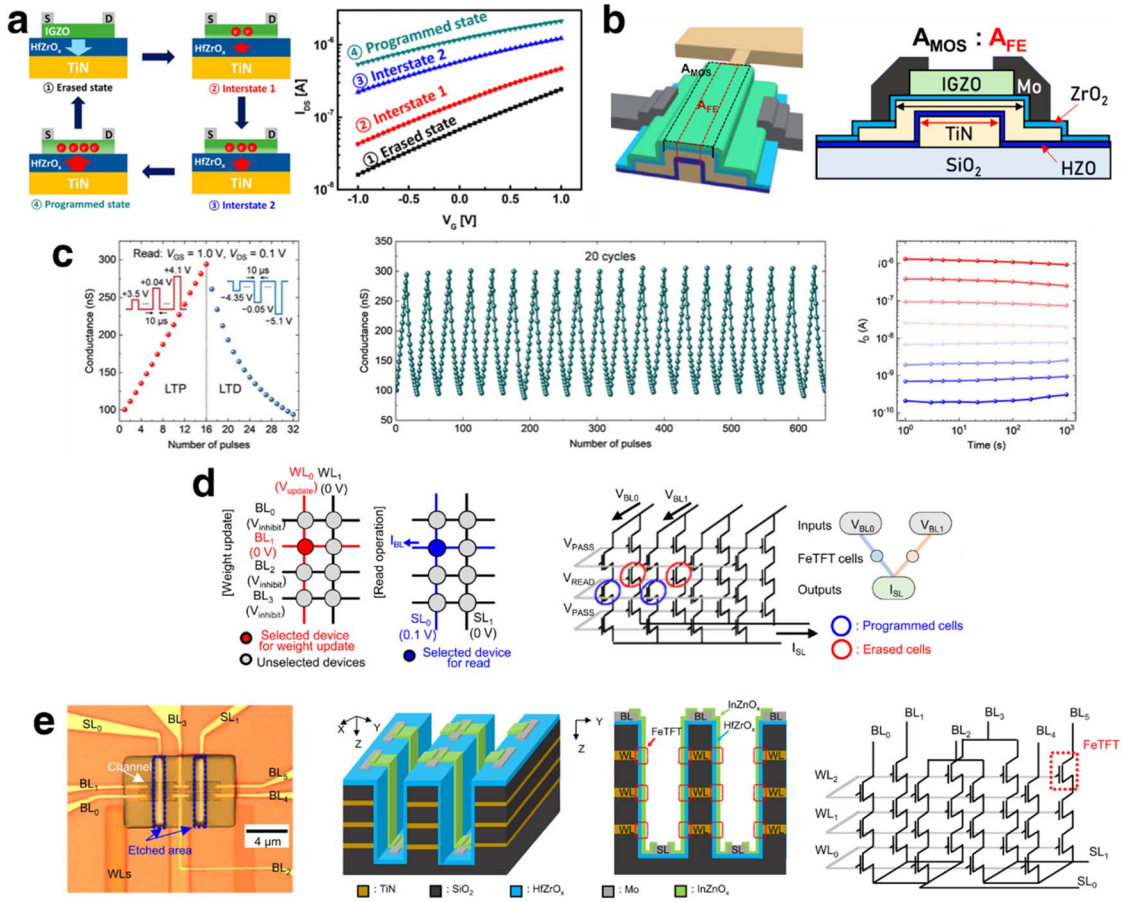

Fig. 5 (a) Schematic of ferroelectric polarization states (erased, programmed, and intermediate states) and corresponding transfer curves demonstrating multiple intermediate conductance levels.[98] Reproduced with permission from Kim and Lee, *Nano Lett.* **19**, 2044 (2019). Copyright 2019 American Chemical Society. (b) Three-dimensional device structure and cross-sectional schematic of the MFMIS FeTFT showing the IGZO channel, ZrO_2 interlayer oxide, TiN inner metal, HZO ferroelectric layer, and Mo gate electrode.[101] Reproduced with permission from Kwon *et al.*, *Adv. Intell. Syst.* **5**, 2300125 (2023). Copyright 2023 Wiley-VCH GmbH. (c) LTP and LTD characteristics, conductance modulation stability over 20 cycles, and retention measurements showing multi-level state stability over >10^3 s.[100] Reproduced with permission from Kim *et al.*, *Nat. Commun.* **15**, 9147 (2024). Copyright 2024 Springer Nature. (d) Biasing schemes for selective weight update and read operations with inhibit voltage control, and schematic of VMM operation demonstrating programmed and erased cell states for neuromorphic computing. (e) Optical microscope image of the fabricated 3D FeTFT array, three-dimensional schematic of vertically stacked layers, and equivalent circuit diagram showing WL, BL, and SL interconnections.[103] Reproduced with permission from Kim *et al.*, *Nat. Commun.* **14**, 504 (2023). Copyright 2023 Springer Nature.

achieved precise analog weight modulation (nonlinearity $\alpha \approx 0.21$, G_{max}/G_{min} ($\approx$53.2) and demonstrated functionality in 3D stacked arrays with vector-matrix multiplication operations, achieving >90% accuracy on MNIST and CIFAR-10 benchmarks. Six-layer stacked arrays have achieved ~93.1% MNIST accuracy approaching software performance.

However, scaling to large-scale systems faces critical challenges. Device-to-device and cycle-to-cycle variation impact weight accuracy in arrays, while the fundamental trade-off between analog weight precision and programming endurance—where higher-resolution multi-level states exhibit reduced cycling stability—complicates optimization. Further scaling beyond current 6-layer demonstrations would encounter wire resistance and cross-talk challenges, while endurance limitations (10^4–10^6 cycles) constrain on-chip learning operations that require frequent weight updates. Long-term retention validation beyond 10^3 s and balancing weight retention *versus* update speed for learning remain essential. As neuromorphic hardware remains pre-commercial, system-level development including peripheral circuits, power management, and manufacturing scalability is required for practical deployment.

2.4 Logic and in-memory computing applications

2.4.1 Content-addressable memory (CAM). Traditional static random-access memory (SRAM)-based CAM has fundamental limitations in area and power efficiency with a 16-transistor structure and standby power consumption.[105] Si-based TCAM implementations exhibit restricted $I_{ON/OFF}$ (~10^4) due to a narrow bandgap (1.12 eV); furthermore, poly-Si variants are hindered by high-temperature processing requirements and poor uniformity (Table 4).[106–108] In contrast, FeFET-based approaches offer significant area reduction and lower operation power compared to SRAM.[105,106,109,110] Combined with OS channels, which enable precise content matching through

Table 4 Summary of device performance for OS-based FeFETs for logic applications reported in the literature

Application	OS (deposition method)	Structure	MW (V)	Endurance (cycles)	Retention	I_{ON}/I_{OFF}	Ref.
TCAM	Al:IZTO (sputter)	MFMIS	3.2	10^6	10^5 s	$\sim10^5$	106
TCAM	IGZO (sputter)	MFMIS	2.9	$>10^8$	10 years (ext.)	$\sim10^8$	107
CECAM	IGZO (ALD)	MFMIS	2.2	10^4	10^4 s	$\sim10^6$	113
TCAM	Si	MFIS	1.1	N/A	N/A	$\sim10^4$	108
M3D	IGZO (sputter)	MFS	1.7	$>10^6$	10^4 s	$>10^5$	116
M3D	ITO-IGZO (sputter)	MFS	2	$>10^7$	10 years (ext.)	$\sim10^6$	117 and 118
M3D	In_2O_3 (ALD)	Vertical MFS	1.88	$>10^{12}$	10 years (ext.)	$\sim10^7$	120
M3D	Poly-Si	MFMIS	2.5	$\sim10^6$	10^5 s	$\sim10^4$	114

consistent switching behaviour, ferroelectric non-volatility allows architectural simplification from 16T SRAM to 1FeTFT-1T structures while achieving extremely low standby power.[111]

BEOL-compatible TCAM using the MFMIS structure achieved a 2.9 V MW with a 40 nm channel length, 10^8 cycle endurance and 8 orders $I_{ON/OFF}$, enabling a larger sensing margin than conventional designs, with 90.4% handwritten digit recognition accuracy in artificial intelligence (AI) applications (Fig. 6a).[107,112] Focused microwave annealing (FMA) based processing at 250 °C enabled BEOL-compatible M3D integration with $2P_r$ 22.5 μC cm^{-2} and 10^8 cycle endurance, achieving high density using single transistor area compared to 12T silicon TCAM (Fig. 6b).[106] Combinatorial encoding CAM (CECAM), which addressed limitations of bit-by-bit storage through combinatorial encoding, achieved 0.75 bit/switch content density with 65% power reduction using the 12-IGZO based FeFET structure storing 9-bit words (Fig. 6c).[113]

2.4.2 Monolithic 3D integration. Poly-Si requires high-temperature processing (600–1000 °C) for dopant activation and defect annealing, exceeding BEOL thermal limits (<400 °C).

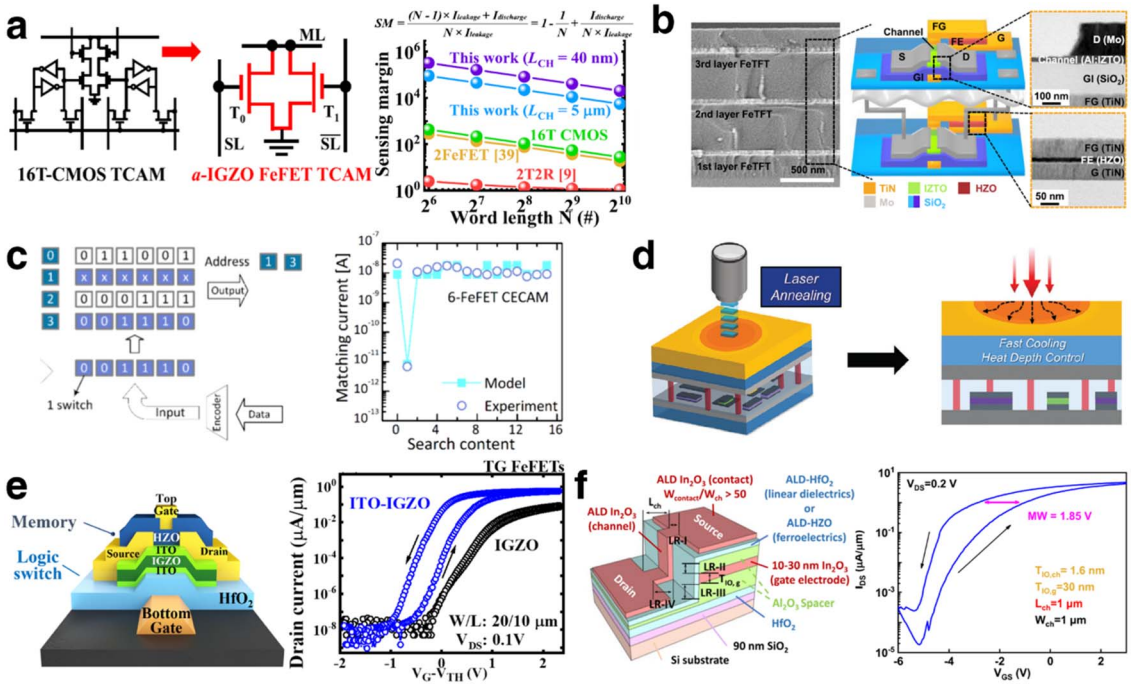

Fig. 6 (a) Schematic comparison of conventional 16-transistor CMOS-based TCAM and two-FeFET TCAM, with sensing margin comparison showing superior performance at reduced word length.[107] Reproduced with permission from Sun *et al.*, *IEEE Trans. Electron Devices* **69**, 5262 (2022). Copyright 2022 IEEE. (b) SEM images of FMA-processed multilayer FeTFT integration (1st, 2nd, and 3rd layer FeTFTs) and 3D schematic with cross-sectional TEM images showing vertical M3D integration.[106] Reproduced with permission from Joh *et al.*, *ACS Appl. Mater. Interfaces* **15**, 51339 (2023). Copyright 2023 American Chemical Society. (c) CECAM access method schematic demonstrating input/output operations and matching current *versus* search content for 6-FeFET CECAM.[113] Reproduced with permission from Nguyen *et al.*, *ACS Appl. Electron. Mater.* **7**, 2404 (2025). Copyright 2025 American Chemical Society. (d) Schematic of heat distribution in multi-layer devices through laser annealing.[116] Reproduced with permission from Kim *et al.*, *Adv. Sci.* **11**, 2401250 (2024). Copyright 2024 Wiley-VCH GmbH. (e) Schematic of the double-gated FeFET structure with memory and logic switching capability, and I_d–V_g characteristics for comparing top-gated ITO-IGZO and IGZO FeFETs.[118] Reproduced with permission from Chen *et al.*, *IEEE Trans. Electron Devices* **70**, 2098 (2023). Copyright 2023 IEEE. (f) 3D schematic of the vertical all-oxide FeFET showing a detailed layer structure including link regions with varying electrostatic control, and bi-directional I_d–V_g characteristics demonstrating a 1.85 V MW at V_{DS} = 0.2 V.[119] Reproduced with permission from Lin *et al.*, *IEEE Trans. Electron Devices* **71**, 7984 (2024). Copyright 2024 IEEE.

Laser annealing enables sub-500 °C processing but yields limited $I_{ON/OFF}$ ($\sim 10^4$) with increasing multi-layer complexity (Table 4).[114] In contrast, OS channels enable BEOL-compatible M3D through low-temperature processing (<400 °C) while maintaining performance.[115] Nanosecond pulsed laser annealing enabled selective crystallization of HZO-IGZO while maintaining the bottom layer temperature below 250 °C, achieving $>10^6$ cycles of endurance, a retention over 10^6 s, and a $>10^5$ $I_{ON/OFF}$ ratio (Fig. 6d).[116] ITO-IGZO heterojunction FeFETs utilizing channel defect self-compensation, which passivated interface/bulk defects, achieved enhanced performance through low thermal budget processing at 380 °C (Fig. 6e).[117,118] The top-gated and double-gated structures were enabled with 68 mV dec^{-1} subthreshold swing, endurance exceeding 10^7 cycles, retention longer than 10 years, and an $I_{ON/OFF}$ ratio of $\sim 10^7$, demonstrating BEOL compatibility for non-volatile logic integration in M3D architectures. Vertical all-oxide FeTFTs using degenerated In_2O_3 for both gate and source/drain electrodes demonstrated metallization-free processing over 400 °C at 1.88 V with 10^{12} cycle endurance, 10-year retention, and $I_{ON/OFF}$ above 10^7 (Fig. 6f).[119] The M3D-FACT architecture with a three-layer structure comprising Si CMOS control logic, analog resistive RAM (RRAM)-based compute-in-memory (CIM) units, and a IGZO FeTFT-based reconfigurable datapath achieved a 15F^2 cell area, representing a 40× area reduction compared to the 7 nm SRAM.[120] CNN benchmarks demonstrated an energy efficiency improvement of 6.9× for VGG-8, 19.2× for DenseNet-121, and 9.9× for ResNet-18 compared to conventional structures.

Si-based TCAM shows low $I_{ON/OFF}$ ($\sim 10^4$) from a narrow bandgap, while poly-Si additionally requires high-temperature processing (600–1000 °C) exceeding BEOL limits, with laser annealing achieving sub-500 °C but maintaining limited $I_{ON/OFF}$ ($\sim 10^4$). In contrast, OS-FeFETs have demonstrated architectural simplification in CAM applications, achieving an area reduction from 16T SRAM to 1FeTFT-1T structures with 0.75 bit/switch content density. OS-based devices achieve high $I_{ON/OFF}$ (10^5–10^8) compared to Si devices ($\sim 10^4$) with a demonstrated endurance up to 10^8 cycles (Table 4). For M3D integration, various approaches, including low-temperature processing (250–380 °C), heterojunction channel engineering, and vertical all-oxide structures, have enabled BEOL compatibility, with system-level demonstrations achieving 6.9–19.2× energy efficiency improvement in CNN benchmarks. However, scaling from laboratory demonstrations to practical implementation faces critical challenges. The primary trade-off in M3D integration involves the number of stacked tiers *versus* cumulative thermal budget, where repeated thermal cycles can degrade bottom layer performance even within nominal BEOL limits. CAM operation in large arrays requires validation of content matching reliability, search power consumption, and false match rates beyond current small-scale demonstrations. Key challenges include balancing search speed *versus* power consumption in CAM operations and achieving device uniformity across multiple functional layers in manufacturable heterogeneous stacking processes. System-level integration of peripheral circuits remains essential for practical implementation.

2.5 Display backplane applications

Display applications uniquely benefit from OS channels being the industry-standard backplane material, with IGZO widely adopted for superior uniformity and low-temperature processing. Display thin film transistors (TFTs) require compensation circuits to address pixel-to-pixel variations and degradation. OS-FeTFTs offer circuit simplification opportunities through ferroelectric non-volatility and programmable threshold voltage control.

A programmable ferroelectric approach to compensate for the positive threshold voltage (V_{TH}) shift in display driver TFTs was developed by integrating ferroelectric films in the gate stack.[121] Display-compatible heat treatment at 350 °C for 1 h simultaneously crystallized the HZO film and annealed IGZO defects and contacts, with intermediate states showing a 20% polarization loss extrapolated for 10 years (Fig. 7a). This approach was advanced to reduce the V_{TH} variation from 0.21 to 0.01 V (Fig. 7b).[122] The programmable compensation enabled the recalibration of degradation-induced V_{TH} shifts during operation, with organic light-emitting diode (OLED) integration demonstrated. Additionally, programmable light intensity control for micro-LEDs has been demonstrated using *a*-ITZO FeTFTs, achieving 3 V MW and multi-level lighting through partial polarization switching.[123] This approach enables Mura-free operation by compensating for light output variations, with the retention exceeding 100 s and an endurance of 10^8 cycles (Fig. 7c). The FeTFT-based active-matrix circuit simplifies conventional designs by removing the need for compensation capacitors while enabling dynamic V_{TH} adjustment. Low-temperature IGZO FeTFT processing on polyimide/polydimethylsiloxane (PI/PDMS) substrates has been demonstrated.[124] The non-volatile characteristics of FeTFTs enabled a 3T0C capacitor-free pixel circuit for pulse-width modulation (PWM) micro-LED operation, which simplified the conventional pixel structures (Fig. 7d). Stable operation was maintained under mechanical stress, including a 1 mm bending radius and 30% biaxial strain for 100 h.

The display industry has already adopted OSs as the mainstream backplane technology due to their superior large-area uniformity and low-temperature processing compatibility. Ferroelectric integration explores additional functionalities through non-volatile operation beyond conventional oxide TFT capabilities. OS-FeTFTs display demonstrated programmable V_{TH} control achieving a 21-fold reduction in V_{TH} variation with degradation compensation. The non-volatile characteristics further enabled capacitor-free three-transistor zero-capacitor (3T0C) pixel architectures for PWM micro-LED applications, with mechanical flexibility at a 1 mm bending radius and 30% strain (Table 5). While ferroelectric layer integration adds process steps, the structural simplification offers potential value. However, OS-FeFET display applications remain exploratory with diverse approaches (V_{TH} compensation, capacitor-free pixels, and flexible implementations) yet to establish dominance. Critical trade-offs include circuit simplification benefits *versus* programming overhead, and refresh/recalibration requirements *versus* long-term V_{TH} stability. Key

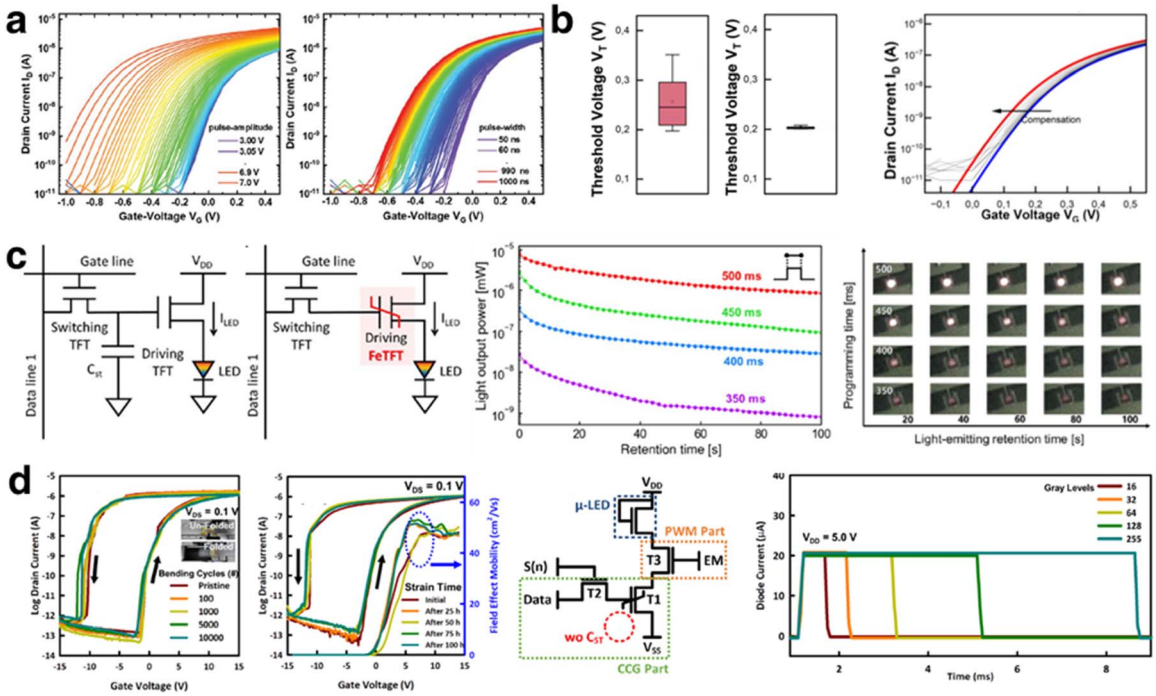

Fig. 7 (a) Transfer characteristics of FeTFTs demonstrating partial switching with voltage pulses of varying amplitude (constant 200 ns width) and varying width (constant 5.5 V amplitude).[121] Reproduced with permission from Lehninger *et al., Adv. Electron. Mater.* **7**, 2100082 (2021). Copyright 2021 Wiley-VCH GmbH. (b) V_{TH} distribution before and after compensation programming for 10 TFTs, and transfer characteristics showing V_{TH} compensation through ferroelectric programming.[122] Reproduced with permission from Joch *et al., SID Symp. Dig. Tech. Pap.* **55**, 100 (2024). Copyright 2024 Wiley. (c) Conventional and FeTFT-based active-matrix circuits for displays. Light output power of an AlGaInP micro-LED with four programmed levels *vs.* retention time, and top-view images during operation.[123] Reproduced with permission from Lee *et al., J. Soc. Inf. Disp.* **33**, 533 (2024). Copyright 2024 Wiley. (d) Hysteresis curves for stretched FeTFT on PDMS under 30% biaxial strain for 100 h. A 3T0C capacitor-free pixel circuit with the FeTFT, PWM timing diagram, and measured current at V_{DS} = 5.0 V.[124] Reproduced with permission from Jin *et al., Nanoscale Adv.* **5**, 1316 (2023). Copyright 2023 Royal Society of Chemistry.

Table 5 Summary of device performance for OS-based FeFETs for display applications reported in the literature

Role	OS (deposition method)	Structure	MW (V)	Endurance	Retention	I_{ON}/I_{OFF}	Ref.
V_{TH} compensation	IGZO (sputter)	MFIS	0.7	N/A	$\sim10^4$ s	$\sim10^6$	121
V_{TH} compensation	IGZO (sputter)	MFIS	0.6	N/A	N/A	$\sim10^6$	122
V_{TH} compensation	ITZO (sputter)	MFIS	3 (V_D = 1 V)	$\sim10^8$ (capacitor)	10^6 s	10^6	123
Constant current generation	IGO (sputter)	MISF	9.1 (V_{DS} = 0.1 V)	$\sim10^4$	2400 s	$\sim10^7$	124

challenges include V_{TH} compensation validation over display lifetimes (>50 000 hours) under continuous operation, array-level uniformity across large panels (>10 inch) beyond current small-scale demonstrations, and flexible display reliability under realistic usage conditions. Commercialization requires demonstrating competitive manufacturing economics and clear advantages over mature LTPS and oxide TFT backplanes that already provide adequate performance for most display applications.

3 Perspectives and future directions

While individual application domains have achieved significant device-level breakthroughs, the maturity levels vary considerably across applications. NAND and neuromorphic systems have progressed to array-level demonstrations, while DRAM and display applications remain at early device-level proof-of-concept stages. Nevertheless, several common challenges have emerged across multiple applications, such as array-level operation, manufacturing integration, and reliability validation. Array implementation requires solutions for device uniformity and array-specific issues, including disturb immunity, interlayer interference, and addressing schemes that would extend beyond individual device optimization. Moreover, manufacturing integration must maintain the advantages of low-temperature processing while meeting commercial fabrication requirements to ensure scalability.

Addressing system-level challenges requires deeper understanding of the OS–ferroelectric interface. Unlike silicon channels that form low-k IL limiting EOT scaling and increasing voltage, OS channels enable direct HfO_2 integration. However, long-term reliability requires systematic investigation. In Si-channel FeFETs, the IL causes wake-up behaviour, limits

endurance to $\sim 10^6$ cycles, and necessitates long read-after-write delays (>10 ms).[125] OS-based FeFETs avoid these IL-related issues, achieving $>10^8$ cycle endurance with immediate readout.[126] However, distinct challenges remain: asymmetric imprint causing read disturb,[127,128] polarization-state-dependent retention,[126,128] longer erase pulses from donor state ionization,[129] and hydrogen-related V_{TH} shifts.[129] Interface engineering, such as oxygen-controlling interlayers, can mitigate these mechanisms.[127] Furthermore, OSs enable low-temperature processing (<400 °C) *versus* poly-Si (>900 °C) critical for multi-tier integration. Deeper understanding of interface dynamics—V_O migration, hydrogen diffusion, and donor state kinetics—remains essential.

Channel engineering represents a relatively recent and limited research area for OS-FeFET development. While structural optimization has been extensively pursued, systematic channel material engineering offers pathways to address application-specific performance requirements. Initial studies explored ITO-IGZO heterojunctions that passivate deep-level defects through self-compensation,[118] and oxygen-deficient intermediate channels providing sufficient depletion charge for full-loop polarization switching.[77] Recent work has expanded these concepts through IGZO composition tuning to balance mobility and bias stress stability,[130] and functional heterostructures (*e.g.*, In_2O_3–ZnO) where oxygen-deficient layers enable efficient switching while high-mobility layers reduce inter-cell resistance.[131] However, these demonstrations remain primarily at the discrete device level. Co-optimization of OS composition with ferroelectric switching dynamics, V_O kinetics, and array-level variability control remains in its early stages,[130,132,133] with validation in 3D architectures such as vertical GAA or multi-tier M3D structures yet to be explored. Further development of channel engineering approaches addressing these aspects holds potential to enhance the MW, cycling endurance, retention stability, and device uniformity in scaled systems.

The diverse requirements across applications highlight the need for systematic material optimization beyond IGZO. NAND and DRAM prioritize cycling endurance and retention stability, logic demands maximum mobility and drive current, neuromorphic systems require precise analog conductance control and displays need low I_{OFF} and a stable threshold voltage. Meeting these varying demands may require exploring binary (IGO, IZO, AZO, and ZTO), ternary (IGZO, IGTO, and IZTO), and quaternary (IGZTO) oxide systems with varying composition ratios, multiple channel stack design, and controlled crystallization. Building on the demonstrated channel engineering approaches, such systematic optimization could enable matching of channel properties to specific applications, advancing OS-FeFET technology through coordinated progress in architecture, interface engineering, and material design.

4 Conclusion

We have discussed the synergistic integration of OSs with HfO_2-based ferroelectrics across five key application domains, revealing how this combination addresses the fundamental limitations of conventional silicon-based technologies. The examination demonstrated that the negligible IL formation and low temperature processability enabled unique advantages across diverse applications. In NAND flash memory, diverse structural approaches and oxygen deficiency control in OS channels achieved substantial MW enhancement in FeNAND. Refresh-free DRAM architectures eliminated standby power through non-volatile 2T0C configurations, while neuromorphic computing demonstrated precise analog weight modulation through the MFMIS structure achieving competitive accuracy on standard benchmarks. Logic applications showcased enhanced functionality in CAM memory and significant energy efficiency improvement in monolithic 3D integration. Display technologies enabled substantial reduction in V_{TH} variation and capacitor-free pixel architectures through non-volatile characteristics.

While each application domain has achieved substantial device-level performance, the transition to practical implementation requires addressing common challenges, including array-level operation, manufacturing integration, and long-term reliability validation. Notably, channel engineering remains less extensively investigated, yet optimization of OS composition, interfacial properties, and heterostructure designs offers promising pathways to address the diverse performance requirements across all applications.

The diverse achievements across memory, computing, and display technologies demonstrate the versatility of OS-FeFET integration and establish a strong foundation for next-generation semiconductor systems. However, realizing commercial potential requires continued research in several critical areas. Fundamental understanding of defect mechanisms-particularly V_O dynamics and their impact on retention, endurance, and reliability phenomena-is essential for predictable operation. Further development in structural optimization, channel engineering through controlled crystallization and V_O control, and interface management represent promising pathways toward enhanced performance and reliability. Additionally, comprehensive array-level validation under realistic operating conditions remains necessary to bridge the gap between discrete device demonstration and practical implementations.

Conflicts of interest

There are no conflicts to declare.

Data availability

No new data were created or analyzed in this study. Data sharing is not applicable to this article.

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