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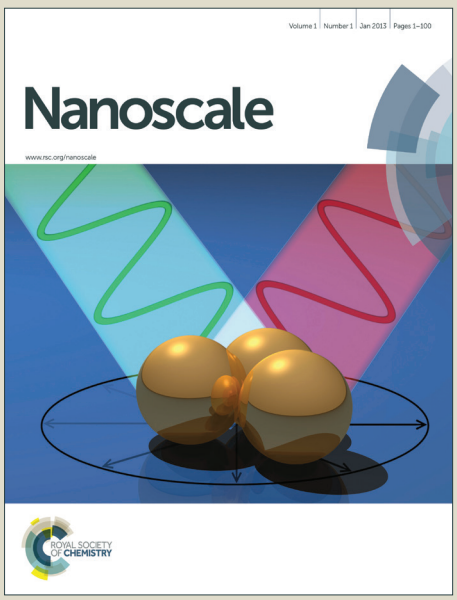

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ARTICLE

Inverted Process for Graphene Integrated Circuits Fabrication

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CMOS compatible 200mm two-layer-routing technology is employed to fabricate graphene field-effect transistors (GFETs) and monolithic graphene ICs. The process is inverse to traditional Si technology. Passive elements are fabricated in the first metal layer and GFETs are formed with buried gate/source/drain in the second metal layer. Gate dielectric of 3.1nm in equivalent oxide thickness (EOT) is employed. 500nm-gate-length GFETs feature a yield of 80% and f_T/f_{max}=17GHz/15.2GHz RF performance. A high-performance monolithic graphene frequency multiplier is demonstrated using the proposed process. Functionality was demonstrated up to 8GHz input and 16GHz output. The frequency multiplier features a 3dB bandwidth of 4GHz and conversion gain of -26dB.

1. Introduction

Graphene is a promising candidate for future high-speed and radio-frequency (RF) electronics, particularly owing to its outstanding carrier mobility and high carrier saturation velocity. Cut-off frequency of graphene field-effect transistors (GFETs) based on CVD grown graphene has reached 427GHz.[1] Researchers have used individual GFETs connected to external passive components to realize graphene circuits.[2-7] However, such circuits inevitably suffer from the degradation induced by external interconnects and parasitic effects. Graphene monolithic integrated circuits, on the other hand, could greatly expand the horizon of graphene technological impacts. Pioneer researchers have made such attempts. Lin et al. has demonstrated graphene circuits integrated on a single SiC wafer which opened up the graphene integration possibility.[8] Han et al. moved forward by utilizing CVD graphene and fabricated GHz-range graphene ICs in IBM 200 mm silicon fab.[9]

Epitaxial graphene on SiC is a candidate for graphene mass production. However, two major drawbacks exist for this method: high cost of the SiC wafers and very high temperature required. On the other hand, CVD graphene shows promise for various applications, especially considering that these films demonstrate transport properties equivalent to exfoliated graphene.[10] Implementing a high-quality gate dielectric on graphene's inert surface remains a challenging issue in GFET fabrication. However, pre-defined buried gates eliminate the need of depositing gate dielectric on graphene. Han et al. fabricated buried gates with 400nm thick W by damascene process and employed 4nm thick HfO_2 as gate dielectric.[9] Double-contact geometry for graphene is recently studied to reduce contact resistance, which consists of metal below and above the graphene sheet in a sandwich-type configuration. Compared with traditional top metal only contacts, it shows at least 40% contact resistance reduction.[11]

Unlike conventional IC process in which field-effect transistors are formed on Si substrates with interconnects on the upper metal layers, this work proposes an inverted graphene integration approach. It shares some similarity with Park et al.'s recent work in which buried bottom gate and source/drain are followed by graphene stacking to form transistors.[12] The starting point is that graphene is a two-dimensional monolayer sheet which offers more flexibility in comparison to bulk materials, such as Si. CMOS compatible two-layer-routing on 8'' wafer is utilized to form pre-patterned IC structures including inductors, interconnects, pads and buried GFET gate/source/drain regions. Next, large-scale monolayer graphene synthesized by CVD method is transferred onto the pre-patterned dies. Buried gates with high-k dielectric layer and source/drain sandwich-type double contacts are employed in this process technology. GFETs with good performance and high yield are demonstrated using the proposed method. In addition, a frequency multiplier based on graphene ambipolar electron-hole symmetry is reported. It features a bandwidth of 4GHz and a conversion gain of -26dB at $f_{IN} = 3GHz$. This

circuit is further operated with input at 8GHz and output at 16GHz.

2. Fabrication Methods

Process flow of the proposed integration approach is shown in Fig. 1(a). A 1μm thick SiO_2 layer was first thermally grown on the 8'' Si substrate. Passive components, four-turn inductors in this case, were formed in the first metal layer (500nm thick Al) with necessary interconnects. After interlayer passivation (1μm SiO_2), the second metal layer (500nm thick Al) was utilized to define GFET gate/source/drain regions, which also enables another layer of interconnects. Each layer of metal is formed by sputtering and etching, followed by chemical-mechanical polishing (CMP) to planarize the surface. The GFET employs a two-finger structure with W/L dimension of 19μm/0.5μm for each finger. 3.8 nm thick HfO_2 (EOT=1nm) was deposited to form the gate dielectric by atomic layer deposition (ALD) method. Then the buried source/drain regions were exposed by photolithography and etching to form graphene sandwich-type contacts in following steps.

Large scale monolayer graphene were grown on polycrystalline Pt substrates by ambient-pressure chemical vapor deposition (APCVD) method.[13] The size of the Pt substrate is 1.5cm × 1.5cm, which determines the dimension of synthesized graphene films. CH_4/H_2 flow rate ratio was set low to guarantee large scale monolayer graphene (see Fig. S1 and S2 in the ESI†). At this stage pre-fabricated wafers were cut into separated dies. Electrochemical delamination method was used to transfer graphene onto pre-patterned dies. Unlike chemical etching transfer method used in Cu and Ni, this method is free of metal residues.[14] Graphene channel was defined by photolithography and 40nm Pt was sputtered as top contacts and patterned by lift-off process to form sandwich-type source/drains. The graphene IC is accomplished on a die by die basis in this work, restricted by the size of available graphene.However, wafer-level fabrication through the whole processes is feasible with wafer-scale graphene films. State-of-art graphene growth technology has increased the size of graphene films up to meter-scale.[15]

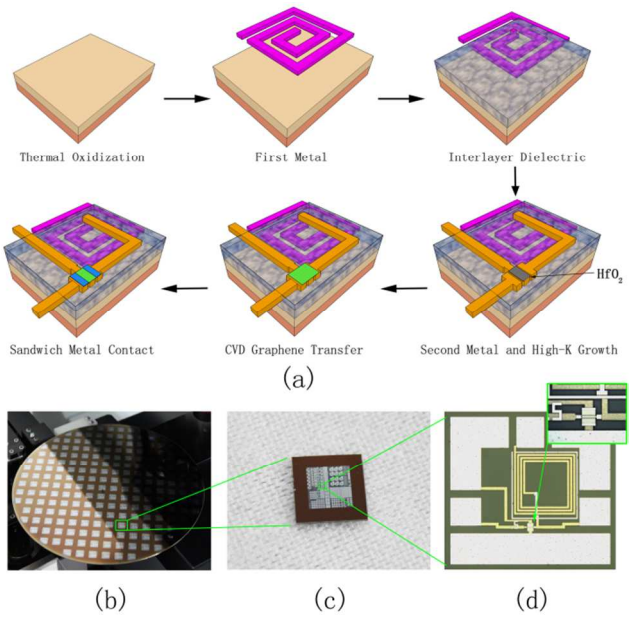

Fig. 1 (a) Process flow of a graphene IC integration with the proposed technology. Photographs of (b) an 8" graphene IC wafer and (c) single pre-patterned die. (d) Optical microscope image of a fully-processed graphene frequency multiplier with inset of the GFET in the IC.

Fig. 1(b) and (c) show photographs of a fully processed wafer and a die, respectively. Fig. 1(d) shows the optical microscopy image of an as-fabricated graphene frequency multiplier circuit, with the inset showing the GFET in the IC. There are a few advantages of this inversed integration process: 1) Easy integration with standard CMOS process. Si transistors, inductors, capacitors, resistors and interconnects, etc. could be first fabricated using standard CMOS process. GFETs are fabricated on the top layer and connected to the rest circuit components by interconnects; 2) Avoiding the challenge of depositing high-k dielectric on graphene. High-k dielectric layer is deposited on metal gates which enables state-of-art CMOS-compatible dielectrics; 3) Sandwich-type contact could lower the source/drain resistance. In this process, Al-graphene-Pt sandwich structure contacts were formed. Lower contact resistance is expected with Pt, considering its relatively large work function.[16] 4) Contaminations from back end of the line (BEOL) processes are eliminated by transferring graphene at the end of the process flow. On the contrary, traditional graphene circuits are fabricated in a "bottom-up" sequence: GFETs are fabricated before interconnects formation.

Based on our experimental results, the proposed method improves the stability and yield of GFETs which is important to achieve graphene ICs. This inverted integration process demonstrates the potential for graphene ICs mass production.

3. GFET Performance

3.1 DC performance

DC characteristics of the fabricated 19μm × 2 wide GFET with gate length of 500nm were characterized using Keithley 4200.

Fig. 2(a) shows the transfer curves measured in vacuum, which demonstrate a four-fold drain current on-off ratio and modest hysteresis. The inset is the scanning electron microscopy (SEM) image of the device. The peak transconductance reaches $21\mu S/\mu m$ with 0.1V V_{ds} bias. Charge transfer induced by Pt contacts extends into the graphene channel, which results in asymmetry of the n and p branches.[17] I_{ds}-V_{ds} curves are shown in Fig. 2(b), with the peak current density of $400\,\mu A/\mu m$. Barreiro et al. experimentally found that drain current in saturation regime ranges from $0.5mA/\mu m$ to $1mA/\mu m$.[18] The measured peak current is close to their observations with the consideration that defects may exist in the graphene channel.

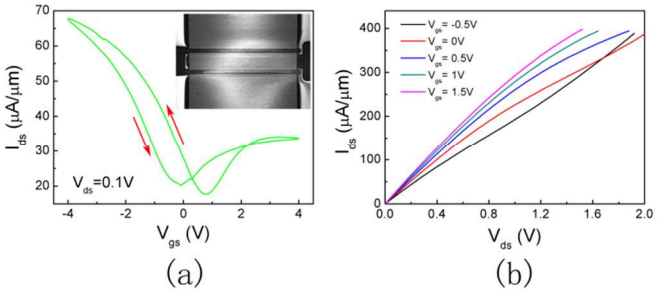

Fig. 2 (a) Transfer curve of a typical 500nm-gate-length GFET at $V_{ds} = 0.1V$. Inset shows SEM image of the device. (b) Output characteristics of the device.

Yield of fabricated 500nm-gate-length GFETs across a die is obtained. GFETs labelled from 1 to 10 cover a range over 3mm, as shown in Fig. 3(a) with the scale bar of 1mm. The corresponding transfer curves with 0.1V V_{ds} bias are plotted in Fig. 3(b). Eight of the ten devices work and five of them feature similar Dirac point positions and comparable drain current. Devices labelled 1#, 9# and 10# have relatively lower current, which is attributed to graphene quality degradation. Failure of the other two GFETs was examined by optical microscope and owed to the final lift-off step. The sources and drains were short-circuited which could be avoided by increasing the thickness of the photoresist. The overall GFETs' high yield proves the feasibility of the proposed graphene technology for potential mass production. Further improvement could be realized by improving the process reliability as well as increasing the size and uniformity of the graphene films.

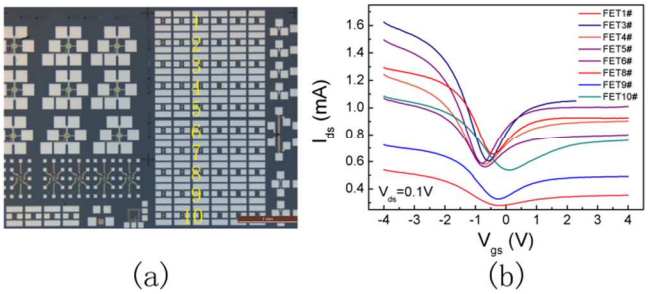

Fig. 3 Yield of the fabricated GFET. (a)Optical image of the 500nm-gate-length GFET array, with the scale bar 1mm. Transfer curves of the corresponding GFETs are shown in (b).

3.2 RF performance

Fig. 4 shows the RF characteristics of the GFET from s-parameter measurements. Careful de-embedding procedures have been performed using "open", "short", and "through" structures, with exact pads layout on the same chip. It can be seen that current gain (h_{21}) and maximum unilateral gain decreases with increasing frequency at a rate close to $-20dB/dec$. The cutoff frequency, f_T equals 17GHz and f_{max}, defined as the frequency where the power gain is unity, reaches 15.2GHz. The f_{max}/f_T ratio is as high as 0.89, as a result of current saturation. Two non-ideal factors limit further improvement of the RF performance in this work at the present stage. The Si substrate has a modest resistivity of $8\sim12\Omega\cdot cm$ and the GFETs are not passivated.

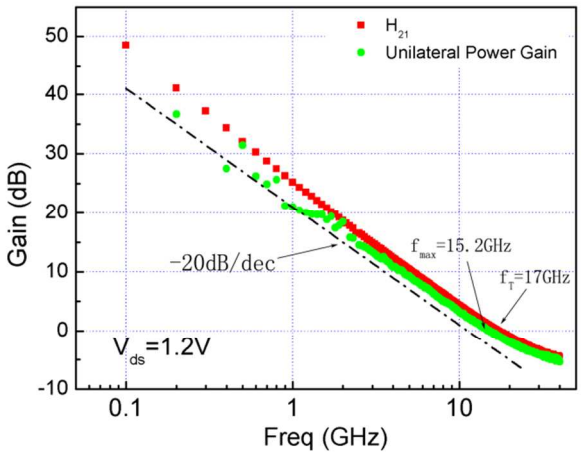

Fig. 4 Measured unilateral power gain and current gain (H_{21}), as a function of frequency for the 500nm-gate-length GFET. The decreasing rate is close to the ideal of $-20dB/dec$. f_{max} and f_T, i.e. frequency at which unilateral power gain and current gain become unity (0dB), result in 15.2GHz and 17GHz, respectively.

3.3 Gate efficiency

Gate capacitance measurement structures were fabricated, which feature gate dimension of 8μm in length and 14.5μm in width. The structures are basically GFETs and the large gate dimension is for measurement accuracy purpose. The V_G dependent gate capacitance C_G of the device was measured by Agilent B1500A, as shown in Fig. 5, with the inset showing the SEM image of a gate capacitance measurement device. AC signal with frequency of 50kHz and amplitude of 50mV was employed to perform the measurement. C_G is viewed as the series of C_q and C_{ox},[19]

$$\frac{1}{C_G} = \frac{1}{C_q} + \frac{1}{C_{ox}} \quad (1)$$

where C_q describes the response of the charge inside the channel to the Fermi level movement and C_{ox} is the bias independent geometrical capacitance of the gate dielectric. The dash line, $C_{ox} = 1.13\mu F/cm^2$ (EOT=3.1nm), in Fig. 5(a) is the

best fit and the retrieved C_q-V_{CH} curve is shown in Fig. 5(b). Capacitance away from the Dirac point increases linearly with V_{CH} with a slope of $\sim 20\mu F cm^{-2}V^{-1}$, corresponding to $v_F \approx 1.1 \times 10^6\, m/s$, in accordance with theoretical values.[19,20] C_q retrieving is very sensitive to C_{ox} in that even C_{ox} variation in a small amount results in C_q deviating from theoretical value significantly. In Ponomarenko et al.'s work, the best fit yields $C_{ox} \approx 0.47\,\mu F/cm^2$ and $v_F \approx (1.15 \pm 0.1) \times 10^6\, m/s$.[19] The C_q-V_{CH} curve in Fig. 5(b) features a C_q minimum at $1.5\mu F/cm^2$, which is determined by residual carrier concentration n*. As n* increases, the minimum capacitance value increases. In this work, C_q minimum translates into $n^* \approx 4 \times 10^{11} cm^{-2}$.[20] The relatively small residual carrier concentration indicates that the graphene is less contaminated as transferred at the end of the process flow.[20]

It is noteworthy that while 3.8 nm thick HfO_2 (EOT=1nm) was deposited to form the gate dielectric, the equivalent gate dielectric, manifested by C_{ox}, is much thicker (EOT=3.1nm). It is attributed to the fact that the buried gate stack is not flat even with CMP treatment. SEM image of the gate stack surface is shown in Fig. 5(c). As a consequence, the graphene film is to some extend suspended rather than absolutely adhere to the underlying gate stack, which is proven by AFM test results (see Fig. S3 in the ESI†). This phenomenon causes an equivalent layer of inserted air between graphene and the underneath gate stack surface. The finding raises a major issue in buried gate graphene technology. Annealing process is proven to help graphene adhere to the buried gate stacks. In addition, more careful planarization is required in further optimization. Still, gate dielectric with thickness of 3.1nm in EOT at the present stage outperforms most top-gate works and has advantages such as eliminating the need of seed layers and being compatible with CMOS technology.[21,22]

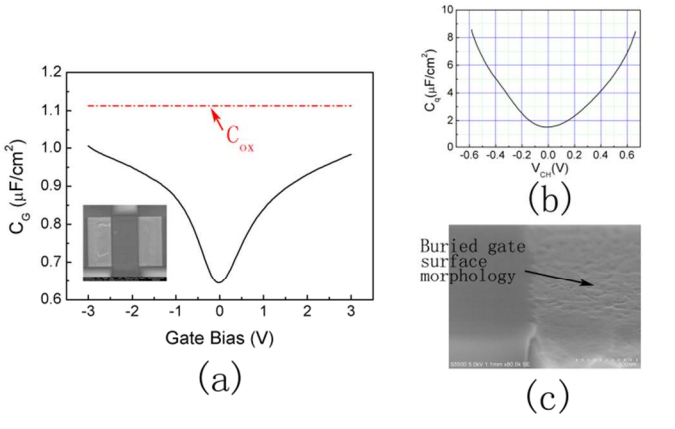

Fig. 5 (a) Gate capacitance as a function of gate bias. The inset shows SEM image of gate capacitance measurement unit. The horizontal dash line is the best fit of C_{ox} which yields quantum capacitance shown in (b). (c) SEM picture of the buried gate surface.

4. Graphene Frequency Multiplier

To demonstrate the capability of integrating circuit components with the proposed process, a frequency multiplier was fabricated. Fig. 6(a) shows the schematic of the frequency multiplier in which 500nm-gate-length GFET is employed, and Fig. 1(d) is the circuit optical microscope image. As the GFET features V-shape transfer characteristics, the sinusoidal input biased at the Dirac point produces an output signal with the fundamental frequency twice of the input frequency.[4-7] The inductor is used to decouple RF signals and drain bias. The input of the graphene frequency multiplier covers a range from 1GHz to 8GHz. For 1GHz and 8GHz input cases, the output spectra are shown in Fig. 6(b) and (c). With input power of 0dBm, this frequency multiplier features output power of -26dBm and -39dBm for 1GHz and 8GHz inputs, respectively. Fig. 6(d) shows the cable loss over frequency in the measurement setup. These values are added back to the measured data.

This frequency multiplier features largely improved performance due to the suppression of parasitic effect induced by external interconnects and the GFET exceeding previous works.[4-7] The frequency response of the multiplier is shown in Fig. 7(a), with V_{ds} biased at 0.5V and V_{gs} at the Dirac point. The 3dB bandwidth of the conversion gain is observed to be around 4GHz, which outperforms previous reports.[6,7] Further improvement of the bandwidth can be achieved with higher V_{ds}, as f_T of a GFET is proportional to the drain bias.[1]

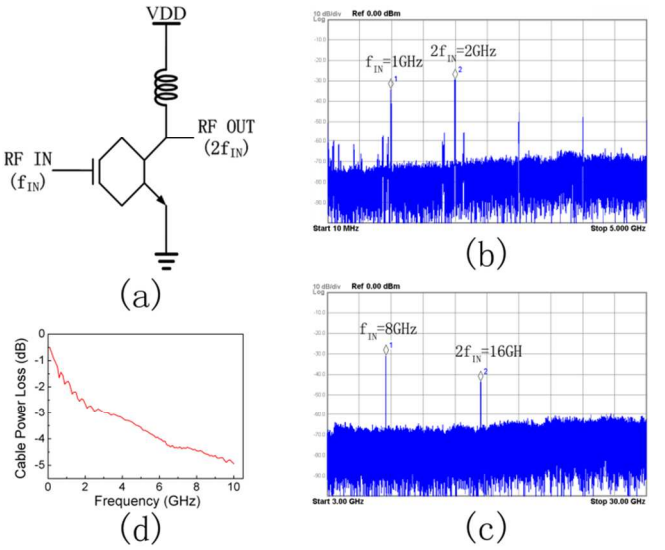

Fig. 6 (a) Schematic of the graphene frequency multiplier. Captured images from the spectrum analyzer during the multiplier operation for 1GHz (a) and 8GHz (b) inputs. The cable loss of the measurement setup was measured independently, as shown in (d).

Conversion gain at $f_{IN} = 1\sim3$GHz is about -28dB with little variation. When the drain bias is increased to 0.8V, the conversion gain at $f_{IN} = 3$GHz increased by 2dB reaching -26dB, which outperforms previously reported discrete circuit results.[6,7] In Wang et al.'s work, conversion gain reached -30dB with the input frequency at 700MHz, and Ramon et al. achieved peak conversion gain of -35dB. Aggressive gate oxide scaling is required to enhance the conversion efficiency, together with the suppression of non-ideal factors, such as high contact

resistance and impurity concentration.[23] The high conversion gain in this work supports that the proposed inverted integration process is suitable for GFETs fabrication. Fig. 7(b) shows output power and conversion gain dependence on input power at 3GHz. Saturation of the output power occurs when input power exceeds 0dBm. Conversion gain peaks at 0dBm input.

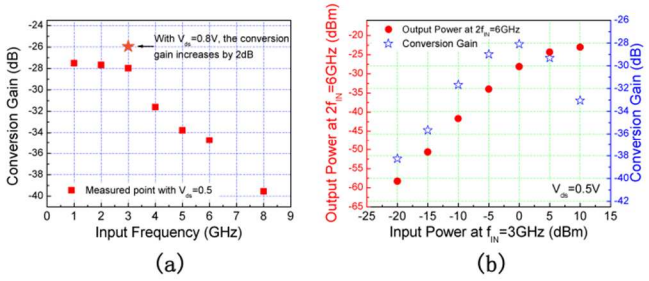

Fig. 7 (a) Frequency response of the graphene frequency multiplier. The 3dB bandwidth of the conversion gain is around 4GHz at V_{ds}=0.5V. (b) Output power and conversion gain at $2f_{IN} = 6GHz$ are plotted against the input power at $f_{IN} = 3GHz$.

5. Conclusion and Outlooks

In summary, we have proposed a novel inverted graphene integration approach. Buried gate/source/drain regions are employed to implement state-of-art CMOS-compatible gate dielectric and sandwich-type source/drain contacts. Graphene being transferred at the end of the process flow, contaminations from BEOL processes are eliminated. Fabricated 500nm-gate-length GFETs feature f_T/f_{max} =17GHz/15.2GHz RF performance and yield of 80%. Two-layer-routing technology enables passive components and interconnects integrated with GFETs easily. With parasitic effects largely reduced, a proposed monolithic frequency multiplier achieves 4GHz 3dB bandwidth, and conversion gain reaches -26dB at f_{IN} = 3GHz. The proposed graphene integration technology is a promising process approach in mass production of graphene based devices and circuits with the possibility to be integrated with Si electronics.

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† Electronic Supplementary Information (ESI) available: Optical images and Raman spectrum of graphene, AFM image of the buried gate stack. See DOI: 10.1039/b000000x/

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