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## A review on single crystal and thin film Si–Ge alloy: growth and applications

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The IV–IV binary alloy, Si–Ge, has attracted incredible attention for its superior performances in multiple disciplines, especially in high temperature thermoelectric and BiCMOS applications in the semiconductor industry. Although the alloy perceptibly exhibits a complete miscible system that can realize Si–Ge crystals with any Ge contents, the wide gap between the solidus and liquidus line inhibits the formation of Si–Ge bulk crystal with uniform Ge content. Several synthesis procedures were adapted to counteract the single crystal Si–Ge with a homogeneous composition. Although polycrystalline Si–Ge finds wide application in thermoelectric applications, single crystal silicon–germanium has proved to be the most economic, unconditional transceiver chipset resolution to uplift the future soaring bandwidth requisite for wireless backhaul information transmission. In addition, the superior electronic mobility in Si–Ge in contrast to Si has established its place in telecommunication, computer technologies, consumer electronics, space, and aerospace applications. Herein, we comprehensively summarize the development in the synthesis of bulk and thin film single crystal Si–Ge with uniform composition to be used in thermoelectric applications, especially in space applications and as heterojunction bipolar transistors to form a Si–Ge heterojunction bipolar transistor (HBT) BiCMOS technology. Thus, this expertise is expanding into diverse end-markets owing to telecom, automobile, solar, and thermoelectric capabilities. The perspective for improving the performance of the binary IV–IV alloy is also provided as a model for future development and applications in the thermoelectric and semiconductor industry.

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### 1. Introduction

Silicon and germanium have been a perpetual source of attraction for researchers for their potential applications in several technological areas. However, significant synthetic impediments such as moisture and oxygen sensitivity, high crystallization temperatures, and restricted surface functionalization choices make the development of these materials an open-ended challenge.<sup>1–12</sup>

#### 1.1. Locus of silicon–germanium in the semiconductor table

Silicon–germanium (Si–Ge) is now a well-accepted semiconductor, which hit a peak in its production in the 1990s. However, this semiconductor did not become a success overnight. The discovery of the combination of silicon and germanium was coincidental.<sup>13</sup>

#### 1.2. Historical sketch

In the 1970s and 1980s, Dr Bernard Meyerson, an IBM researcher, inadvertently dropped a piece of silicon that was just cleaned in HF on the ground. Thereafter, rinsing the silicon wafer under

water to clean revealed that it was water-repellent. Later, Meyerson discovered that cleaning silicon in hydrofluoric acid forms a protective hydrogen layer, which negates the requirement of heating silicon to 1000 °C to eliminate the contaminating oxide on silicon. At 600 °C, the H<sub>2</sub> layer blows off and forms the oxide. This discovery permitted scientists at IBM to grow Si–Ge at 550 °C. Thus, Dr Bernard Meyerson from IBM laid the foundation for an explosive improvement in wireless products, such as global positioning system (GPS) devices, mobile TV, wireless broadband Internet (WiFi), and cell phones. The magnificent Si–Ge was far more competent than silicon alone. Equally important, it was less expensive than GaAs, the foremost alloy of the day employed in communication chips. With Si–Ge, IBM single-handedly attained great production proficiency along with a patent safeguard.<sup>14</sup>

#### 1.3. Silicon–germanium in thermoelectric (TE) applications

A significant matter in TE investigation is to discover a TE material having high-performance, *i.e.*, high electric conductivity and low thermal conductivity. More conceivable solutions were put forward and proved; one of the potential resources was silicon. Silicon and new Group IV binary or ternary alloys possess the capability to be utilized in the development of a thermoelectric generator (TEG) in the commercial industry for

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several reasons. The source of Group IV elements is more inexpensive than the conventional TE materials, and is preferred over toxic materials such as  $\text{Bi}_2\text{Te}_3$ . Group IV elements are also ecofriendly and harmless for civic use.<sup>15,16</sup>

#### 1.4. Silicon–germanium in the electronic industry

In accordance with the Cisco Annual Internet Report, which is a global forecast/analysis, almost 2/3rd of the population worldwide will enjoy Internet access by 2023. The overall Internet consumers will be 5.3 billion (66% of global inhabitants) by 2023, ahead by 3.9 billion, *i.e.*, 51% of the global population in 2018. This could lead to worldwide Internet traffic that evaluates digital transformation across various business segments.<sup>17,18</sup> These colossal figures, in addition to their exponential enhancement, remarkably elucidate how computing systems, and hence, integrated circuits (ICs) fix the velocity for both complementary metal oxide semiconductor (CMOS) commerce and a completely progressive civilization. The eternal swelling requirement meant for mobile devices is regarded as the main driver. Nevertheless, the negative side of this progress, *i.e.*, the radically enhanced power consumption ensuing in the alleged power consumption crisis, demands novel, enhanced mobility channel materials and innovative device hypotheses for low power transistors.<sup>19</sup>

Silicon–germanium (Si–Ge) has proved to be the first low-cost, absolute transceiver chipset resolution to boost the forthcoming high bandwidth prerequisites for wireless backhaul information transmission. Specifically, these chips are capable of transferring information over the network quicker than the present arrangement, and can maintain mobile device expansion for years to come. Si–Ge poses a solitary chip platform with the functionality usually bestowed by several chips, comprising digital, mixed-signal, and analog circuits, and is thus an

extremely modest solution for mobile service contributors to empower ultrahigh-speed data streaming.<sup>20</sup>

Thus, the alluring characteristics of the Si–Ge alloy can be utilized for various applications including (i) solar cells, (ii) high mobility CMOS gadgets, (iii) wavelength sensitive photonic devices, (iv) light-emitting diodes (LED), (v) micro-electronics, (vi) thermoelectric generators, (vii) next-generation semiconductor devices, (viii) gamma detectors, (ix) X-ray focusing systems, and (x) high-performance discrete devices.<sup>21</sup> It exhibits complete miscibility across its whole composition range, which permits the modification of its properties, *viz.*, lattice constant and bandgap amongst those of bulk Si as well as Ge. This implies that based on the composition, Si–Ge alloys are can tune the thermoelectric and optoelectronic properties rather than depending on size alone, making these a potentially valuable class of materials for diverse applications. In solar cell applications, Si–Ge proposes new design features that expand its operational life to  $\sim 80$  years and efficiency to 30–40%. The asset of the constituents of the Si–Ge alloy is that both Si and Ge have resources that are comparatively more abundant, low-cost, and non-toxic, unlike standard solar materials.<sup>22–24</sup>

As stated, the wide application of Si–Ge alloy is attributed to (i) dense, smooth and, crack-free single crystal semiconductor growth, (ii) epitaxial layer having high carrier mobility, (iii) the rate of yield is high, and (iv) high speed and moderate cost.<sup>25</sup>

Initially, in the 1970s when Si–Ge was considered the only high temperature thermoelectric alloy for space missions, the evaluation of its thermoelectric properties was promising, and thus, the preparation of good quality samples was critical. At the first stage of investigating the material, a single crystal or large grain polycrystalline ingot was synthesized.<sup>26</sup> Since Si–Ge is a completely miscible system, therefore, in principle, Si–Ge crystals with desired Ge contents can be realized. The phase diagram presents opportunities to engineers and scientists worldwide to manipulate the material properties and increase the device efficiency by including Si–Ge in Si.<sup>27,28</sup> However, crystal growth expertise has not yet been established for single crystalline Si–Ge bulk crystal having homogeneous Ge content from liquefied Si–Ge. This can be attributed to the inherent complications of controlling the Ge content and circumventing polycrystallization from molten Si–Ge during bulk crystal growth. The phase diagram of Si–Ge, as indicated in Fig. 1, is very straightforward with one solidus and liquidus line. These two lines intersect at the freezing points of Ge (938 °C) and Si (1414 °C). Usually, the outgrowth from the melt progresses under near-equilibrium conditions, and the solidus line determines the content of Ge in the  $\text{Si}_{1-x}\text{Ge}_x$  crystal,  $X_s$ , which originate from molten Si–Ge at a given temperature,  $T$ .<sup>29</sup> Therefore, the manipulation of the growth parameters is very crucial, especially  $T$  with a steady value to attain consistent Ge content. Moreover, the high distribution coefficient of Si in Ge ( $\kappa_{\text{Si}}^{\text{Ge}} \approx 5$ ) creates problems in developing SiGe single crystals from the melt and the considerable difference among the melting points of Ge ( $\sim 938$  °C) and Si ( $\sim 1414$  °C) tends toward constitutional supercooling.<sup>30</sup> Supercooling can be avoided by high temperature gradients at the phase periphery in agreement



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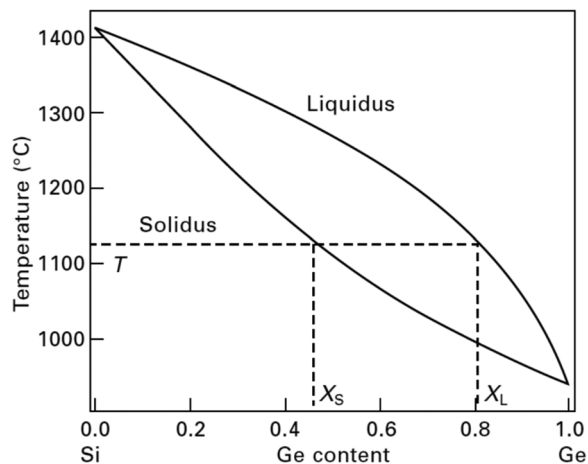


Fig. 1 Phase diagram of Si–Ge: at a given temperature  $T$ , the presence of Ge in the Si–Ge bulk crystal can be established based on the solidus line.

with the Tiller criterion. Thus, a minor variation in the temperature,  $\Delta T$ , might cause a considerable disparity in the Ge content,  $\Delta x_s$ . Besides, the phase diagram of the binary alloy system Si–Ge illustrates that there is a wide separation between the solidus and liquidus lines at a particular temperature. This implies that the segregation coefficient,  $k = X_s/X_L$ , deviates from unity, and the liquidus Ge content,  $X_L$ , is greater than the solidus Ge content,  $X_s$ . Hence, it is obvious that crystal growth will result in the depletion of SiGe; thus, we begin with a predetermined amount of liquefied Si–Ge. Thus, the leading force of the crystal growth vanishes. Hence, there exist two major prerequisites for crystal growth to obtain an Si–Ge bulk crystal with consistent Ge content: (i) to maintain a constant temperature for growth, and (ii) to supply Si in the SiGe melt.<sup>29</sup>

## 2. Synthesis methods for Si–Ge alloy using bulk crystal growth

Increasing demand for crystals used in semiconductor physics, engineering, electro-optic devices, *etc.*, has led to the growth of crystals otherwise. In earlier days, natural specimens were the lone source of large, well-formed crystals.<sup>31</sup> Crystal growth generally occurs utilizing the following series of processes.

- Diffusion of the molecules of the substances to be crystallized through the surrounding atmosphere.
- Molecules diffuse over the surface of the crystal to distinct sites on the surface.

By crystal growth techniques, nowadays, nearly all naturally occurring crystals of interest can be synthesized successfully in the laboratory.<sup>32</sup> The growth aspect varies with the crystal depending on their chemical and physical properties such as decomposition, solubility, phase change, and melting point.

### 2.1. Basics of crystal growth

To grow a crystal, the state of supersaturation, followed by the process of nucleation, is the fundamental condition that needs to be attained.<sup>33,34</sup>

### 2.2. Conditions for growing a crystal

Crystal growth can only occur from pure gases and pure liquids or liquid and gaseous solutions, if a certain degree of supersaturation or supercooling has been initially achieved in the system. The realization of the supersaturated state is vital for any crystallization operation and the extent of super saturation or divergence from the equilibrium saturated condition is the key factor controlling the deposition process.<sup>35</sup> The growth of crystals can be considered to take place in the following steps.

- (1) Attainment of supersaturation or supercooling.
- (2) Development of crystal nucleus of microscopic size.
- (3) Consecutive growth of crystals to produce distinct faces.

### 2.3. Crystal growth techniques

Crystal growth is a demanding task and the procedure followed for the growth of the crystal depends on the features of the material under investigation, such as its volatile nature, melting point, and solubility in solvents.<sup>36–44</sup> The fundamental growth methods available for crystal growth are broadly classified in accordance with the flow chart,<sup>45</sup> as shown in Fig. 2.

**2.3.a. Melt Growth method.** Melt growth is the method of solidification of a pure material after crystallization of fusion and crystallization from the melt upon cooling the liquid below its freezing point. The speed of growth is relatively better than that of other possible techniques; therefore, the probable contamination is low, *i.e.*, either from the crucible materials or from the encompassing environment. Moreover, the principle of the technique is that melt growth is the most commercially viable technique of crystal growth.<sup>46</sup>

The most common techniques that have been adapted are as follows.

(i) *Bridgman method.* In essence, the Bridgman Method, as shown in Fig. 3, produces crystals from flux by gradually freezing it from one end to the other. The technique yields crystals with suitable dimensional control and involves little or no supervision due to its simplicity.<sup>47,48</sup> However, controlling the heat flow becomes progressively difficult; for instance, the diameter of the crystal enlarges. A broad variety of materials are formed using this method. One major requirement is that the crucible material should remain intact either from the melt or its vapor. Dislocation densities can also be restricted to  $>10^4 \text{ cm}^{-2}$ , and many materials comprise grain boundaries with a low angle. Because the Si–Ge phase diagram depicts that it undergoes strong segregation in the course of growth, the synthesis of the alloy is not straightforward. The convection current occurring within the molten  $\text{Si}_{1-x}\text{Ge}_x$  causes fluctuations within the growth parameters.<sup>49</sup> Moreover, due to the massive density difference of molten Si and Ge, gravity plays a key role in the stimulation of convection movements in the liquefied alloy. This indicates the significance of Si–Ge crystal growth on an extended interval microgravity stage to unearth its basic properties. Concerning the planning of likewise experiments, the growth of  $\text{Si}_x\text{Ge}_{1-x}$  crystal with  $x = 0.25$  and  $0.15$  was performed by means of the vertical Bridgman technique within the test site. The expansion was carried out in a 3-zone





Fig. 2 Categorization of crystal growth techniques.



Fig. 3 Schematic of the Bridgman method.

resistive furnace comprising of Pt–Rh heating wire. The expansion ampoules were moved at a pace of  $0.3 \text{ mm h}^{-1}$  and  $0.4 \text{ mm h}^{-1}$ , where the slope was alongside the  $g$  vector. The developed Si–Ge samples were measured to be 9 cm long and 2.5 cm in diameter. The samples were carved axially, polished, and etched to review the growth of the expansion patterns along the axis of expansion. The interface profile transformed from concave to planar or convex as the growth progressed. Microprobe analysis using electron microscopy was dispensed to live the Si content beside and transverse to the axis of expansion. The axial Si content was analyzed employing a simple 1-D model, considering full amalgamation of the melt in the course of growth and a segregation coefficient that differs in the Si content within the flux, as given by the phase diagram of the Si–Ge alloy.<sup>50,51</sup>

(ii) *Czochralski method*. This technique may be a workhorse for the synthesis of an overwhelming majority of Si single crystals to date. Thus, several researchers have applied the CZ method, as shown in Fig. 4(a), to get single crystal Si–Ge. The technique is known after the renowned scientist Jan Czochralski from Poland, who developed it in 1916.<sup>52</sup> However, numerous intrinsic difficulties are related to the growth of the single crystal from the melt having multi-elements such as Si–Ge in divergence to the growth of a crystal of a single element.<sup>53</sup> Freidrich *et al.* illustrated that probability of existence of “structure loss”, *i.e.*, presence of dislocations and grain boundaries increases the manifold by CZ growers thanks to the high concentration of doping; therefore, the phenomenon is often termed as “constitutional supercooling”.<sup>54</sup> The phenomenological description of constitutional supercooling can be described by Fig. 4(b). However, it is applicable to materials that melt congruently or nearly congruently. To realize a stable liquid–solid interface, Kürten *et al.* reported the CZ growth of Si-enriched Si–Ge by means of a very sluggish pulling rate.<sup>55</sup> Deitch *et al.* explained that the phase diagram of Si–Ge dictates that to avoid the onset of dendritic growth, an extremely low pulling rate is required.<sup>56</sup> Thus, the synthesis of the Si–Ge bulk crystal by the CZ method is 40 times slower than the traditional CZ method of the synthesis of the Si bulk crystal. Abrosimov *et al.* used Si rods for the continuous feeding of Si to the melt so as to avoid the depletion of Si during CZ growth.<sup>57</sup> As a result, single crystalline Si–Ge having  $\text{Ge} \leq 0.2$  was attained. Kurten and Schilz produced Si–Ge alloys having  $0.62 < x < 0.98$ <sup>55</sup> using the heteroseeding process, where the seeding material is either Si or Ge crystals. Usually, the Si seed is employed aiming at the production of Si–Ge single crystal even from the original melt of pure Ge. The heterocrystal is created by considering Si element in the molten seed of Si. Hence, for the entire composition range of  $x = 0-1$ , Si seed is





Fig. 4 (a) Representation of the Czochralski method and (b) distribution of the concentration  $C_L(x)$  of a dopant within the melt versus distance  $x$  from the expansion interface, where  $C_L(0)$  denotes the concentration within the melt when no distance is traversed from the interface.  $\delta$  signifies the width of the physical phenomenon. Liquidus temperature  $T_L(x)$  resembling the concentration profile  $C_L(x)$  plotted in (a) versus distance  $x$  from the expansion interface, plotted within the same scaling as in (a). The temperature profiles  $T'(x)$  and  $T''(x)$  are two cases that show two different designs of the new zone or the heating conditions in an exceedingly certain CZ growth setup. The shaded area indicates the zone where the melt is "constitutionally supercooled" before the expansion interface, reaching up to position  $x^*$  within the case of temperature profile  $T''(x)$ . Reproduced with permission from ref. 54.

understood to be available for the growth of Si-Ge crystals.<sup>58</sup> Based on Tiller's criterion,<sup>59</sup> Yonenaga *et al.* estimated the critical growth velocity of the occurrence of constitutional supercooling as a function of Ge content at a given  $\Delta T$ .<sup>53</sup> However, polycrystallization was observed for the intermediate Ge content, even when the expansion velocity is slower than the critical value. Fig. 5(a-c) demonstrates the Si and Si-Ge crystals grown by the CZ method.

(iii) *Zone melting.* The word 'zone melting' symbolizes a genus of techniques for regulating the impurities or solute concentrations in crystalline materials, which was first pioneered by Pfann<sup>60</sup> to purify Ge for its use in transistors.<sup>61</sup> It will be employed to enhance the impurity segregation by offering a high degree of separation of the solvent and solute, which is

termed as zone refining, or to get rid of segregation by offering a standardized distribution of impurity within the material, which is known as zone levelling. Zone refining is an exceptionally efficient purification method that utilizes combined melting and freezing practices for refining semiconductors, metals, and inorganic and organic chemicals.<sup>60,62,63</sup> Here, a narrow molten zone is allowed to navigate across a solid bar by concentrating and progressing a source of warmth at a specified rate along the matter having both melting and solidifying liquid interfaces, as shown in Fig. 6(a and b). At the edge of melting, solid matters are liquefied and blended including the contents of the molten region. However, at the interface of freezing, the impurities within the recent frozen solid varies as of that within the liquid. However, if the impurity reduces the freezing temperature of the solvent, the freezing interface



Fig. 5 (a) Silicon crystal having a radius of 150 mm and a weight above 250 kg, grown by the CZ technique (Image courtesy of Siltronic AG4), (b)  $\text{Si}_x\text{Ge}_{1-x}$  alloys developed by the CZ method having [001] oriented Si seed crystal. (c) GeSi boules developed with Dash necking (left) and developed with a Si-Ge seed with identical constituents (right). Reproduced with permission from ref. 53.



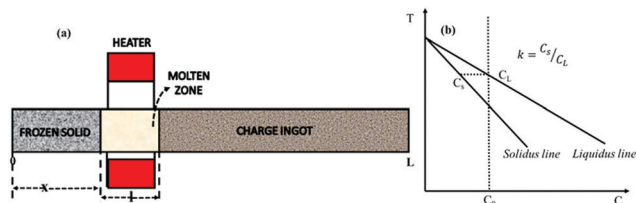


Fig. 6 Schematic of (a) the zone melting method; (b) a part of binary phase diagram.

continuously discharge the solute atoms into the molten zone where they bring together and are propelled toward the intense end of the bar, *i.e.*, within the similar direction of the zone movement. Nevertheless, if the solute increases the temperature of the solvent, the build-up of the solute within the solidifying interface is going to be preferred, thus offering a progressive purification within the reverse direction of that of the zone movement. Thus, the interface of freezing can attract or reject selected kinds of solutes, leading to better-purified materials. Zone refining seeks suitable application in synthesizing silicon-on-insulator (SOI) films<sup>64–67</sup> and ultra-pure materials<sup>68–74</sup> as super-conducting and semi-conducting<sup>75–78</sup> substances.

Based on the above principle, different zone refining technologies exist and, counting on the strategy of charging and

also the geometry, the categorization will be of four types (Fig. 7), *viz.*, (a) horizontal, (b) vertical, (c) floating, and (d) continuous zone refining. Table 1 summarizes the different ways of zone melting, which comprises detailed characteristics, pros and cons, and operations for each variant.

*a. Zone Levelling.* As mentioned earlier, zone levelling is unique among several zone melting methodology and is used for high  $T$  thermoelectric alloy, *viz.*,  $\text{Si}_{80}\text{Ge}_{20}$  solid solution, which causes homogeneous distribution of impurities.

The molten zone navigating a block has two solid-liquid interfaces: (i) a melting edge and (ii) a freezing edge. At the melting edge, the melting of the solid ingot initiates and fuses with the matters of the zone and thus separates out, whereas at the freezing edge, the concentration of the solute in the region that is getting solidified differs from that in the liquid.

The two possible conditions that prevail are (i) if the soluble impurities (solute) lower the melting point of the solid charge (solvent), then the concentration of the impurities will be lower in the freezing solid as compared to that in the liquid. Hence, the impurities will be discarded by the freezing solid and expelled with the molten part; (ii) if the contaminant elevates the melting point of the charge solid, then the strength of the impurities in the freezing solid will be high as compared to that in the liquid and thus the liquid will be depleted of impurities.



Fig. 7 Arrangement of technologies involved in variable zone refining: (a) horizontal zone refining set up;<sup>79</sup> (b) vertical zone refining set up;<sup>80</sup> (c) floating zone refining set up;<sup>81</sup> (d) continuous zone refining set up,<sup>82</sup> adapted pictures.



Table 1 Comparison of various alternatives of zone refining technologies

Forms of zone refining	Features	Pros	Cons	Purposes
Horizontal zone refining	Crucible is placed horizontally whereas heating elements are moved horizontally	Simple to load and unload the materials, and the interfaces can be distinguished easily	Engage more space	Used for most metals except for some materials that are reactive.
Vertical zone refining	Crucible is placed vertically whereas heating elements are moved vertically	Engages small space	It is difficult to load and unload materials and crucibles are at a higher risk of cracking	Used for most metals except for some materials that are reactive
Floating zone refining	Deprived of crucible, the stuffs are positioned vertically and the molten zone is retained at the solid-liquid interface	Low contamination, low space occupation, and good transfer of heat	Restricted charging material of high surface tension and low yield due to small size of the material	Used for reactive metals such as silicon, zirconium, tungsten, and iron
Continuous zone refining	Inlets and outlets are there for feeding materials and continuous collection of waste and product, respectively	High yield and high refining efficiency	Intricate design, high cost, and inconvenient operation	Hypothetically, most metals but the experimental stage is under development and hence is of no commercial usage

Thus, the freezing interface can expel out certain amounts of impurities.<sup>83</sup>

Here, the charge consists of two components that constitute a binary solid solution. The composition varies with along the length of the ingot ( $x$ ). The ingot might contain two rods of pure components whose relative cross-section is decided by the mean composition  $C_0$ . The length  $l$  of the molten zone traverses the charge gradually. When the heater (zone) passes through the ingot, the profile of the distribution of the impurities (solute) is shown in Fig. 8.

The curve has been divided into three discrete regions: (i) initial region, (ii) level region, and (iii) final region. At the beginning, the concentration of the melted material is  $C_0$ . Assuming the efficient distribution coefficient ( $k$ ) to be less than unity, whilst the zone proceeds a brief distance, it solidifies, at  $x = 0$ , a sheet of solid of strength  $kC_0$  of the solute, and so persists, at  $x = l$ , by liquefying a layer of strength  $C_0$ . Consequently, the region is enriched and solidifies at a higher concentration. The critical important parameter in this process

is the equilibrium diffusion coefficient,  $k$ , along with  $k_{\text{eff}}$ .  $k_{\text{eff}}$  is demonstrated to be the ratio of experimental  $C_s$  and  $C_L$ , *i.e.*,  $C_s/C_L$ . Nevertheless, the difficulty in determining  $C_L$  experimentally, the Bruton-Prim-Slichter (BPS) equation,<sup>84,85</sup> and the model is used to determine  $k_{\text{eff}}$  and is given by  $k_{\text{eff}} = \frac{k}{k + (1 - k) \exp(-V\delta/D)}$ , where  $V$  is the velocity of movement of the molten zone,  $D$  is the diffusion coefficient of the impurity in the flux, and  $\delta$  is the width of the boundary of the diffusion layer at the interface of solid/liquid.

In the case of refining of the  $\text{Si}_{80}\text{Ge}_{20}$  alloy, two precursors of Si-Ge were chosen:  $a(\text{Si}_{52.5}\text{Ge}_{47.5})$  for zone melting and  $x(\text{Si}_{80}\text{Ge}_{20})$  for homogeneity, *i.e.*, composition levelling.<sup>86</sup> They are preloaded into either the processing boat, which can be made of glassy carbon, carbon-coated quartz, or graphite, which is scaled inside a quartz tube maintained at vacuum, and the zone is melted at a steady temperature. During the passing of zone on both liquid-solid interfaces, two processes take place simultaneously: melting of the pre-synthesized (non-uniform) precursor  $x$ , on the interface at the right, and the crystallization of uniform composition  $x$ , at the left interface. However, at each fixed time, the amount of the crystallized material and the amount of the molten precursor remains the same. Thus, a fixed composition of the melt is retained, and so a uniform  $\text{Si}_{80}\text{Ge}_{20}$  solid-solution bar is yielded. In order to evade the relapse of the quartz ampoule, the zone heater made of RF coil is used as an alternative of the typical resistance furnace. Here, the graphite crucible performed the function of an RF susceptor, the complete heating assembly was fixed, and the ampoule was slid. The rate of movement was kept sufficiently low to deliver uniform recrystallization of the charge. Hence, inter-crystalline liquation was averted. It needs to be noted that the overall procedure was accomplished at a temperature much lower than  $T_{\text{liq}}$  of  $\text{Si}_{80}\text{Ge}_{20}$ .



Fig. 8 Estimated solute concentration following the movement of the molten zone across the charge of homogeneous mean concentration  $C_0$ . Adapted from ref. 60.



*b. Floating zone method.* The float zone (FZ) method is a crystal growth technique where a zone of melt is created between the upper feed material and lower seed material by employing restricted heating (Fig. 9).<sup>58,87</sup> The starting material of the process consists of a seed crystal and a polycrystalline rod. Using the comparative motion of the heating device, the zone of floating is translated along the length of the rod in such a manner that the growth of the crystal occurs on the seed (which is underneath the melt) and concurrently melts the feed material over the floating zone. Here, unlike the CZ method, the crystal is allowed to grow without any interaction with the wall of the crucible. Thus, the concentration of impurities reduces drastically and high purity crystals are obtained, although the diameter of the crystal is less than 150 mm and the diameter of the ingot is restrained by the surface tension of the molten zone. The technique leads to next-generation saleable crystal products (such as a majority of extremely pure silicon yielded today is administered by the FZ technique).

The benefits of the FZ method for the growth of Si-Ge crystal lies in the fact that there is a sharp temperature gradient to circumvent constitutional supercooling<sup>59,88</sup> and the lack of wall contact. Both are beneficial for overcoming polycrystallization. However, it is difficult to feed the base elements in the molten zone because the feed rods are chemically deposited for

Si technology and are not accessible for silicon-germanium crystal growth. Thus, a method was adapted for the alloying of Si with Ge, which allocates the enduring feeding of Ge granules ( $\sim 3.5 \text{ mm}^3$ ) throughout the process of growth precisely into the melt.<sup>89</sup> Saidov *et al.* explained that to avoid constitutional supercooling, electron beam heating can be used as it creates a temperature profile where the centre of the liquid zone attains the maximum temperature and thus a characteristic temperature gradient is established.<sup>87</sup> The obtained single crystal can have Ge up to 50% with an ingot (pre-synthesized polycrystalline Si-Ge) of diameter  $< 3 \text{ mm}$  with narrow melting zone. Wollweber *et al.* worked with the RF-heated FZ equipment for the synthesis of  $\text{Si}_{1-x}\text{Ge}_x$  single crystal,<sup>90</sup> whereas Campbell *et al.* used the mono-ellipsoid mirror furnace in the FZ method to grow Ge-rich Si-Ge crystal.<sup>91</sup> The significance of the technique, for the perfection of the  $\text{Si}_{1-x}\text{Ge}_x$  single crystal, has to be credited to the optimized progression parameters, *viz.*, the rate of rotation, the dimension of the RF coil, and the feature of the feeding rod.

*c. Liquid encapsulated zone melting (LEZM).* Since the bulk crystal growth of uniform composition of Si-Ge alloy is challenging using the conservative method, *viz.*, Bridgman and Czochralski (CZ), studies that are more recent indicated that the FZ technique is highly suitable, which aims at the synthesis of uniform Si-Ge alloy composition. However, to regulate the composition for growth, the method demands the measured feeding of Ge granules into a Si bar. Advancement toward the experiments have shown that the approach of LEZM can produce a single crystal having a uniform chemical composition, a uniform strength of dopants all through the crystal, and a low and uniform dislocation density. This non-conservative technique portrays the use of  $\text{CaCl}_2$  as an encapsulate and yields single crystal of a constant composition.<sup>92,93</sup>

An RF furnace with a vertical tube geometry has been tailored with a concentrator coil having a water-cooled jacket for zone refining, as depicted in Fig. 10. Theoretically, the coupling amongst the charge and the concentrator needs to be adequate to liquefy the Si charge; however, the limitation from the power source inhibits the melting of the charge immediately. Thus, a susceptor ring of graphite was mounted into the concentrator coil to deliver an uninterrupted supply of radiant heat. The alloy charge and the silicon seed were preloaded into a quartz ampoule, which are precisely attached within the graphite susceptor ring. As shown in Fig. 10, the ampoule was preloaded with a single-crystal seed of silicon at the bottom; subsequently, a disk of pure Ge and, afterward, a cylindrical bar of pre-synthesized Si-Ge alloy. The encapsulant  $\text{CaCl}_2$  was positioned above the charge such that it covers the internal region of the quartz ampoule as soon as the melting is initiated. A fiber optic thermometer system is used to monitor the temperature profile of the zone melting system. A fiber was placed into quartz tube at the centre of the pre-pierced Si-Ge charge, and the recorded temperature was documented while the fiber was detached from the hot zone at a speed of few  $\text{mm h}^{-1}$ . Thus, the sapphire fiber treated at the tip with a thin layer of refractory metal was employed to determine the



Fig. 9 Schematic of FZ growth of the Si-Ge bulk crystal with continuous charging of Ge granules. Adapted from ref. 29.





Fig. 10 Liquid-encapsulated zone melting growth set up. Reproduced with permission from ref. 93.

temperature of the alloy charge and from the seed through the molten zone.<sup>94</sup>

Thus, the LEZM technique proved to be a useful elucidation of two glitches related with the growth of single crystals of non-congruently melting alloys. Formerly, the liquid encapsulant minimizes the adhesion difficulty, reduces the reaction among the container and the melt, and regulates nucleation. In addition, the liquefied zone method regulates the compositional homogeneity of the entire solid solution.

*d. Multicomponent zone melting methods.* Aimed at the growth of multicomponent semiconductors, Nakajima *et al.*

and Suzuki *et al.* recommended the “multicomponent zone melting method” where the constituents are entirely soluble in the solid state.<sup>95</sup> This method satisfies two requirements, *i.e.*, to attain uniform alloy content in the development of binary and ternary compositionally graded bulk crystals.<sup>96–99</sup> Yonenaga and Murakami *et al.* could attain Si-rich  $\text{Si}_y\text{Ge}_{1-y}$  bulk crystals having a homogeneous composition with  $y = 0.03$  and  $0.07$  and with a length of 10 mm but without the introduction of feeding methods, which compensates the depletion of silicon solute elements during compositional alteration into the crystals.<sup>100</sup> To elucidate the influence of depleted solute elements of Si, two types of methods were adapted to grow the bulk crystals of Si-rich SiGe. Fig. 11(a and b) demonstrate the arrangements of the quartz crucible with growth materials both prior to and during growth along with temperature programming in the furnace.

Here, in Fig. 11(a), single crystals of Si and Ge were loaded in the quartz crucible and placed inside the graphite crucible. Temperature programming inside the furnace contains both a constant and a gradient zone. The carbon crucible was rotated to ensure consistent temperature profile perpendicular to the growth direction. Initially, portions of both Si and Ge crystals were liquefied and the solute element, *i.e.*, Si from the single crystal diffuses into the molten Ge to create binary Si–Ge melt. Prior to the withdrawal of the crucible, the binary melt is almost uniform and the composition of the molten alloy is dictated by the equilibrium composition of the melt, which is in proximity to the Si crystal at the interfacial temperature. During growth, the Si solute atoms unceasingly diffuse toward the interface of the Si–Ge binary melt and the subsequent supersaturation drives the growth of the crystal. Thus, the composition of Si in the melt decreases gradually. The Si crystal serves twofold purposes: (i) source material and (ii) seed.

Fig. 11(b) shows the growth of Si–Ge bulk crystals where temperature programming has a constant temperature zone and a fast-cooling zone with substantial temperature gradient. The method involves incessant stock of Si from the basis crystal for the binary growth of Si–Ge from the melt. Two Si single crystals and polycrystalline Ge crystals are placed in a quartz crucible airtight in a quartz ampoule maintained at high vacuum. With the onset of the melting of a portion of the two



Fig. 11 Quartz crucible with growth materials before and throughout growth, and the temperature outline inside the furnace. (a) Without any means of supply of depleted Si solute elements. (b) With supply means of depleted solute elements of Si. Reproduced from ref. 95.

Si crystals (both source and seed) and Ge crystal, the growth is initiated to form a binary growth melt of Si-Ge. In the melt, the diffusion of the Si atoms is initiated from the source crystal to the seed crystal due to the gradient of concentration of Si developed due to the temperature difference. The growth arrangement was heated up to 1453 K rapidly. For the growth, the geometry of the Si and Ge crystals was controlled to pin the temperature at the interface at 1373 K. In this technique, the Si seed crystal was not melted and the crucible was not pulled during the growth of the crystal. Rather, the method adapts the cooling of the growth system by rapid quenching.

*iv. Travelling solvent technique.* Travelling solvent technique is an influential and versatile method and is related to the growth of crystals, especially for materials that are difficult to melt owing to phase transformations or decomposition.<sup>101</sup> There are two main alternatives: the first approach, the travelling solvent method (TSM), is particularly applicable for thin perfect crystal growth and single-crystal rectifying junctions, and the second approach, THM is beneficial for the development of bulk single crystals, where it diminishes the detrimental outcome of constitutional supercooling.<sup>102a,b</sup> In brief, the latter approach is extremely effective for solid solutions of uniform composition and of peritectic compounds.<sup>83</sup> The liquid zone softens and melts the polycrystalline feed at its upper interface with high  $T$  and deposits, with approximately similar composition at the lower interface with low  $T$ , in near equilibrium conditions.<sup>103–105</sup> The method is capable of removing both dislocations and impurities. This process resembles that of zone levelling, where through a dilute solution, the recrystallization of a concentrated solution occurs and is usually performed vertically with a single pass of the liquefied zone.<sup>102</sup> The schematic and the principle of the technique is shown in Fig. 12. Solvents such as Ga and Sn were frequently used for the bulk ingots of  $\text{Si}_{80}\text{Ge}_{20}$ , having growth temperatures between 800 and 900 °C (in comparison to  $T^{\text{liq}} = 1350$  °C for  $\text{Si}_{80}\text{Ge}_{20}$ ).

Thus, THM is a complicated skill requiring the regulation of several technological parameters such as radiant heating, radius of the ampoule and wall thickness of the ampoule,

pulling system, fine-tuning of the basis material in the ampoule, as well as ground and temperature stability. Amongst all, a considerable requirement is the suitable temperature programming of the growth furnace. It should produce a narrow molten zone having a sharp temperature peak (approximately of dimension equals to the diameter of the ampoule) and a well-defined temperature difference at the growth interface to counteract constitutional supercooling.

A consolidation of all the single crystal growth techniques is shown in Table 2. This table envisages the technology complexity, sample qualities, and desired applications of different melt growth methods.

**2.3.b. Synthesis methods for thin film Si-Ge alloy.** The unveiling of nanotechnology initiated novel prospects, which were earlier unachievable by the thermoelectric community. The research on thermoelectric took a new turn in 1993 with the introduction of nanotechnology, which unlocked new perspectives, aiding thermoelectric devices to attain previously unreachable efficiency. The objective of thermoelectric micro-system conveys is to acquaint an energy harvesting usage to drive wireless sensor networks (WSN) for biomedical devices. The nanoscale prodigies began to be used *via* the methodology of thin-film depositions to enhance the efficiency of thermoelectric films.<sup>106–111</sup> The application of Si-Ge alloy is extensive. This section reviews the preparation of thin film Si-Ge alloy for thermoelectric devices and semiconductor industry since it was discovered in 1822.<sup>112</sup> The detailed description for obtaining the Si-Ge alloy on a substrate is given.

*(i) Liquid phase epitaxy.* In liquid phase epitaxy (LPE), the solution remains in a growth cell, which is generally a rectangular cavity.<sup>113</sup> The elevated rate of growth in LPE is appropriate for the growth of dense Si-Ge buffer layers with varying composition and forming Si-Ge top layers having thickness above 20  $\mu\text{m}$ , which is suitable for generating SiGe-on-Si epitaxial virtual substrate. Thus, two-dimensional models provide satisfactorily accurate predictions for most objectives. In this section, the technique presents the simulation models developed for the LPE growth of binary Si-Ge systems.<sup>114</sup> Nevertheless, under LPE

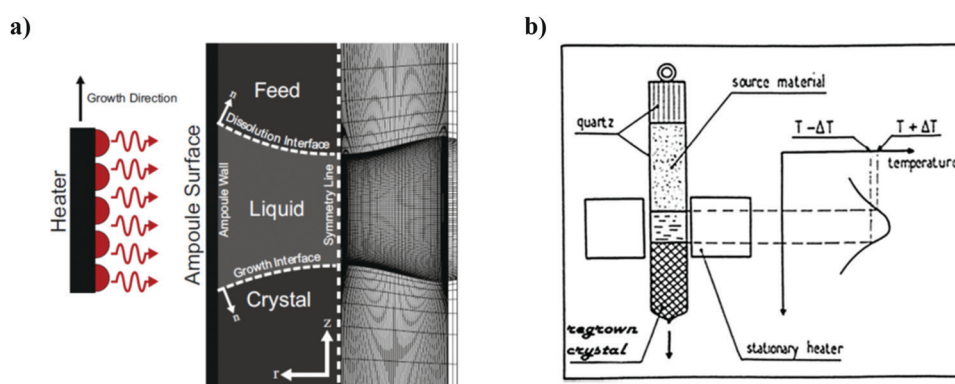


Fig. 12 (a) Left: Representation of the travelling heater method (THM). The heater moves in the upward direction of growth. Right hand side shows the finite element mesh representing 90 axial and radial elements within the liquid zone having a higher density of elements at the boundary. (b) Principle of the travelling heater method. Reproduced with permission from ref. 102 (a) and ref. 102 (b).



Table 2 shows the growth methods, technology complexity, sample qualities, and desired applications for different single crystal growth techniques

Crystal growth techniques	Technology complexity	Sample qualities	Desired applications
Melt growth method	<ul style="list-style-type: none"> <li>Controlling heat flow becomes progressively difficult as the diameter of the crystal enlarges</li> <li>The method can reliably yield but does not essentially result in homogeneous properties throughout the crystal</li> </ul>	<ul style="list-style-type: none"> <li>Synthesis of the single crystal ingots with homogeneous composition is not straightforward owing to the massive density difference of molten Si and Ge</li> <li>The vertical Bridgman technique enables the growth of crystals in circular shape, whereas horizontal Bridgman technique grows D-shaped ingots. Nevertheless, the horizontally grown crystals show high crystallinity, <i>i.e.</i>, low dislocation density as the crystal undergoes lesser stress owing to the open surface present at the top of the melt and can be expanded in the entire process of growth</li> </ul>	Widely used for the synthesis of GaAs single crystal in the semiconductor industry
Czochralski method	<ul style="list-style-type: none"> <li>Growth of single crystal from melt having multi-elements such as Si-Ge are related to the existence of "structure loss", <i>i.e.</i>, enhancement in the presence of dislocations and grain boundaries and so, extremely low pulling rate is required</li> </ul>	Si <sub>x</sub> Ge <sub>1-x</sub> alloys developed having [001] oriented Si seed crystal	Workhorse for the synthesis of overwhelming majority Si single crystal.
Zone refining	<ul style="list-style-type: none"> <li>Engage more space</li> <li>Difficult to load and unload materials and crucibles</li> <li>Intricate design and high cost of operation</li> </ul>	Exceptionally efficient purified alloy is obtained	Silicon-on-insulator (SOI) films, ultra-pure materials, Superconducting and semiconducting substances
Traveling solvent technique	<ul style="list-style-type: none"> <li>Complicated skill requiring the regulation of several technological parameters such as radiant heating, radius and wall thickness of the ampoule, pulling system, fine-tuning of the basis material in the ampoule, as well as ground and temperature stability</li> </ul>	Efficient for the growth of crystals, especially for the materials possessing difficulty in melting due to phase transformations or decompositions. It diminishes the detrimental outcome of constitutional supercooling	Growth of Si, Ge, and GaAs crystals



Fig. 13 Representation of the principle of LPE.

condition, lattice disparities higher than 1% are identified to restrict the nucleation of epitaxial layers. The schematic of the LPE technique is shown in Fig. 13.

In the last few years, LPE has been grown on Si<sub>1-x</sub>Ge<sub>x</sub> or Ge on Si using the fast melt growth method;<sup>115</sup> however, the epitaxial areas were restricted to diminished structures and

recurrent pre-growth lithographic and deposition handlings were essential. Of late, to deposit strained Si<sub>1-x</sub>Ge<sub>x</sub> layer above the thorough Si(100) substrates in a lone step, a lateral LPE technology has been established. The technique yields either Si<sub>1-x</sub>Ge<sub>x</sub> or Si<sub>1-x</sub>Ge<sub>x</sub> graded buffers. The essence of the film developed by LPE on an average shows low dislocation densities in comparison to other techniques, *viz.*, molecular beam epitaxy (MBE) and chemical vapor deposition (CVD), due to growth in proximity to the equilibrium, which makes dislocation nucleation difficult. Moreover, LPE encompasses low investment, high rate of growth than MBE and CVD, and is less toxic than CVD.<sup>116</sup>

(ii) *Molecular beam epitaxy*. In this epitaxial process, materials are grown under ultra-high vacuum (UHV) conditions on a pre-heated crystalline substrate using the reaction of the adsorbed species provided by atomic or molecular beams.<sup>117-119</sup> The layers possess (i) a structure with analogous symmetry or comparable crystalline structure of the substrate and (ii) a lattice parameter of the film deposited; the substrate should differ by less than ~10%. In general, the beams contain thermal energy and are formed by the sublimation/evaporation of suitable constituents placed in ultrapure crucibles.<sup>120,121</sup>

The method is extensively applied for the formation of not only single thin films but also multilayers of semiconductors and metallic materials. In this technique, since the growth



occurs under an UHV condition, *i.e.*, of the order of  $10^{-8}$  Pa, the growth rate can be slowed to a sub-nanometer scale thickness per second. Thus, the method has great potential for producing wide varieties of nanostructures such as quantum dots, multi stacking atomic layers, and nanowires.<sup>122</sup>

In this section, we focus on MBE as a tool (Fig. 14) for the formation of nanostructures made with Si-Ge and related materials. A strain-relaxed Si-Ge layer on Si is a model structure for technological applications. The technique is perhaps the most accepted method for Si/SiGe growth in academia and research labs. MBE is essentially a physical-vapor deposition procedure, provided the development of the layer is *via* the direct evaporation of Si and Ge (from ultrapure solid sources) simultaneously, along with the coveted additives under UHV conditions. The straight impingement of the constituent elements on a hot substrate alters the evaporants to a supersaturated state, which is concentrated, followed by nucleation and growth. Thus, in accordance to the first-order approximation, the rate of growth is independent of the orientation of the substrate; however, it depends weakly on the substrate temperature. Recently, Si/SiGe heterostructures were successfully grown using MBE systems with gas sources.<sup>123</sup>

During epitaxy, dopants are normally added into the film by low-energy ion implantation using an effusion cell by evaporation.<sup>124,125</sup> In few instances, ion implantation cannot be used for doping as the Si-Ge films may undergo damage due to induction by ion source. However, in such cases, evaporation by solid source is beneficial, and mostly Ga is used as the p-type dopant while the Sb is chosen as the n-type dopant, considering the vapor pressure of the dopants.<sup>126</sup> Exclusive effusion cells of boron, which illustrates good doping outlines and device characteristics for HBTs of B-doped SiGe, have also been prepared.<sup>127</sup> Thus, MBE can cause very rapid changes in the dopant profiles as the shutters right next to the effusion cells can cause disruption in the dopant fluxes. Some of the inherent probable benefits of MBE in comparison to UHV-CVD for the growth of Si/SiGe heterostructure includes (i) reduced growth temperature, (ii) better regulation of Ge and profile of dopant, (iii) thickness of the film, and (iv) the aptitude to

form additional elegant Si-based structures and superlattices (including separator and layers of metal on Si).<sup>128</sup>

In 1992, the renowned scientists Dresselhaus, Harman, and Venkatasubramanian were the first to propose the concept of superlattices in thermoelectric research.<sup>109</sup> Superlattices are defined as multilayer structures where two different materials grow by turn and the depth of the layer is at the nanometer scale. There is a noteworthy disparity amongst the conductivity of the layers, where one serves as a conduction layer and, subsequently, the other behaves as a barrier layer. Although different techniques are available to prepare the superlattices, MBE was found to be the finest way to obtain well-defined interfaces despite being expensive and having reduced efficiency.<sup>111</sup>

In the superlattice, the exceptional arrangement along with the band alignment, leads to progress in *ZT*. In accordance to the quantum confinement effect,<sup>129</sup> with the existence of nanostructure, the DOS varies as shown in Fig. 15(a) and the patterns of carrier compartments can be determined from the dispersal of DOS, which is represented in Fig. 15(b).

The idea of carrier pocket/compartment engineering, first suggested by Koga *et al.*,<sup>130</sup> utilizes the confinement effects, whereby the *zT* is improved owing to the enhancement in the DOS by exploiting the decreasing dimensionality. This technique is employed to enhance the number of active conduction valleys specifically. Fig. 16 demonstrates the failure of the confinement problem in common multilayer structure in Si and Ge. Since the X-pocket is energetically low, electrons prefer to fill the X-pocket instead of the L-pocket. However, as the depth of the Si- and Ge-layer decreases, the effect of confinement arises and the structure of the carrier pocket differs from the bulk materials.<sup>131</sup>

However, the disadvantages associated with MBE are (i) lower output compared with the UHV-CVD technique; for mass production, definite levels of quantity are required. (ii) Undesirable contamination due to the chemisorbed oxygen or carbon from the substrate<sup>132</sup> or from the residual gas impingement, which demand the cleaning of the substrate *in situ* prior to the deposition or a dip in the HF solution as an effective cleaning method.<sup>133</sup>

(iii) Vapor deposition. Vapor deposition or evaporation is a coating process where the substrate to be coated is hung over the evaporation source and the precursor powders are heated



Fig. 14 Schematic of the principle of MBE.



Fig. 15 (a) Arrangements of density-of-states (DOS) and (b) carrier compartments in 3-D bulk materials and 2-D quantum-well materials. The width of the conduction valley in (b) signifies the DOS. Reproduced with permission from ref. 111.





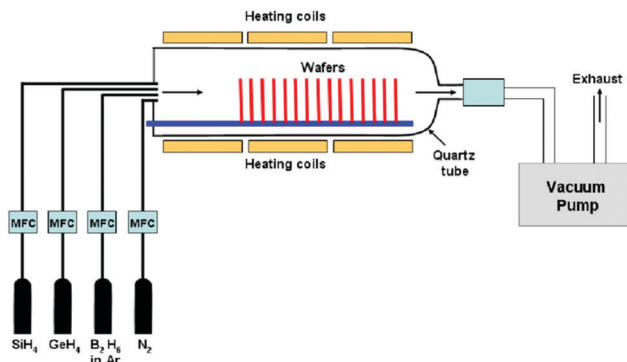
**Fig. 16** Configurations of the carrier pocket in the Si/Ge multilayer. The lower energy X-pocket is occupied by most of the electrons in the 3D structure. Nevertheless, in quantum well superlattices (2D structure), the energy separation between the X-pocket and L-pocket diminishes due to enhanced confinement energy in the X-pocket ( $E_{c,x} > E_{c,l}$ ) to the L-pocket. Occupancy of both the pockets by electrons increases the DOS, reduced the  $E_F$ , and enhances the Seebeck coefficient. Reproduced with permission from ref. 111.

until the vapor pressure is sufficient to smear under high vacuum. The deposition of thin films on varying substrate occurs *via* (i) physical vapor deposition (PVD);<sup>134–137</sup> and (ii) chemical vapor deposition (CVD),<sup>138–143</sup> where the vapor states are either condensed through condensation or chemical reaction. The technique is beneficial for being able to increase the deposition technique effortlessly and allocates a better control on the thickness of the film with homogeneous film morphology.

In PVD, atom-by-atom or molecule-by-molecule relocation of material occurs from the solid phase to the vapor phase, resulting in deposition on the substrates. Ion implantation, vacuum evaporation, and sputtering are the most notable techniques used in PVD.

On the other hand, CVD uses a chemical reaction to form a coating from a vapor, with the reaction by-products leaving as volatile species. High temperature is needed for CVD to initiate the chemical reaction. Kunhe *et al.* described the chemical vapor deposition of epitaxial SiGe-layers from  $\text{SiH}_4$ ,  $\text{GeH}_4$ ,  $\text{H}_2$ , and  $\text{HCl}$  gas mixtures at atmospheric pressure.<sup>144</sup> Kazmi *et al.* described that amongst a myriad of practices from various research groups, the low pressure chemical vapor deposition (LPCVD) technique for poly SiGe films deposition is believed to be superior and most extensively used to other deposition techniques due to reproducibility, uniformity, and its higher throughput with a setback of low deposition rate (2–30 nm).<sup>145</sup> The plasma enhanced chemical vapor deposition (PECVD) technique is an alternate of LPCVD if high deposition rate, an order of magnitude higher, is required with a compromise on the uniformity and throughput for a conformal deposition.<sup>146</sup>

In this technique, as reported by Kazmi *et al.*, poly  $\text{Si}_{1-x}\text{Ge}_x$  was deposited on  $\text{SiO}_2$  surface with a thin layer of amorphous silicon. B-doped poly  $\text{Si}_{1-x}\text{Ge}_x$  layer was deposited *in situ* using conventional LPCVD from the pyrolysis of pure silane ( $\text{SiH}_4$ )



**Fig. 17** Schematic view of the LPCVD system.

and pure germane ( $\text{GeH}_4$ ) gases with 0.2% diborane ( $\text{B}_2\text{H}_6$ ) diluted in argon gas (Ar) as a dopant precursor (Fig. 17). The experiments were executed at varying  $\text{B}_2\text{H}_6$  mixture flow rates of 0, 50, and 100 sccm with preset  $\text{SiH}_4$  to  $\text{GeH}_4$  ratio (75 : 37) and the deposition time of 70 min to originally check for the dopant distribution and Si and Ge contents in the thorough thickness of the deposited layers.

Dutarte *et al.* mentioned that rapid thermal chemical vapor deposition (RTCVD) can be used to grow silicon and  $\text{Si}_{1-x}\text{Ge}_x$  structures at a low temperature using  $\text{SiH}_4$  and  $\text{GeH}_4$  in an  $\text{H}_2$  ambient.<sup>147</sup> Haratmann *et al.* in their detailed review reported about Reduced Pressure-Chemical Vapor Deposition (RP-CVD) for the growth of Si/SiGe heterostructures for nanoelectronics. In this technique, pure silane or dichlorosilane are used as Si gaseous precursors ( $\text{SiH}_2\text{Cl}_2$  for (SEG)  $\leftrightarrow$   $\text{SiH}_4$  for Non-Selective Epitaxial Growth (NSEG)). Germane ( $\text{GeH}_4$ ) and mono-methylsilane ( $\text{SiH}_3\text{CH}_3$ ) diluted at 2% and 5% in  $\text{H}_2$  are used as Ge and C gaseous precursors.<sup>148</sup> For n-type and p-type doping, phosphine ( $\text{PH}_3$ ) and diborane ( $\text{B}_2\text{H}_6$ ), with concentrations in  $\text{H}_2$  between 5 and 2000 ppm, were chosen. Pure gaseous  $\text{HCl}$  can be added to the gaseous mixture in order to promote selectivity *versus*  $\text{SiO}_2$  or  $\text{Si}_3\text{N}_4$ . To clean at high temperature and pressure, large flows of  $\text{HCl}$  were used in between wafers at the inner surfaces of the chamber quartz domes. Finally, very high purity  $\text{H}_2$  in adequate quantity was used as the carrier gas.

(iv) *Sputtering.* Although polycrystalline  $\text{Si}_{1-x}\text{Ge}_x$  films were frequently synthesized by means of CVD, RF sputtering (Fig. 18), followed by annealing, offers a trouble-free, inexpensive, and ecofriendly fabrication method.  $\text{Si}_{1-x}\text{Ge}_x$  films deposited using this technique are amorphous, which crystallizes under different annealing conditions.

RF sputter deposition involves a network-harmonized current source at a customary frequency of 13.56 MHz and is frequently used through the cathode-anode space. By persistently reversing the positive ions or negative electrons reaching on it, the RF power source prevents the accumulation of charges on top of the insulating materials. Moreover, the oscillatory motion of the electron is discriminately increased by the RF power (due to its smaller mass *vs.* the heavier ions in the plasma) throughout the chamber. The impact-ionization rate is thus recovered and causes higher plasma density. This methodology is usually





Fig. 18 Schematics of the RF sputtering system.



Fig. 19 Representation of the ion-beam sputtering system.

employed to attain sputtering rates at high-speed and insulating materials.<sup>149,150</sup> Here, the anode is generally connected to the walls of the chamber to enhance the effectual area of the anode. However, a larger voltage drop occurs at the cathode (source) if the effective area for the anode is large; thus, a majority of the sputtering will take place on the source.

Choi *et al.* in his report explained about the deposition of  $\text{Si}_{1-x}\text{Ge}_x$  films of four different stoichiometries,  $\text{Si}_{0.37}\text{Ge}_{0.63}$ ,  $\text{Si}_{0.40}\text{Ge}_{0.60}$ ,  $\text{Si}_{0.72}\text{Ge}_{0.28}$  and  $\text{Si}_{0.87}\text{Ge}_{0.13}$ . In order to deposit amorphous  $\text{Si}_{1-x}\text{Ge}_x$  films on  $\langle 100 \rangle$  Si wafers (p-type) having a thin layer oxide grown thermally, the RF sputtering system was employed. Intrinsic Ge pieces affixed to a 4-in. n-type Si wafer were used as a sputtering target. Here, the Ge fraction was regulated by the comparative surface areas of Ge and Si subjected to argon plasma. The RF power employed was 150 W and sputtering and base pressure were maintained at  $1 \times 10^{-2}$  and  $1 \times 10^{-6}$  torr, respectively. The as-deposited films were crystallized in an  $\text{N}_2$  ambience at an annealing temperature between  $600^\circ\text{C}$  to  $900^\circ\text{C}$  kept for 24 h.<sup>151</sup>

Sasaki *et al.* explained the epitaxial growth of Si-Ge thin films using sputtering by ion-beam on the Si(100) substrate, as shown in Fig. 19. Using the alternate sputtering method, SiGe films were synthesized by layer-after-layer sequence. A rotatable target system was adapted to prepare multilayer structure and *in situ* doping. Substrate preheating is essential to initiate the deposition.  $\text{Si}_{1-x}\text{Ge}_x$  films were synthesized using the sputtering of the targets of Si and Ge interchangeably. During the target rotation, the shutter interrupts the Ar ion-beam for approx. 10 s. However, by regulating the sputtering time, the thickness and the average composition of the film can be determined.<sup>152,153</sup>

A consolidation of all the thin film growth techniques is shown in Table 3. This table envisages the growth methods, technology complexity, sample qualities, and desired applications of different thin film growth techniques.

#### 2.4. Strength of binary Si-Ge alloy

Si-Ge technology (Fig. 20(a and b)) has arrived a long way since its fortuitous discovery and commercialization. Subsequently,

circuit designers have unearthed that this alloy is more efficient than pristine silicon in terms of performance and power consumption, while also intensifying the oscillating and frequency competences of a device.<sup>154-165</sup>

Thus, the benefits of Si-Ge include

- Power saving and high performance
- Numerous possible ways of integration
- Reduced size
- Enhanced electronic mobility
- High oscillating and frequency capability
- Overall low component cost
- High temperature thermoelectric performance

The enhanced electronic mobility in Si-Ge in comparison to Si has managed its place in consumer electronics, telecommunication, computer technologies, space, and aerospace devices.

**2.4.1. Significant relevance of the binary IV-IV Si-Ge alloy.** Certain industries, such as space, automotive, telecommunication, and industries dealing with solar panels, need a semiconductor competent to work at high temperatures, while impelling for efficiency in terms of performance, miniaturization, or regulatory compliance.

Several architects and scientists consider Si-Ge a crucial material for that “novel technology”, which imparts cutting-edge high efficiency, space-savings, and thermal stability to progress innovations in space, automotive, telecommunications, and solar industries.

*a. Space industry.* Thermoelectric devices can acquire the largest power range (W) from the waste heat source. Planetary explorations have great aptitude for their usage as a considerable amount of electrical energy is produced. However, serious threat persists because of the use of radioactive materials. Over the past several decades, Si-Ge type alloys have aided as the desired material for thermoelectric conversion in U.S. radioisotope thermoelectric generator (RTG) power systems for deep space planetary voyaging missions. Silicon germanium (SiGe) alloys, since 1976, were featured in the unicouple device, and showed progress as the thermoelectric materials of preference



**Table 3** Shows the growth methods, technology complexity, sample qualities, and desired applications for different thin film growth techniques

Thin film growth techniques	Technology complexity	Sample qualities	Desired applications
Thin film growth method			
Liquid phase epitaxy (LPE)	<ul style="list-style-type: none"> <li>This growth method under near-equilibrium causes poor control on the thickness of layer and toil in yielding layers having thickness in sub-0.1 <math>\mu\text{m}</math></li> <li>Incompatibility with the development of several hetero-structures owing to mismatch in lattices or non-equilibrium conditions amid underlying seeding</li> </ul>	Crystals developed by LPE displays 3-dimensional and edge effects in the areas in proximity to the wall of the crucible. Otherwise, LPE process generally produces flat and homogeneous crystalline layers. Thus, 2D-models offer moderately exact predictions for most purposes	III-V solar cells, semiconductor devices such as LEDs, semiconductor lasers, and HBTs, were developed with LPE. The technique is also used for the growth of ferrites, oxides, garnets superconductors, II-VI semiconductors, and II-V compounds
Molecular beam epitaxy (MBE)	<ul style="list-style-type: none"> <li>The significant complexity includes the necessity for high-volume pumping, diminished uniformity, and high-complicated surface chemistry, comprising the demand to pre-crack several precursor molecules</li> <li>The technique also demands enormously clean ultrahigh-vacuum (UHV) condition in the material growth chamber</li> </ul>	Well appropriate for the growth of superior structures having the profile of doping and composition regulated at the $10^{-9}$ scale. This growth mechanism enables the preparation of both less (<2-3%) and extremely lattice-mismatched structures of (1) 2D structures having atomically flat interfaces and (2) 3D nanoislands, which completely restrict the carriers, respectively	MBE can grow crystalline films of extensive kind of materials including Si, II-VI semiconductors, Si-Ge, cuprate superconductors, III-V semiconductors, and metals
Vapor deposition	<ul style="list-style-type: none"> <li>Method is applied at high temperature</li> <li>Challenging to the mask surface</li> <li>The reaction chamber capacity dictates the size of the sample</li> <li>The sample needs to be relocated at the deposition site and so is not an "on site" process</li> </ul>	High purity films can be deposited.	Used for the synthesis of a wide range of materials such as semiconductor devices or for coating to enhance the wear and tear of the materials
Sputtering	<ul style="list-style-type: none"> <li>The bombardment site of the target is too small and the rate of deposition is usually low</li> <li>Damage of the substrate may occur due to ion bombardment or ultraviolet radiation formed by the plasma</li> </ul>	<ul style="list-style-type: none"> <li>Capable of depositing several metals, alloys, insulators, and composites</li> <li>The deposited film is the replica of the target</li> <li>Film quality and step coverage are superior to evaporation</li> <li>Large targets can deposit a uniformly thick layer over the substrate</li> </ul>	Widely used by semiconductor industries and for integrated circuits for the deposition of elements ( <i>e.g.</i> , Ta), compound ( <i>e.g.</i> , TaN), multilayer ( <i>e.g.</i> , Ti-Cu-Au), and alloy ( <i>e.g.</i> , Al:1%Si:1%Cu)

**Fig. 20** (a) Si-Ge solar panels (image courtesy NASA), (b) Si-Ge chips (image courtesy IBM).

for U.S. RTG-driven space delegations. These encompass the Lincoln Experimental Satellites 8 and 9 in U.S. Air Force for communications (1976), followed in 1977 using the Space Administration Voyager 1 and 2 planetary missions and National Aeronautics 4J. In 1989, advanced Si-Ge RTGs remained employed to drive the Galileo's discovery of Jupiter and, in 1990, was used to operate the Ulysses' unearthing of the Sun. Furthermore, Si-Ge expertise has been selected toward delivering RTG power for the

1995 Asteroid Flyby mission and Comet Rendezvous in addition to the 1996 Cassini Saturn orbiter mission.<sup>166-170</sup>

In conjunction with the Modular RTG Program, the thermoelectric development activities in U.S. Department of Energy comprise (1) the improvement of transformation devices established on close packed couple of arrays having high density, and (2) the growth of enhanced functioning of "multicouple" Si-Ge type thermoelectric materials (Fig. 21(a-c)).<sup>171</sup>





Fig. 21 Detailed demonstration of (a) high density close-packed array (CPA) thermoelectric modules and (b) 21 Couple spring-loaded thermoelectric modules (c) segmented unicouple technology (image courtesy NASA).



Fig. 22 Si-Ge rectifiers in automobile sector (image courtesy Nexperia).

*b. Automotive industry.* Si-Ge rectifiers coalesce the efficacy of Schottky rectifiers having thermal constancy of fast recovery diodes, empowering scientists and engineers to augment their power outlines of 100–200 V for enhanced efficiency, as shown in Fig. 22. The devices target applications in automotive sector, communications infrastructure, and server markets. By proposing

a comprehensive secured-operating area encountering no thermal runaway till 175 °C, the AEC-Q101 acquiescent Si-Ge rectifiers were found to be particularly suitable for high temperature applications.

Recently, Si-Ge proved to have ideal rectifier performance by automobile industries and designers of varied systems working at elevated temperatures for better efficiency.<sup>172</sup>

As Fig. 23(a and b) displays, novel gadgets exhibit improved thermal stability, widening the secure operating area – from 145 °C, the temperature where the thermal runaway initiates the Schottky rectifiers to greater than 175 °C for SiGe rectifiers, the stipulated threshold of the Clip-bonded Flat Power (CFP) package.

Concerning the efficacy, Fig. 23(c) shows that usually a Fast Recovery rectifier exhibits approx. 0.9 V forward voltage. However, the Si-Ge diode presently shows the least leakage current (1 nA) of the family, where the curve is equated to a forward voltage ( $V_F$ ) of about 0.75 V and a gain of 150 mV. The outcome is a decrease in the losses due to conduction of nearby 20%. As an estimate,



Fig. 23 (a) Structural difference between a Schottky and SiGe rectifier; (b) plot of leakage current as a function of case temperature for a Schottky and a SiGe rectifier. When the leakage current turns out to be super-exponential, thermal runaway occurs; (c) compromise in forward voltage vs. leakage current for Schottky rectifier, Nexperia SiGe, and Fast Recovery rectifiers. The SiGe rectifier demonstrates approx. two orders of magnitude less leakage current in comparison to the Schottky rectifier, and approx. 20% reduced forward voltage drop in contrast to Fast Recovery rectifier. Adapted from ref. 173.





Fig. 24 Schematic of Si-Ge heterojunction bipolar transistor for Bi-CMOS technology. Adapted from ref. 179b.

5–10% enhanced efficiency could be envisioned, having analogous thermal stability in comparison to the finest-reported fast recovery diodes.<sup>173</sup>

*c. Electronics and telecommunication industry.* The Si-Ge heterojunction bipolar transistor (HBT), as shown in Fig. 24, happens to be the foremost realistic bandgap-engineered gadget to be accomplished in the silicon material system.<sup>155</sup>

Circuit designers and microelectronic device have long strived to unite the exceptional transport properties and design suppleness accessible by bandgap engineering (as normally performed in semiconductors, *viz.*, GaAs and InP),<sup>174,175</sup> with superior yield and low cost of conventional Si fabrication. The vision could finally be materialized by the introduction of epitaxial silicon germanium (Si-Ge) alloys.

The amalgamation of Si-Ge HBTs having the best-of-breed silicon CMOS to form a Si-Ge HBT BiCMOS demonstrates an obvious fit for delivering upcoming system-on-a-package and system-on-a-chip integrated circuit solutions.<sup>176–179</sup>

While the Si-Ge technology experiences a rising significance in performance-constrained digital, analog,<sup>180</sup> and RF through mm-wave circuits and systems, budding Si-Ge applications for which reliability concerns exist both nuanced challenges and thrilling prospects include the quantum realm, power electronics, space systems, and integrated photonics.

Thus, a multinational company, MACOM,<sup>181</sup> utilized its expertise in extremely high frequency (EHF), *i.e.*, mmW circuit design and microwave, which joined in the Si-Ge commercialization endeavor throughout the 1990s with the fabrication and development of several monolithic microwave integrated circuit (MMIC) designs that attained extensive recognition in several handset and base station diligences.<sup>182</sup> MACOM has also led the avenue in applying Si-Ge BiCMOS technology for both military and commercial demands.

Another, multinational industry Maxim integrated already illustrated that Si-Ge is capable of RF front-end performance.<sup>183</sup> Moreover, due to low saturation voltage than silicon, Si-Ge seeks wide application in high-current devices. Moreover, better high-quality signal spectrum can be processed using the Si-Ge binary alloy.

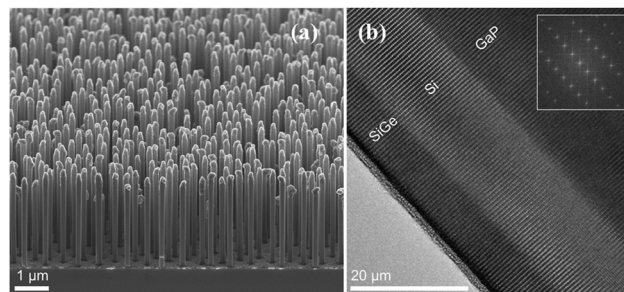


Fig. 25 (a) SEM image of the GaP/Si/SiGe core/multishell NWs with hexagonal structure; (b) the HAADF HRSTEM image of the SiGe/Si/GaP interfaces and the corresponding FFT as the inset. Reproduced with permission from ref. 184.

A recent study by Fadaly *et al.* revealed, hexagonal Si-Ge alloy synthesized using the crystal transfer method with gallium phosphide (GaP) core nanowire having a wurtzite structure as a template, showing direct band gap, which is dissimilar to the traditional cubic lattice structure of the group-IV elements in the electronics industry (Fig. 25(a and b)). This leads to temperature-insensitive radiative recombination lifetime in sub-nanosecond, which causes light emission (an elusive for decades) comparable to group-III-V semiconductors having direct-bandgap. Thus, the light-emitting SiGe alloy opens a new avenue for a photonic chip, the latest revolution in integrated chip function.<sup>184,185</sup>

*d. Solar Industry.* Si-Ge possess both an elevated electron and hole mobility than Si, *i.e.*, with less energy loss and 4× faster carrier mobility in comparison to single crystal silicon; it can be utilized for enhanced processing power, reduced dimension, and power fetching for a unit of similar size.

In photovoltaics (PV), Si-Ge is a favorable candidate to meet the outstanding need with enhanced adsorption characteristics and better conversion efficiency as the cell structures demand materials having bandgap similar to Ge but open-circuit voltage ( $V_{OC}$ ) similar to that of silicon. However, due to the losses in  $V_{OC}$  and inadequacy in the crystal quality, SiGe lacks practical applications in PV cells.

Zhao *et al.* mentioned that the use of expensive traditional substrates in the III-V multi-junction devices regulates their application; in this regard, Si-Ge was chosen to be a promising material for bottom cell in a two-fold junction system owing for good process compatibility, excessive mobility, tunable lattice parameter, and competence to absorb light of wavelengths ~1800 nm, which are supposed to be the most notable factors for bottom cell material selection in a two-terminal configuration (Fig. 26(a and b)).<sup>186</sup>

Diaz *et al.* reported an efficacy of 18.9% under one sun from the GaAsP-SiGe structure, whereas Wang *et al.* reported that for the GaAsP-SiGe cell, an efficiency of over 20% can be achieved in the III-V epitaxial layers having a threading dislocation density (TDD).<sup>187</sup>

**2.4.2. Trade-offs of the Si-Ge alloy.** Although Si-Ge alloy is beneficial in several applications that demand greater electron





Fig. 26 (a) Tandem device structure design of basic two-terminal GaAsP/SiGe on Si. Reproduced with permission from ref. 187; (b) optical paths in the Si-Ge structure. Reproduced with permission from ref. 186.

mobility, it also has trade-offs. For example, silicon is the foremost choice for the devices operating at extremely high temperatures. Moreover, although the cost of the IV-IV binary Si-Ge alloy is less than the III-V binary GaAs, it is more costly than silicon.

In other words, although Si and Ge are abundant elements in Earth's crust, they become expensive when synthesized in the laboratory as the process involves refining, followed by tedious single crystal or polycrystalline alloy formation. Fortunately, SiGe's growing acceptance has made it more available in the recent years, specifically in components geared for telecommunications, automotive, and solar environments.

### 2.5. Synergistic connection of the Si-Ge alloy in semiconductor and thermoelectric applications

In the Upcoming Industrial Revolution, the paradigm of Internet of Things (IoT) is likely to gain wide recognition owing to its vast applicability in a universal network. These IoT sensors are low energy wireless modules, typically driven by batteries, which are non-renewable energy storage units. However, these batteries pose constraints due to limited life-time; thus, frequent replacement is unviable. In this regard, the realization of miniaturized energy scavengers or energy harvester-controlled micro electro mechanical-system (MEMS) seems to be a solution to conjugate the prime requirement of IoT usage, *viz.*, self-sufficiency in energy and integration or miniaturization.<sup>188-193</sup> These energy harvesters are micro or nanoscale thermoelectric generators capable of supporting power requirement to IoT sensors in the range of few microwatts. Silicon and its Group-IV partner, which forms binary or ternary alloy, are promising to form  $\mu$ -TEG as they are compatible with the traditional CMOS fabrication methodology and can be integrated at the chip level effortlessly. These also harmonize the need for economic and miniaturized systems.

### 2.6. Conclusion

In conclusion, this review article has shown that with the prevailing COVID-19 crises, performing communication coordination for the extensive use of video conferences, home office, *etc.*, retain paramount significance for maintaining the economy and stability under lockdown situations. In addition, the

resilience concept is acquiring significance in the political domain and is presently resonating alongside the common public owing to the COVID-19 emergency. The country's strategic sectors, *viz.*, the communication system, is a supreme issue, and understanding its importance is highly indispensable.

Several projects such as Toward Advanced bimos Nano-Technology platforms for radiofrequency (RF) and terahertz (thz) applications (TARANTO) in Europe aims at further strengthening the semiconductor industry in the Si-Ge BiCMOS technology and offering a concrete industrial base for the progress of novel products in areas such as home electronics, telecommunications, and car electronics that are of fundamental significance for high-tech industries. In fact, engineers and researchers worldwide are aimed for the setting up of subsequent BiCMOS technology programmes having enhanced performances of Si-Ge Higher Integration level and Heterojunction Bipolar Transistor (HBT) needed to tackle Enhanced Speed & Enhanced Data Rate communication systems. In fact, the enhanced execution of BiCMOS technology programmes are a major enabler of those functions that need the blend of front-ends high-performance radio-frequency (RF) along with advanced CMOS nodes having elevated computational power and low power consumption.<sup>194</sup>

Leibniz Institute for High-Performance Microelectronics (IHP) has studied numerous device concepts for Si-Ge HBTs pertaining to their ability to have enhanced performance in RadioFrequency.<sup>195</sup> The speediest apparatus were attained in a practice having non-selective epitaxial growth (NSEG) of the Si-Ge base and elevated extrinsic base (EEB) regions made in a careful epitaxial process distinctly. In a bipolar-only procedure, the device concept is optimized following the illustration of ring oscillator gate delays of 1.34 ps and peak values of 505 GHz/720 GHz, which are descent values described for Si-Ge HBTs to date.<sup>196-198</sup>

IHP in collaboration with X-FAB will work on advanced Si-Ge bipolar CMOS (BiCMOS) technologies based on IHP's Si-Ge HBT's, which will be integrated on single circuit devices. Thus, Si-Ge BiCMOS remains a lucrative prospect in several wireless applications such as 5G due to the amalgamation of enhanced performance radiofrequency on an Si-based substrate.<sup>199-201</sup>



Moreover, through the Internet of Things (IoT), Bipolar Junction Transistors empower Bi-CMOS toward supporting the nation's strategic and civilian welfares as it links the appliances and sensors to data acquisition system or computers and the internet for creating an intelligent system, hence making smart decisions and responding seamlessly. Fig. 27 illustrates the smart environment using IoT-based IV-IV binary alloy. In fact, the superior features of Si-Ge in comparison to Si lies on the fact that substituting some Si atoms with Ge deforms the crystal lattice and enhances the pace of the electrons to facilitate  $1000\times$  rapider systems. These expeditious systems have wide applicability in systems related to high-end communications.<sup>202–205</sup>

Tower Semiconductor Ltd, a leading foundry of high-end analog semiconductor solutions from Israel, introduced a latest RF switch technology targeted at 5G (ranging from the sub-6 Hz bands and millimetre waves) smartphones and the cellular base stations that are capable of connecting them to ultrafast networks. The novelty of the switch technology is that Internet of Things devices can be used with limited battery life. The company claims to have the ability to integrate the RF switches with other production processes it offers customers, including SiGe BiCMOS and power CMOS. In this regard, several chips based on its SiGe, BiCMOS, RF CMOS, image sensor based on CMOS, assimilated power management, MEMS, as well as other production processes were introduced.<sup>206,207</sup> Moreover, according to BIS research, which gives an overview of the place for market intelligence on deep technology, which includes research of

more than 70 companies across the value chain, painstaking compilation of more than 700 research hours across 231 pages, and exclusive insight from in-depth expert interviews, forecasts that global silicon and germanium materials, is projected to grow to 5045.3 million dollars by 2021 on a compounded annual growth rate (CAGR) of 13.7 from 2016 to 2021. This technology is swelling into varied end-markets owing to communications devices, lightweight, automobile collision avoidance systems, and thermoelectric capabilities. Nevertheless, the rapid growth of internet, high mobile acceptance, and growth in the global self-governing driving industry are the key opportunities lined up in the Si-Ge market in the coming future.<sup>208,209</sup>

Moreover, Si-Ge seeks wide applicability in the energy harvesting sector as high temperature thermoelectric modules, especially in deep space planetary explorations. In this regard, initially, the space agencies synthesized single crystal Si-Ge alloy; subsequently, the work was extended to polycrystalline Si-Ge alloys as it is very much essential to understand the properties of the alloy extensively in a single crystal alloy. Nevertheless, the difficult synthetic procedures, to achieve single crystalline Si-Ge alloy with fixed compositions, were overcome by several groups worldwide using the various techniques, as discussed in the review.

Although, in recent years, polycrystalline Si-Ge has gained wide applicability in thermoelectric research, single crystalline Si-Ge alloy still enjoys widespread usage in the electronics and semiconductor industry.



Fig. 27 IoT-based smart environment using the Si-Ge based BiCMOS technology.



## Conflicts of interest

No conflict of interest.

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