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High-density conductance states and synaptic plasticity in SnP_2S_6 memristors for neuromorphic computing

Thaw Tint Te Tun, Jiali Huo and Kah-Wee Ang *

Memristors with programmable conductance are considered promising for energy-efficient analog memory and neuromorphic computing in edge AI systems. To improve memory density and computational efficiency, achieving multiple stable conductance states within a single device is particularly important. In this work, we demonstrate multilevel conductance tuning in few-layer tin hexathiophosphate (SnP_2S_6 or SPS) memristors, achieving 325 stable states through a pulse-based programming scheme. By analyzing conductive filament evolution, we devised a voltage-pulse approach that effectively suppresses current noise, thereby maximizing the number of distinguishable states within the device ON/OFF ratio. Furthermore, we experimentally emulated synaptic plasticity behaviors including long-term potentiation and depression, and validated their performance through artificial neural network simulations on digit classification. These results highlight the potential of SPS memristors as high-resolution analog memory and as building blocks for neuromorphic computing, offering a pathway toward compact and efficient architectures for next-generation edge intelligence.

New concepts

This work demonstrates finely tunable multilevel conductance states in tin hexathiophosphate (SnP_2S_6 or SPS) memristors, a material where systematic analog switching studies remain limited. By achieving up to 325 stable conductance states, this study highlights the capability of SPS to support high-resolution analog memory and neuromorphic computing. The ability to reliably access a large number of states within a fixed ON/OFF ratio provides additional insight into how conductance modulation can be extended in emerging 2D materials. Alongside conductance tuning, device-level synaptic behaviors such as long-term potentiation and depression were also explored, with their implications assessed through artificial neural network simulations. Together, these results establish SPS as an exploratory platform for investigating multilevel switching in 2D memristors, broadening the range of materials available for in-memory and brain-inspired computing research.

Introduction

The growing integration of artificial intelligence (AI) in edge devices has accelerated the development of embedded AI and ambient intelligence (AmI) systems, where real-time, low-power, and efficient computing is essential.[1] Conventional von Neumann architectures, limited by the separation of memory and processing units, suffer from high latency, energy inefficiency, and restricted throughput, making them less suitable for always-on applications.[2,3] To address these challenges, non-von Neumann paradigms such as in-memory computing have been proposed. Memristors are promising candidates owing to their simple two-terminal structure, scalability, and low power operation.[4–6] Their ability to modulate conductance in response to voltage enables analog memory functions and synaptic plasticity behaviors relevant for neuromorphic computing.[7,8] Depending on their operating mechanisms, memristive devices can be broadly categorized into electrical, optoelectronic, and ionic types. Electrical memristors, such as those based on filamentary or interfacial resistive switching, have been extensively studied for their scalability and CMOS compatibility.[9,10] Optoelectronic memristors combine optical and electrical stimuli to achieve light-assisted programming and enhanced control over conductance states.[11,12] Ionic memristors, in which ion migration directly modulates channel conductivity, offer high analog tunability and potential for bioinspired signal processing.[13]

Among these various device types, memristors with multiple stable conductance states are particularly attractive for neural network applications, especially at the edge, where they allow direct mapping of pretrained weights, reduce retraining overhead, and support adaptive tuning during deployment. Such high-resolution control also promotes consistent synaptic behavior across devices, improving learning accuracy and inference stability. Beyond neuromorphic computing, analog programmability in memristors offers opportunities for broader applications, including scientific and mortal computing.[14,15] Nonetheless, achieving

Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, 117583, Singapore. E-mail: eleakw@nus.edu.sg

precise and reliable analog tuning over a wide dynamic range remains a key challenge, particularly in two-dimensional (2D) material-based devices.

2D materials have recently attracted attention for resistive switching (RS) devices due to their atomic thickness, low switching voltages,[16,17] reduced device variability,[18] and ability to exhibit both threshold and bipolar RS behaviors.[16,19] Among them, nanoporous metal chalcogenophosphates (MP_2X_6; M = Sn, Ge, Pb; X = S, Se, Te) show potential for electronic applications.[20–25] Within this family, tin hexathiophosphate (SnP_2S_6 or SPS) is particularly notable due to its wide indirect bandgap of 2.2 eV, ambient stability, room-temperature ferroelectricity, and strong light–matter interactions.[26–30] Despite these favorable attributes, systematic demonstrations of finely tunable analog conductance states in SPS memristors remain limited.

Here, we explore the potential of SPS memristors for analog memory and neuromorphic applications by demonstrating multi-level conductance tuning using a high-precision pulse programming (H3P) approach combined with a denoising strategy. The H3P scheme employs conditional logic and predefined pulse sequences without requiring device-specific calibration, while the denoising process reduces current fluctuations that often limit the resolution of conductance states. This combination enables up to 325 stable states to be accommodated within the available ON/OFF window. While the approach is expected to be broadly useful for filamentary RS systems, its application to SPS represents an early demonstration of high-resolution conductance control in this material. Beyond conductance tuning, we emulate long-term potentiation (LTP) and depression (LTD) through tailored pulse trains and incorporate the measured responses into artificial neural network (ANN) simulations using MLP + NeuroSim V3.0. The simulations indicate that improved linearity in LTP/LTD responses correlates with higher classification accuracy, underscoring the importance of pulse scheme design when linking device behavior to system performance. This work thus provides an exploratory demonstration of finely tunable analog states and neuromorphic functions in SPS memristors.

Results and discussion

Device structure and the switching performance in SPS memristors

The cross-sectional structure of the fabricated SPS memristor was examined using bright-field transmission electron microscopy (BF-TEM), which confirmed the Ti/Au/SnP_2S_6/Ti/Au layer sequence (Fig. 1(a)). Elemental mapping *via* energy-dispersive spectroscopy (EDS) further verified the presence of Sn, P, and S in the switching layer and indicated an SPS thickness of approximately 8 nm (Fig. 1(b)). A schematic illustration of the effective device architecture is provided in Fig. 1(c), showing the exfoliated SPS flake sandwiched between the top Ti active electrode and the bottom Au electrode. Spectroscopic characterization was also performed on the exfoliated SPS flakes. The Raman spectrum (Fig. S2(a), SI) shows three peaks at $\sim$142, $\sim$169, and $\sim$265 cm^{-1}, consistent with previous reports.[26,27] The photoluminescence spectrum (Fig. S2(b), SI) also matches earlier results,[27,28] further confirming the material's properties.

Electrical characterization of the SPS memristor demonstrated reproducible bipolar RS behaviour (Fig. 1(d)). During a positive voltage sweep from 0 to 2 V with a compliance current (I_{CC}) of 1 mA, the device transitions from a high-resistance state (HRS) to a low-resistance state (LRS). Conversely, under a negative voltage sweep from 0 to -2 V, the device resets to the HRS without requiring an I_{CC}. All pristine devices undergo an initial forming process, with a mean forming voltage of $\sim$3 V (Fig. S3, SI). To assess temporal variations in switching voltages, the device was subjected to 100 direct current (DC) cycles. The results show a switching memory window exceeding 10^2 (Fig. 1(e)), with minimal variations in SET and RESET voltages (V_{SET} and V_{RESET}). Statistical analysis (Fig. 1(f)) indicates mean V_{SET} and V_{RESET} of 1.14 V and -0.94 V, with standard deviations of 0.0758 V and 0.0832 V, respectively. These variations are comparable to those reported for high-performance memristors (Table S1, SI). To elucidate the RS mechanism, EDS scans were performed on SPS memristors in both HRS and LRS states. The line scans (Fig. S4, SI) reveal a higher Ti concentration in the SPS switching layer in the LRS compared to the HRS, while the Au concentration remains unchanged in both states. This suggests that Ti ions are actively involved in the switching process, classifying the device as an electrochemical metallization (ECM)-type memristor. To further verify this conclusion, an SPS-based memristor with Au electrodes on both sides was fabricated. When subjected to voltage sweeps up to $\pm$6 V, the device did not exhibit any RS behaviour (Fig. S5, SI), confirming that Au ions do not contribute to the switching process.

In addition to evaluating temporal or cycle-to-cycle (C2C) variations, spatial or device-to-device (D2D) variations were analysed through electrical measurements on a 6 $\times$ 6 CBA of SPS memristors fabricated on a uniformly thick SPS nanosheet (Fig. 1(g) and Fig. S6, SI). DC sweep cycles were recorded for all 36 devices, each undergoing six switching cycles (Fig. S7, SI). Both *I–V* characteristics and statistical analyses of the HRS and LRS currents confirm consistent switching behaviour, with a switching memory window comparable to that observed in C2C measurements ($>10^2$) (Fig. 1(h) and Fig. S7, SI). Furthermore, across all 36 devices, statistical analysis yields mean V_{SET} and V_{RESET} of 1.08 V and -0.79 V, with standard deviations of 0.0994 V and 0.0968 V, respectively (Fig. 1(i) and Fig. S8, SI), indicating minimal D2D variations in switching voltage. Retention measurements on a representative device confirm stable LRS and HRS levels for 10^4 s without degradation (Fig. S9(a), SI), while endurance tests on the same device show reproducible switching up to 10^4 cycles (Fig. S9(b), SI), suggesting the potential for stable non-volatile memory operation.

Multiple conductance states using a high-precision pulse programming scheme with denoising process

In the context of in-memory computing, the number of distinguishable current levels plays a key role in determining a memristor's information storage capacity. In this study, we employed the H3P scheme to achieve 325 distinct conductance

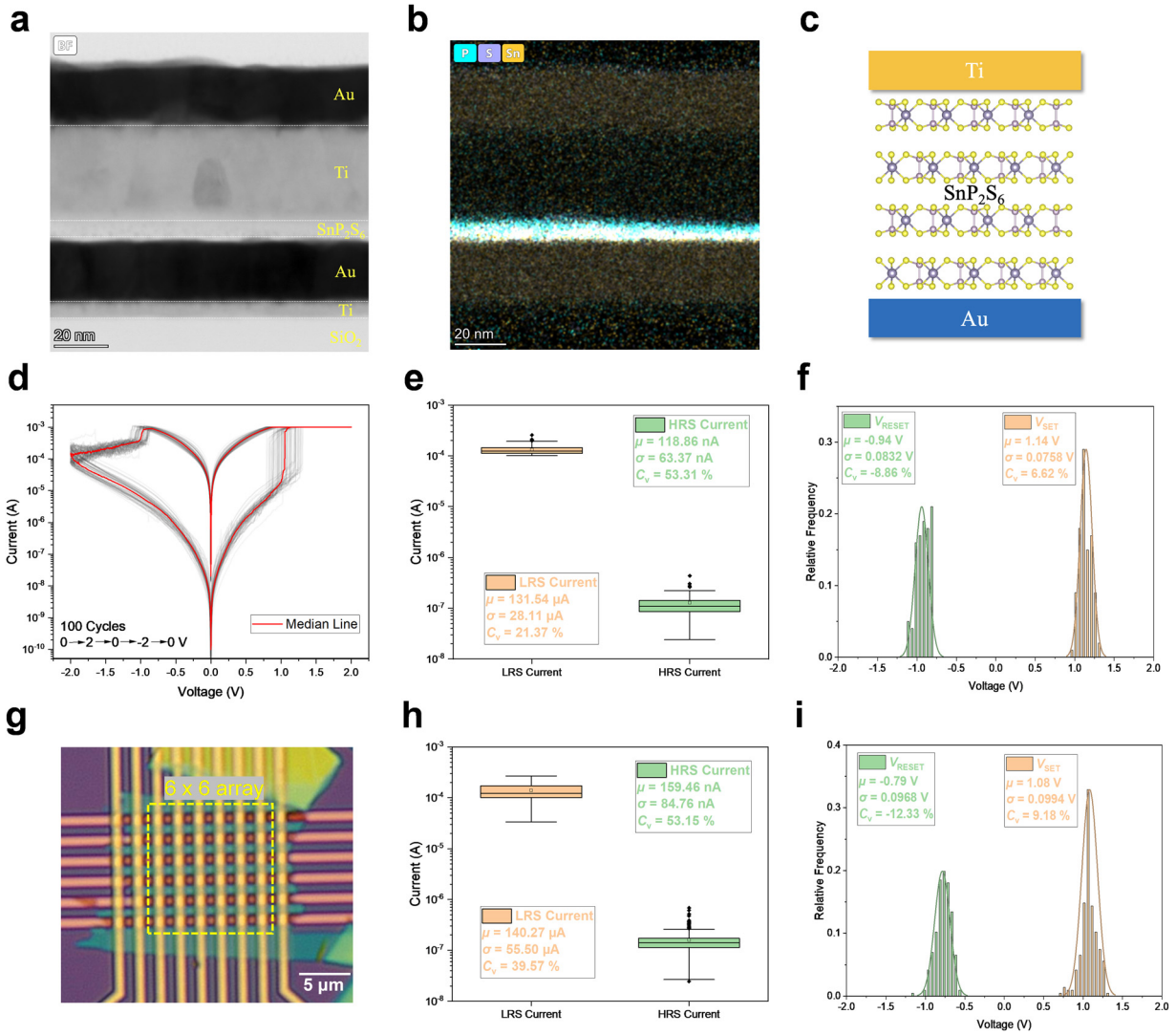

Fig. 1 (a) Cross-sectional BF-TEM image of the as-fabricated Ti/SnP_2S_6/Au memristor. (b) Cross-sectional EDS map highlighting the SnP_2S_6 layer. (c) Schematic illustration of the memristor device structure. (d) *I*–*V* curves of the memristor over 100 switching cycles with an I_{CC} of 1 mA during SET processes. The corresponding distributions of (e) HRS and LRS currents, and (f) V_{SET} and V_{RESET}. (g) Zoomed-in optical microscopy image of a 6 × 6 CBA of SnP_2S_6 memristors. The distributions of (h) HRS and LRS currents and (i) V_{SET} and V_{RESET} for *I*–*V* curves measured across 36 devices from the CBA. In both (e) and (h), each box represents the distribution of multiple repeated measurements of LRS and HRS currents. The central line inside each box indicates the median current, while the box edges correspond to the interquartile range (IQR). The dot within each box represents the mean current, and the vertical whiskers extend to values within 1.5 × IQR, with any points beyond this range plotted as outliers. In (e), (f), (h), and (i), μ denotes the mean, σ denotes the standard deviation, and C_v denotes the coefficient of variance.

states in SPS memristors, providing a demonstration of multi-level tuning in a 2D material system. Table S1 (SI) provides representative reports of multilevel tuning in other 2D memristor systems. Our H3P scheme utilizes ramped stair pulses with positive or negative biases to induce SET or RESET transitions, respectively. For example, when tuning the device conductance from a higher LRS current of 130 μA to a lower LRS current of 72 μA, negatively ramped stair pulses ranging from −0.2 V to −4.5 V are applied. If the conductance falls below the target of 72 μA, positively ramped stair pulses (0.2 V to 4 V) are subsequently applied. This process is iterated until the conductance stabilizes within an acceptable range around the target value (72 ± 0.2 μA). An illustration of this process is shown in Fig. 2(a) and (b).

However, without an effective denoising strategy, the programmed current levels exhibit noticeable fluctuations (Fig. 2(c)), reducing the minimum distinguishable range between adjacent conductance states. In ECM-based memristors, such as the SPS memristor studied here, such fluctuations can be mitigated by disrupting weak filaments while preserving stronger ones, a process referred to as the denoising mechanism.[14] In our scheme, after reaching the target range, we applied a sequence of positive–negative denoising pulse pairs that effectively suppressed current fluctuations within an acceptable precision margin (target current ± 0.15 μA), which was empirically determined as the minimum stable margin during the denoising process. The full details of the H3P scheme and its denoising procedure are

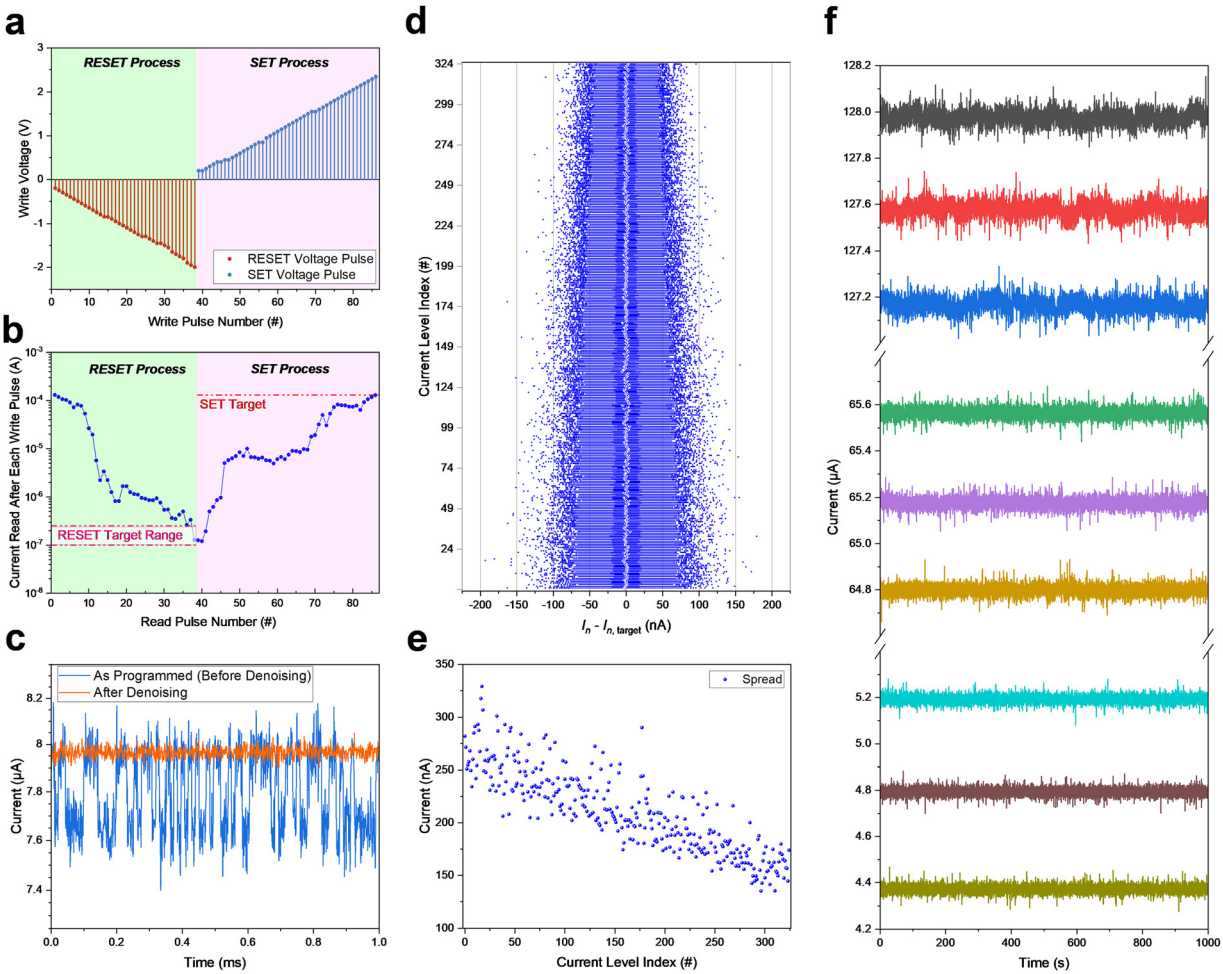

Fig. 2 (a) Example of SET and RESET operations using stair pulses with ramped-up voltage amplitudes under the H3P scheme. (b) Corresponding current measured by a 0.2 V/1 μs read pulse following each SET or RESET pulse in (a). (c) As programmed and after denoising currents of the memristor, read using a constant voltage of 0.2 V. (d) Distribution of current deviation ($I_n - I_{n,\text{target}}$) across 325 programmed conductance states achieved in a memristor using the H3P scheme with denoising. Each box represents 1000 data points (10 s retention monitoring per level), with box edges indicating the IQR, whiskers extending to 1.5 × IQR, and the central dot marking the mean. (e) Current spread corresponding to the deviations shown in (d). In both (d) and (e), current level index 0 corresponds to the highest current level, while index 324 represents the lowest. (f) Retention measurements of three representative current levels from each of the high, medium, and low conductance ranges after denoising.

shown in Fig. S10 (SI). This approach enabled the generation of 325 distinct current levels in SPS memristors (Fig. 2(d)), suggesting their suitability for multi-bit memory and analog in-memory computing applications.

To evaluate the robustness of the multilevel states, we analyzed current fluctuation behavior and inter-level separability across three representative devices. Each of the 325 programmed levels was monitored for 10 s. The analysis of current deviation from the target (Fig. 2(d) and Fig. S12, SI) reveals noise distributions with minimal state overlap after denoising, a trend consistently observed across all three devices despite minor variations in noise characteristics. Scatter plots of current deviation metrics (Fig. S13, SI) further illustrate differences in distribution width and noise behavior between devices. Nonetheless, the minimum inter-level spacing (~400 nA) remains significantly larger than the observed current fluctuations at each level (Fig. 2(e) and Fig. S13, SI), ensuring clear separation between adjacent states. The lack of significant overlap confirms the precision and reliability of the multilevel programming scheme. Furthermore, the retention stability of these states was further verified up to 10^3 s across three conductance ranges (Fig. 2(f)), showing stable state maintenance over time. In terms of energy and time consumption, the H3P scheme with denoising process consumes an average of ~116 nJ and requires ~7 ms to achieve a stable conductance state (Fig. S14, SI). These measurements were obtained using a passive device controlled by a B1500A semiconductor analyzer, suggesting that further optimization of the programming scheme could improve both energy efficiency and switching speed. In this context, the H3P scheme primarily serves to establish stable and reproducible conductance levels, rather than being a continuously active operation. For applications such as edge inference, where trained neural networks are downloaded from cloud servers to local devices for real-time recognition or decision-making and only infrequently updated,

the additional energy involved in this scheme is expected to remain moderate.[14]

To explore the applicability of the proposed H3P scheme in SPS memristors for edge-inference computing, we implemented a proof-of-concept temporal convolutional network (TCN) classifier using a 6 × 6 SPS memristor CBA, where multiply-and-accumulate (MAC) operations were executed based on conductance states programmed *via* H3P (Fig. S15, SI). This demonstration illustrates how high-resolution conductance tuning can be applied to a representative edge-inference task. Using accelerometer features from the HAR70+ dataset,[31] the TCN model was trained in software and the six 3 × 3 convolutional kernels were quantized to 8-bit precision. These values were then programmed into the memristor array using the H3P and denoising process. A pre-characterized MAC dataset was generated by measuring column-wise current outputs for all input voltage combinations, which were subsequently retrieved during inference to execute convolution steps, with remaining layers processed in software. The hardware-assisted TCN achieved a classification accuracy of 82.81%, which, although lower than the 90.96% obtained from the fully software implementation (Fig. S25, SI), indicates that SPS-based hardware can reproduce inference results with reasonable accuracy relative to software baselines. This hardware-assisted inference provides an exploratory validation that H3P-tuned multilevel states in SPS memristors can support convolution operations, while highlighting opportunities for further optimization toward closing the performance gap.

Investigation of conductive filament evolution in denoising process

To investigate the mechanism underlying the improved fluctuation reduction in current levels of SPS memristors, we examined the evolution of conductive filaments (CFs) during the denoising process. As SPS memristors operate *via* an ECM mechanism, CFs play a key role in resistive switching. Analysing their evolution under different voltage stimuli provides insights into how denoising influences switching stability.[14,32–34] Conductive atomic force microscopy (C-AFM) was employed for this analysis. To facilitate C-AFM measurements, a customized structure was fabricated to replicate the electrical behaviour of the memristor while ensuring optimal imaging conditions (Fig. S27(a), SI). This structure consists of an Au-coated C-AFM probe tip as the top electrode, an SPS nanosheet as the RS medium, and a Ti layer deposited on a silicon substrate as the bottom electrode. While this configuration is a reversed version of the original device, it maintains identical electrical functionality when the probe tip is grounded, and voltage is applied *via* the Ti bottom layer.

Initially, the selected area of the pristine SPS nanosheet sample was scanned using the read voltage of 0.1 V to check any existing conductive pathways. As shown in Fig. 3(a), the pristine SPS sample area shows no CF, and it serves as the reference to compare after CF formation. The sample area was then scanned with a higher voltage of 3 V to induce CF formation. The subsequent read scan (Fig. 3(b)) reveals the emergence of several small high-current regions, indicating CF formation. After this, a denoising process was mimicked by scanning the same area with sub-threshold positive and negative voltages, replicating the denoising pulses used in the H3P scheme. A follow-up read scan (Fig. 3(c)) showed notable morphological changes: some smaller current regions disappeared while a few more prominent regions became more conductive. These observations suggest that sub-threshold denoising voltages selectively modulate CF morphology, weakening or disrupting unstable filaments.

To further investigate this effect, a more localized analysis was conducted on individual CFs. After forming, the current of a selected CF was monitored for 10 s prior to applying denoising pulses (Fig. 3(d), red line), during which significant current fluctuations were observed. A corresponding C-AFM scan captured the filament structure in this state (Fig. 3(e)). Subsequent application of sub-threshold negative voltage scans led to a gradual stabilization of the current within an acceptable fluctuation range (Fig. 3(d), black line). The corresponding C-AFM image (Fig. 3(f)) revealed a modified filament structure, showing diminished peripheral branches while the core remained intact. These results suggest that weaker or incomplete filaments are preferentially suppressed, thereby reducing noise sources. A similar trend was observed when sub-threshold positive voltage biases were applied to another selected CF. Please note that the selected CF was re-formed to isolate the effect of positive biases. A clear improvement in current stability was observed (Fig. 3(g)), and the corresponding before-and-after C-AFM images (Fig. 3(h) and (i)) shows that a few more prominent regions became more conductive. This again confirmed the selective modulation of unstable CF branches. Together, these results support the hypothesis that paired positive–negative denoising pulses reinforce stable filaments while selectively eliminating transient, noise-prone conductive paths. This selective refinement of the conductive network facilitates more precise conductance tuning and effectively expands the number of distinguishable conductance states within a fixed ON/OFF ratio. The observed behaviour is consistent with previous studies on denoising in ECM-based memristors using HfO_2/Al_2O_3 and HfO_2 systems.[14]

Artificial synaptic plasticity and image recognition simulation using a synaptic plasticity based artificial neural network

In addition to their capability to achieve multiple conductance states, SPS memristors can function as electronic synapses, mimicking key properties of biological synapses, which serve as the fundamental units of brain-inspired computing. Structurally, an SPS memristor closely resembles a biological synapse, where the two electrodes act as the pre- and post-synapses, while the SPS switching layer facilitates Ti ion migration, forming CFs analogous to synaptic connections (Fig. 4(a)). For neuromorphic computing applications, long-term potentiation (LTP) and long-term depression (LTD) are essential synaptic functions required for ANNs.[35,36] These properties were demonstrated in SPS memristors, where positive voltage pulses induced LTP by increasing post-synaptic currents, while negative pulses induced LTD, reducing the current (Fig. 4(b)). Additionally, the dependence of excitatory post-synaptic current (EPSC) on pulse amplitude was observed, with larger positive voltage amplitudes resulting in greater EPSC responses,

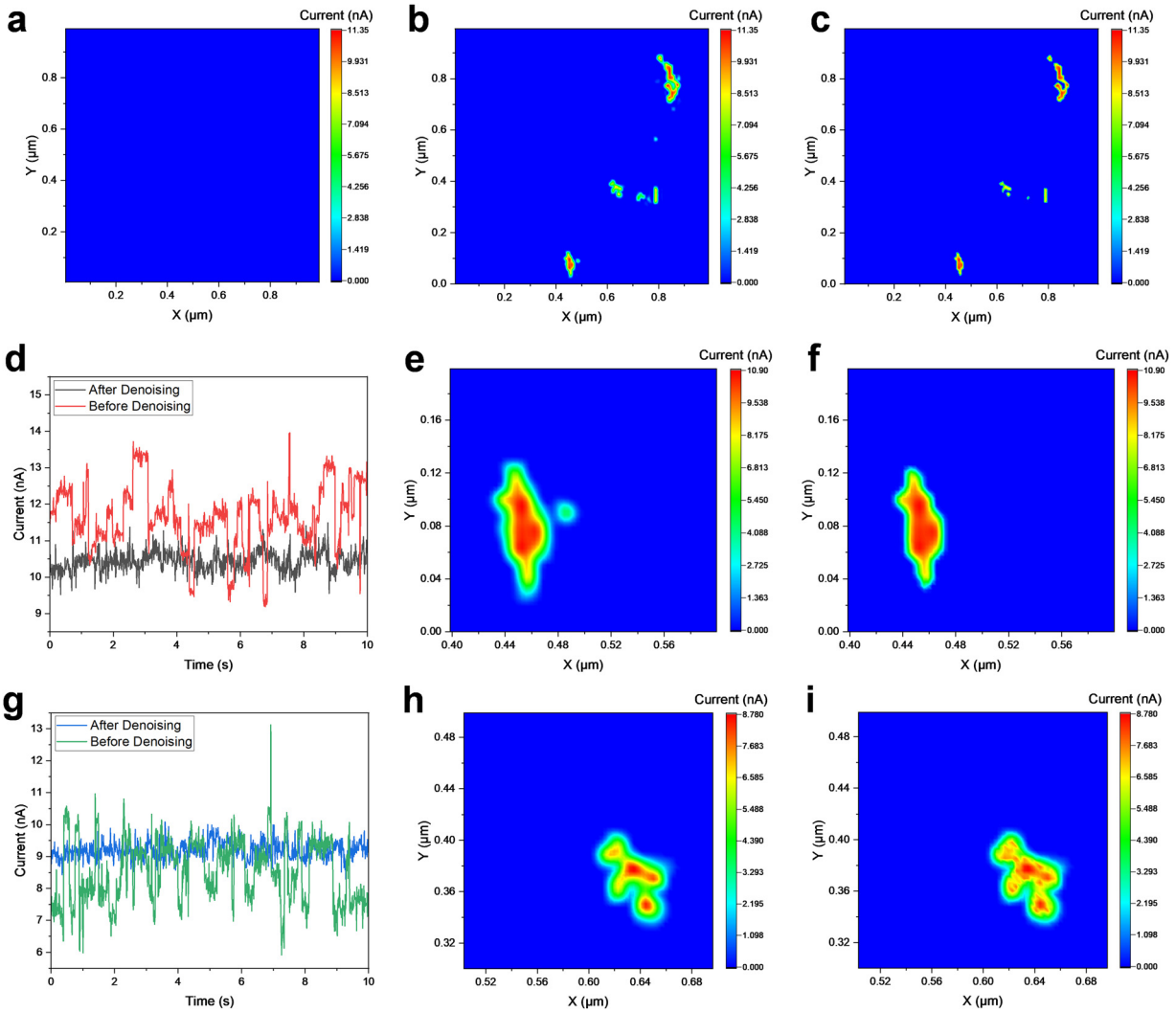

Fig. 3 (a) Current map obtained from C-AFM scanning on the pristine area of the SnP_2S_6 surface. (b) Current map obtained from the same area after applying electrical stress of 3 V. (c) Current map obtained from the same area after the application of sub-threshold positive and negative voltages, following the 3 V stress in (b). (d) Currents measured before and after denoising using a sub-threshold negative voltage, read at a constant voltage of 0.1 V during C-AFM measurements. (e) Current map obtained from C-AFM scanning, corresponding to the before denoising state in (d). (f) Current map corresponding to the after denoising state in (d). (g) Currents measured before and after denoising using a sub-threshold positive voltage, read at a constant voltage of 0.1 V during C-AFM measurements. (h) Current map obtained from C-AFM scanning, corresponding to the before denoising state in (g). (i) Current map corresponding to the after denoising state in (g). All C-AFM scans were acquired using a read voltage of 0.1 V.

demonstrating synaptic amplitude-dependent plasticity (SADP) (Fig. 4(c)). Similarly, inhibitory post-synaptic currents (IPSC) were induced by applying negative pulses of varying amplitudes, where higher-amplitude negative pulses resulted in a lower final post-synaptic current, starting from a nearly identical initial state (Fig. 4(d) and (e)).

Furthermore, the SPS memristors exhibited "learning–forgetting–relearning" behaviour, a characteristic of biological synapses. When voltage pulses of alternating polarity were applied, the post-synaptic current initially increased due to positive pulses and subsequently decreased with negative pulses. However, the current did not return to its original state, indicating memory retention effects. With repeated learning–forgetting–relearning cycles, the post-synaptic current progressively increased, resembling biological memory reinforcement (Fig. 4(f)). By adjusting voltage pulse amplitudes, it was also possible to simulate synaptic and neural dynamics relevant to brain-inspired computing. Distinct LTP and LTD responses were observed under both identical and non-identical pulse amplitude schemes. To assess the C2C variability of the memristor, each scheme was tested over 10 repeated cycles, showing consistent performance with minimal variation (Fig. 4(g) and (h)). To evaluate the linearity of LTP and LTD events, we normalized the measured conductance values using:

$$\frac{G - G_{\min}}{G_{\max} - G_{\min}} \quad (1)$$

where $G_{\max}$ and $G_{\min}$ represent the maximum and minimum conductance values, respectively. The linearity of potentiation (α_p)

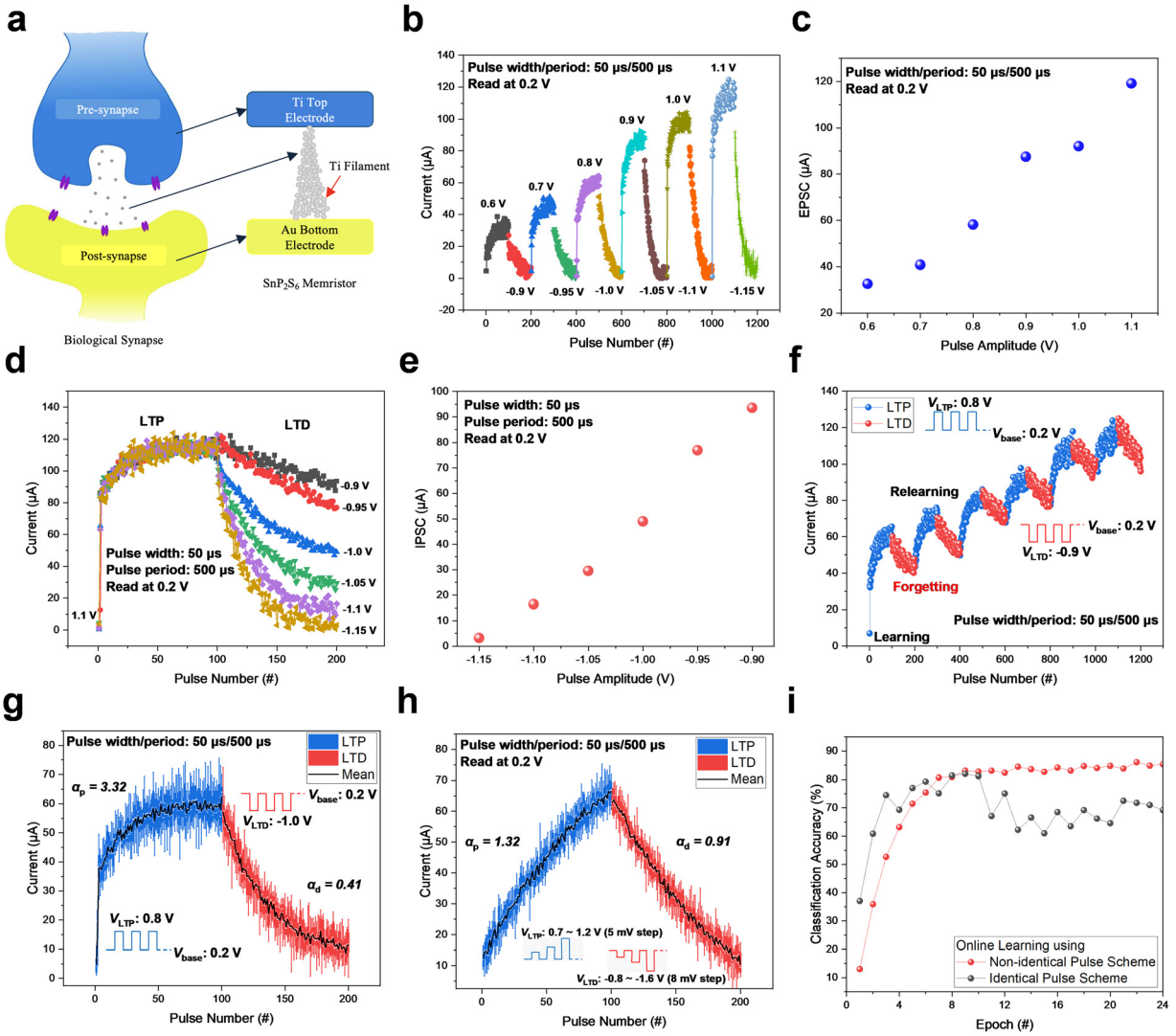

Fig. 4 (a) Schematic illustration of the structural similarity between a biological synapse and a Ti/SnP_2S_6/Au memristor. (b) Tunable LTP and LTD processes by applying pulses with different amplitudes. (c) EPSC of the synaptic memristor, with current values extracted from (b) after 100 positive pulses for each amplitude. (d) Tunable LTD process by applying negative pulses with different amplitudes, while the positive pulse amplitude is fixed at 1.1 V. (e) IPSC of the synaptic memristor, with current values extracted from (d) after 100 negative pulses for each amplitude. (f) Repeated LTP–LTD characteristics, with potentiation and depression pulse amplitudes fixed at 0.8 V and −0.9 V, respectively, resembling learning–forgetting–relearning behaviour. (g) Ten-cycle LTP–LTD characteristics under identical pulses, with potentiation and depression pulse amplitudes fixed at 0.8 V and −1 V, respectively. (h) Ten-cycle LTP–LTD characteristics under non-identical pulses. In both (g) and (h), each box represents the distribution of 10 repeated current measurements acquired at each pulse number. The box edges indicate the IQR, and the whiskers extend to values within 1.5 × IQR. The dot inside each box denotes the mean current, and the black solid line connects these mean values across pulses. α_p and α_d represent the linearity of potentiation and depression, respectively. For all measurements, the pulse width and period were fixed at 50 μs and 500 μs, respectively. (i) Pattern classification accuracy for online learning simulated using MLP + NeuroSim V3.0, based on experimental LTP and LTD characteristics under two distinct pulse schemes: non-identical and identical.

and depression (α_d) was then analysed using the following equations:[37]

$$G = \begin{cases} \left(\left(G_{LRS}^{\alpha} - G_{HRS}^{\alpha}\right) \times w + G_{HRS}^{\alpha}\right)^{\frac{1}{\alpha}} & \text{if } \alpha \neq 0 \\ G_{HRS} \times \left(\frac{G_{LRS}}{G_{HRS}}\right)^{w} & \text{if } \alpha = 0 \end{cases} \quad (2)$$

The results showed that the non-identical pulse scheme exhibited the best linearity, with $\alpha_p = 1.32$ and $\alpha_d = 0.91$. Ideally, a perfectly linear response corresponds to $\alpha = 1$. These findings suggest that conductance modulation *via* non-identical pulse schemes enhances synaptic behaviour. In addition, D2D variability was also assessed by repeating the same process on two other devices randomly selected from the SPS CBA. The results (Fig. S31 and S32, SI) show low variation in weight update and similar linearity responses of the devices for the two respective schemes.

To further evaluate the synaptic properties of SPS memristors, we simulated a fully connected perceptron neural network using MLP + NeuroSim V3.0.[38,39] The measured LTP and LTD

values from both identical and non-identical pulse schemes, including the respective C2C, D2D, and conductance range variations, were incorporated into the simulation to compare their effects on classification accuracy. It is important to note that the α_p and α_d values calculated served as relative evaluation indices for evaluating non-linearity and were not directly implemented in NeuroSim. The simulated neural network comprised 20 × 20 input neurons, 100 hidden neurons, and 10 output neurons, designed for classifying the 10-digit classes of the Modified National Institute of Standards and Technology (MNIST) dataset. The network was trained over 24 epochs, and the resulting classification accuracy was recorded. The results (Fig. 4(i)) indicate that the neural network trained with the non-identical pulse scheme achieved higher accuracy of ~85%, likely due to good linearity in conductance modulation. In contrast, the identical-pulse scheme exhibited faster accuracy improvement during the initial epochs, which can be attributed to its larger effective weight-update step arising from steeper conductance-pulse characteristics. However, this aggressive early learning led to less stable convergence and a lower final accuracy, consistent with an effect widely observed in neural network optimizations, where an excessively large learning rate may accelerate early learning but impede convergence to the optimal solution.[40] While this is the most likely explanation, other factors such as stochastic weight initialization and device-level variation may also play a role. Taken together, these findings highlight the potential of SPS memristors for brain-inspired computing applications, demonstrating effective conductance modulation through pulse parameter tuning.

Building on these promising results, future work may explore integrating SPS memristors into larger CBAs for advanced in-memory computing. As array size increases, factors such as device variability, IR drop, and cross-talk can introduce computational inaccuracies.[8,41] Cross-talk, arising from parasitic currents, capacitive coupling, or voltage sharing, can lead to read/write disturbances, signal attenuation, or erroneous current summation during MAC operations, particularly when many low-resistance cells exist in parallel paths.[42,43] These effects become increasingly significant with higher array density. Addressing these challenges will require wafer-scale SPS growth to minimize variation, along with access mechanisms to suppress sneak currents and ensure cell isolation. Strategies include one-transistor-one-resistor (1T1R) architectures, one-selector-one-resistor (1S1R) configurations, and self-rectifying memristor arrays.[10,44–46] Since SPS devices exhibit abrupt SET transitions and rely on external compliance, selector-free integration is not feasible. While 1T1R or 1S1R integration may be promising, realizing such architectures with SPS memristors will require co-design and fabrication of dedicated access elements, which lie beyond the present scope. Future efforts should explore these directions to unlock full-array integration and broaden the applicability of SPS memristors in neuromorphic and analog computing systems.

Conclusions

In conclusion, SPS memristors demonstrated repeatable bipolar RS behavior with minimal spatial and temporal variations in switching voltages. Through the H3P scheme combined with a denoising process, up to 325 stable conductance states were reliably achieved. C-AFM investigations revealed that carefully designed denoising pulses effectively minimize incomplete filament formation and suppress current fluctuations, thereby enhancing the stability of the conductance states. Beyond their potential for multi-bit memory storage, SPS memristors also demonstrated the ability to emulate synaptic plasticity behaviors, supporting their applicability in brain-inspired computing. Collectively, these findings highlight the potential of SPS memristors to serve as a high-resolution platform for analog memory and neuromorphic computing, with promising relevance for edge-inference applications.

Experimental

Device fabrication

Two-terminal crossbar memristor devices were fabricated on a silicon/silicon dioxide (Si/SiO_2) substrate. The bottom electrode, consisting of a 5 nm Ti adhesion layer and a 20 nm Au layer, was deposited onto the Si/SiO_2 substrate *via* e-beam evaporation. A mechanically exfoliated SPS nanosheet was then transferred onto the bottom electrode. The fabrication was completed by depositing a 30 nm Ti layer and a 20 nm protective Au layer as the top electrode. The top and bottom electrodes were patterned using electron beam lithography (EBL, JBX-6300FS) with poly (methyl methacrylate) (PMMA) as the photoresist and isopropyl alcohol/methyl isobutyl ketone (IPA/MIBK, 1 : 3) as the developer.

Device measurement

All electrical characterizations, including DC measurements and pulse-based measurements, were conducted using a Keysight B1500A semiconductor analyser. During electrical testing, the Ti top electrode was biased, while the Au bottom electrode was grounded. All measurements were performed under ambient conditions at room temperature.

Material characterization

The Raman and PL spectra of exfoliated SPS nanosheets were acquired using a Renishaw Raman microscope, equipped with a 532 nm excitation laser and a 50× objective lens, under ambient conditions. The laser power was limited using a 5% filter. The Si peak at 520 cm^{-1} was used as a reference for calibration. Cross-sectional TEM and EDS were performed using a Talos F200X TEM. Thin lamellae for TEM characterization were prepared using a focused ion beam (FIB, FEI Helios NanoLab). C-AFM scans were conducted using a Park NX20 atomic force microscope.

Statistical analysis

In Fig. 1(e) and (f), the sample size is 100 data points. In Fig. 1(h) and (i), the sample size is 216 data points, from six cycles across 36 devices. For each current level in Fig. 2(f), the sample size of the current deviation distribution is 1001 data points. The overall mean and standard deviation of the current

deviation are −0.02 nA and 33.58 nA, respectively. For Fig. 4(g) and (h), statistical analyses are provided in Tables S2 and S3 (SI).

Simulations

Details of the simulated TCN are shown in Fig. S15 (SI), and the NeuroSim setup parameters are summarized in Table S4 (SI).

Author contributions

T. T. T. T. and J. H. designed the experiments. T. T. T. T. performed the experiments, conducted the device measurement, and wrote the original manuscript. K.-W. A. revised the manuscript and supervised the work. All authors commented the manuscript.

Conflicts of interest

There are no conflicts to declare.

Data availability

The data supporting this article have been included as part of the supplementary information (SI). The accompanying Excel file contains all raw data used to generate the main figures (Fig. 1–4), except for Fig. 1(a)–(c), (g), and 4(a), which rely on schematic or imaging data. Supplementary information is available. See DOI: **https://doi.org/10.1039/d5nh00675a**.

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