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Graphene-CNT Hetero-Structure for Next Generation Interconnects

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1. Abstract:

Carbon nanomaterials, Graphene and Carbon Nanotubes (CNTs), are emerging as potential materials proposed for integration in the future semiconductor technologies, and have been included in the 'International Technological Roadmap for Semiconductors' future plans (ITRS 2012).[1] The main strength of these carbonaceous carbon nanomaterial materials lies in their well-known advantageous electrical characteristics, namely low-resistivity, high current densities ~ 10^9 A/cm^2 , long electron mean-free-paths in order of sub-mm range. ŧ and also their 10 times higher thermal conductivities as compared to copper. and [2] A rather uncommon combination of several beneficial electrical, thermal and physical characteristics has made them a strong contender for the replacement of metals in interconnects for the future Very Large Scale Integration (VLSI) and Ultra Large Scale Integration (ULSI) technologies. However, upto now unexpectedly high contact-resistances at the carbon/metal interfaces has presented a stiff technological challenge, hindering the large-scale adoption of the carbon-technology to replace the metals in interconnects in the semicon industry.

The technological development for the implementation of Graphene and CNTs inside the Through Silicon Via (TSV) Structures for 3D-IC packaging, for Back-End-Of-Line (BEOL) and inter-chip interconnects is a real challenge. Although several reports has mentioned about the

Graphene or CNT based interconnects [3] [4] [5][6] with metals but the main disadvantage is laying at the carbonaceous materials to metal interface. A novel growth and fabrication technique have demonstrated for the heterostructure of the CNT/Graphene materials for replacing horizontal metal lines, and metals in the vertical interconnects. We have developed a process-flow for low-temp (~550^{o}C) growth of the CNTs on top of semi-metallic few-layer Graphene (FLG). In this approach, CNTs replaces the conventional metals in the vertical interconnects, while Graphene is used to replace the traditional horizontal metal-lines on the integrated chips (IC) at back-end level, and at the inter-chip interconnects levels using TSVs The innovative idea is to create a low-resistance CNT/Graphene connection at their mutual interfaces for high-speed signal propagation, which is realized by formation of covalent (sp^2) bonds between carbon atoms in the CNT and FLGshows that $R_{FLG/CNT}$ is about 1/6th of the $R_{Cu/CNT}$, and is about 1/15th of the total via resistance; that will initiate the large-scale adoption of the carbon-technology to replace metals in next generation interconnects.

2. Introduction:

Miniaturization of the electronic and semiconductor device's dimensions and increase of their performance has been well-predicted by the Moore's law for the past few decades or so. There have been concomitant improvements in the device speeds, reduction of power consumption and success at ultra-large scale integration of devices on the chip real-estate, leading in turn to significant cost-reductions. Initially, device packing density on a chip used to be in few-thousands due to the simplicity of the design process, and constraints of the contemporary

fabrication technology. Advancements of the design techniques, and gradual improvements in the fabrication technology enabled for an exponential increase of the device density enabling an ultra-dense scale of integration leading to fabrication of ICs with billions of devices per chip and faster cycles. However, in the recent past, ICs scaling has reached fundamental physical limitations in terms of device size, which has created constraints for the industry's drive for miniaturization. Further, on-chip interconnects have been a source of delay and serious bottleneck to performance improvements of the ICs due to their decreasing cross-sections/dimensions with scaling. In order to deal with these issues, novel and revolutionary approaches are needed in the realms of fabrication, design of device architecture and packaging-technologies, and have been proposed by the association for ITRS, 2012. Since 2007 onwards, the ITRS roadmap has brought forward the concept of vertical interconnects to improve performances attainable through vertical-stacking or TSV interconnects for faster signal propagation, viz. 3D-IC technology.[7]

TSVs are enabling technology for 3D stacking for the future growth of IC industry, as an alternative to node-scaling. TSVs are vertical vias that can be etched in a die or wafer to enable faster, small-path length communication channels between vertically stacked integrated circuits and devices. The TSV technology for three-dimensional (3D) integration of chip ICs, on stacked-die or silicon-packages depending upon multifaceted applications, provides novel ways for dealing with current deviation of the progress trend from the Moore's law and allows the industry to continue with its drive for (*i*) device miniaturization, (*ii*) system-level scaling, (*iii*) reduction of local/global delays, (*iv*) to do away with the need for large input/output drivers and, (*v*) allows for fabrication of low-power, low-loss, faster clock-cycles, higher-bandwidth interconnects. The

future objectives of the industry are to build know-how and develop process technologies for seamless, functional incorporation of heterogeneous structures; namely integration of diverse and disparate integrated circuits such as digital, analog, RF circuits with nano- and/or micro-electromechanical systems (N/M-EMS) onto one single system for applications in system-on-chip (SOP) and system-in-package (SIP). Eventually, TSV interconnects are going to contribute in a big way towards technological feasibility and realization of the mentioned goals.

TSV's are conventionally filled with suitable low-resistance, thermally-conductive, high-reliability materials/metals. The downscaling of the TSV dimensions, i.e. fabrication of high-aspect ratio TSVs, is an important goal. The scaling of TSV-interconnects would allow facile connectivity between the blocks of lower-level of BEOL metal lines in vertical stacked dies, and thereby significantly enhance the packaging density. Scaling of TSV interconnects leads to an inevitable exponential rise in the resistance of the metals used for via-filling, which is highly undesirable. A proper choice of via-filling materials is therefore quite important. Upto now, conventional filler materials, such as copper (Cu), tungsten (W), poly-silicon, gold (Au) and conductive polymer pastes, have been widely utilized for several decades. However, each of these materials has it's particular drawbacks or short-comings limiting their suitability for applications at the local and global interconnects levels,[8] with copper being the most commonly used material currently.

The desirable properties of more suitable via filling materials are high-current carrying capability, lower thermo-mechanical or thermo-electric stress effects during operation, void-free filling, and good thermal cycling performance. High electrical conductivity, a well-established

electrochemical deposition (ECD) process, and good thermal characteristics make Cu a favorable choice as a filler material for large-dimension vias. In contrast, limitations in deposition of the seed-layer by physical vapor deposition (PVD) process, and in via-filling by the electro-chemical deposition technique (ECD), occurrence of catastrophic defects caused by electro-migration at high current-densities, increasing grain-boundary resistivity caused by the combination of increased scattering, presence of a highly diffusive barrier layer and creation of voids under physical-scaling has eventually led to a realization that copper is a difficult choice for filling of high aspect-ratio vias.[9] Similarly, W is best suited to fill small vias with high-aspect ratios only at temperatures as low as 200°C, and cannot be used for larger vias; it also has a lower conductivity than Cu does. Poly-silicon, Au, and other materials have similar and other/additional issues that make them unsuitable as interconnect filler-materials in this aspect.

Inevitably, active research and development work are being pursued in academia and industry for creating or developing appropriate filler materials for application in low-dimension and high aspect-ratio TSVs based inter-chip interconnects, that would offer desirable physical, chemical, mechanical, thermal and electrical properties. On this front, multi walled-CNTs bundles seem to be highly interesting material of choice that promises a solution to the industry's efforts for overcoming traditional bottlenecks associated with TSV interconnects. As an alternative material to replace the traditional TSV-filling materials, main advantages of CNTs in interconnects are (*i*) high current densities of 10^9 A/cm^2 for single CNT (*ii*) Low grain boundary, i.e. low internal scattering resistance (*iii*) high thermal conductivity of CNTs (1750-5800 W·mK^{-1}) which exceeds that of copper (385 WmK^{-1}) by a factor of 15 and is therefore ideal for dissipating heat from

active devices, (*iv*) low-coefficient of thermal expansion; CTE of CNT ($\pm 0.4 \times 10^{-6}$/K) as compared to the Cu (17.5×10^{-6}/^{o}C), or to Si substrate (2.5×10^{-6}/^{o}C) provides the promise of generating one of the lowest thermo-mechanical stress in the TSV structures.[10] Thus, there is a strong motivation for the researchers to implement CNT technology into on-chip interconnects (BEOL), and in inter-chip interconnects (TSV). With the trend for continuous shrinking of the feature-sizes and contact dimensions, there exists favorable opportunities and challenges for the implementation of the CNTs in low-dimensional structures. As we know the resistivity of the copper based metal lines increases significantly due to scattering of interconnect dimensions. Thus the incorporation of CNTs in vertical interconnect as alternate filler material can't solve the issues existing at the interface. In order to reduce the high barrier resistance, Carbon based heterostructure has been introduced leading to relaxation in stringent demand in existing technology. Moreover, the minimum density at which the CNT contact meets the resistance of the Cu contact decreases when the contact dimensions shrink. This is because the resistivity for Cu increases significantly for confined dimensions and high aspect ratio vias.[11] For comparison, Fig. 1 shows the density of CNT shells for one MWCNT with the same diameter as the contact hole.

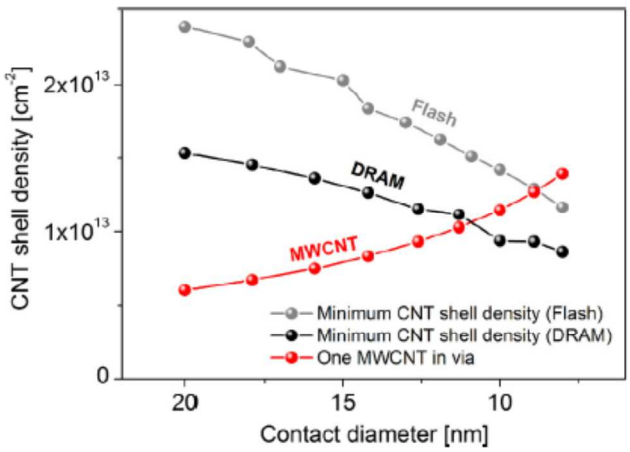

Figure 1:CNT shell density as a function of the contact diameter for DRAM and Flash contacts. Minimum CNT shell densities obtained for DRAM and Flash technology using specifications in the ITRS roadmap; adapted from Ref. [9].

H. Kawarada *et*. *al*. have shown[12,13] that the CNT bundles can be successfully grown on top of metal-lines inside SiO_2 vias (BEOL) of diameter as low as ~ 2μm, with CNT growth density of 1.6×10^{11} cm^{-2} at 390^{o}C. They have demonstrated that after chemical mechanical polishing (CMP) the resistance of CNT bundle falls from 32 Ω to 0.9 Ω, which is possibly due to contribution to the overall bundle conductivity by all of the interior walls of MWCNT. Furthermore, a many-fold enhancement of the as-grown CNT bundle density, to an order of magnitude higher value (2.5×10^{12} cm^{-2}), has also been demonstrated via wet-chemical densification process.[14] The reported densification had characteristic advantages, such as reduction of the via resistance down to 22 Ω for ~ 1000 CNTs embedded in vertical interconnects of 250 nm via-diameter, and aspect-ratio of 4. However, the as-measured CNT density, which is manually determined by visual inspection under SEM, is not so accurate. In another novel approach, an IMEC group,[15] has demonstrated that one of the alternate possibilities is to grow the CNT bundles on top of the metal-lines followed by CMP, and metal-electroplating through metal-ion-reduction at highly-

reactive dangling CNT tips. By this process, metallic particles are formed only on those CNTs that are in electrical contact with the bottom metal-lines. As compared to the previous approach, this is a relatively more accurate method to determine the density of truly conductive CNT inside any particular via. The same group also demonstrated a far simpler way to extract the single CNT bundle resistivity,[16] which was measured to be 2.7×10^{-3} Ω cm for SiO_2 via of 300 nm diameter and 530 nm depth. In a later report, it has demonstrated the transfer and replication of this technique to 150 nm diameter interconnects,[17] which is advantageous in being compatible with the single Cu damascene module at 130 nm technology node. On the other hand, for inter-chip interconnects technology through the implementation of TSVs, the preferable diameters, and the length comes in the range of 30-50 μm and 85-200 μm, respectively.[18,19] The resistance of the CNT-bundle in the TSV vias depends directly on the CNTs length; for instance, as the length increases from 86 μm to 139 μm, the resistance shoots-up from 0.21 kΩ to 0.34 kΩ, respectively.

The CNT growth and via-filling in TSV technology can be done by two distinct process flows, viz., either growth of CNT bundles directly in TSV-via in a bottom-up approach, or otherwise to transfer CNT bundles, post-growth, to the TSV vias.[20-23] It has been observed that bottom-up approach of CNT growth requires high growth temperatures, approximately 700^{o}C for longer TSV channels.[18] On the other hand, post-growth transfer process is limited to large diameter TSVs only.[20] For sub-5 μm diameter TSV structures, it is experimentally difficult to transfer the CNT bundles effectively due to unavoidable misalignment factor of ~ 2μm. Thus for small-diameter, high aspect-ratio TSV structures the only feasible way to achieve CNT filling, is to follow the bottom-up growth process.[18]

Though, several groups have reported successful growth of the CNT on top of metal-lines there are issues regarding high-contact resistances at the Metal/CNT interfaces, which need to be solved for successful commercialization of the technology for CNT integration in the interconnects by the semiconductor industry. To the best of our knowledge, there are no well-known standard processes for the estimation of the CNT to metal contact resistance values. Different groups have presented their results for determination for the CNT/Metal resistance values using approximations for various measurement techniques and assumptions, which are essentially non-equivalent approaches. To add to the complexity, samples have been fabricated using varying and disparate, non-standardized growth techniques (variable catalysts/metals/ growth-temperature/isolation-layers), and different conditions, which makes it very difficult for straightforward comparison of these reported values in the literature. Further, ITRS roadmap for the integration of the CNTs in TSVs mentions about an assumption of the contact resistance, R_C to be about 10% of the single-CNT resistance, R_{CNT}, in a via.[24] However, there are no known reports in the literature about exact determination of the individual resistance values, R_C and R_{CNT}, as defined by the ITRS guidelines. CNT-via resistance values vary over wide range from 25 Ω [25] to upto 200 kΩ, [26] while the resistivity values are reported in the range of 0.8-12 mΩ.cm for the CNT-Bundles grown on top of metal-lines (Au, Co-Silicide) interfaces. For single CNT to metal (TiN) contact resistance, the values reported are in the range of ~2.8 kΩ to 4.8 kΩ. Recently, Vanpaemel et.*al*.have reported different resistance values for the CNT grown on top of TiN. [11]In the absence of Al_2O_3 isolation layer between the CNTs, the four-probe determined resistance of single-CNT is 51 kΩs, whereas with the presence of isolation layer the

single-CNT values ranges from 4.9 - 6.3 KΩs. On the other hand, Chiodarelli *et. al.* [15] report CNT bundle resistance values, for CNTs grown on top of TiN through oxide-vias, to be between 100-140 kΩs, i.e. about three-order of magnitude higher than other reports. However, the values quoted do not separate the different contributions from the R_C and R_{CNT}. Recent work on tomography based 3D measurement of resistance by Schulze using scanning spreading resistance microscopy (SSRM), ultra-sharp full-diamond AFM probes measured the bottom contact resistance of a CNT bundle with high-precision.[27] They reported the R_C to vary from ~146-541 kΩs per CNT (for the case of single-shell current conduction). Whereas, in an earlier work on a similar sample, Chiodaralli *et. al.* had estimated the R_C from measurements done on about 576 CNT-integrated Vias connected multiply in-parallel under each metal-pad to be around ~1.16 kΩs for a bundle comprising 100 CNTs.[16]

In the present study, we report about an experimental way to determine and separate the contributions of the CNT bundle resistance (R_{CNT}) and the contact resistance ($R_{CNT/Cu}$) from the total via resistance using state-of-the-art electrical characterization techniques with high-precession, four-probe/two-probe (4PP/2PP) electrical nano-probing tools integrated with a SEM system. The total CNT-bundle resistance is found to be ~1.2 kΩ, amounting to a resistivity of ~66.2 mΩ.cm per bundle. Further, taking into account the total number of CNTs in contact with the probe-tip (~ 75 CNTs), the total via resistance/CNT is about ~136 KΩs, out of which the individual CNT resistance is ~90 kΩ; that is, ~66% contribution to the via-resistance is by the single-CNT. Whereas, the $R_{CNT/Probe}$ resistance is ~ 11.3 KΩs, with the remaining contribution to the total via resistance is coming from CNT/Metal-line contact resistance, R_C. Implicitly, this

means that the CNT-to-metal contact resistance, $R_{C,}$ is in our case is ~ 35 kΩ for a single CNT/Cu contact, that is ~39% of the single-CNT resistance, that is four times higher than the ITRS guidelines,[26] and not in agreement with the ITRS roadmap. Thus, there is an urgent need of a technological innovation to drastically reduce the resistance between vertical-CNT pillar and horizontal conductive paths in both local and global interconnects.

Hereby, we propose a novel technical solution to tackle and deal with high contact-resistance issues in interconnects by integration of the carbonaceous nanomaterials to replace metals in both vertical and horizontal interconnects. Below, we present explicit details and radical ideas for conceptual implementation and experimental realization of Graphene and CNT hetero-structures to provide low-resistivity, high thermal conductance, low-stress advantages for metal-free interconnects in the 3D-IC stacking technology. Please refer to the sections below for further details.

3. Experimental Details:

First the graphene has grown in tubular CVD furnace at 900˚C on 25 μm thick copper foil. The graphene containing copper foil is spin coated with Poly-methyl methacrylate (PMMA) to hold the free standing graphene during chemical etching of copper foil against iron nitrate solution. The film is rinsed thoroughly under deionized water to get rid of metal contaminants. This free standing graphene film is transferred by scooping technique on 6”-wafer and thoroughly has been dried under vacuum with mild heating keeping the substrate with 30 degree tilt that allows removal of trapped water sandwiched between graphene and silicon wafer. This process allows the strong adhesion of graphene film on silicon wafer with Van der Wall force. The wafer is then

rinsed with acetone to remove PMMA layer from the top of adhere graphene film. The 500nm SiO_2 is sputtered at room temperature onto the graphitic film followed by pattering by photolithographic technique using SHIPLEY MICROPOSIT S1813 as photo-resist (PR) under 365nm I-line. The oxide vias are created by the chemical etching of sputtered oxide through the PR pattern by buffered oxide etchant (NH_4F/HF) to reach to the graphene film at the bottom layer. A thin layer of iron of 1-2 nm is deposited on top of the substrate followed by lift-off to remove the remaining photoresist. Thus the oxide separated Fe islands are formed on Graphene film that leads to vertical CNT growth in thermal CVD at 550°C that results to the growth of seamless graphene-CNT heterostructure. Electrical measurement is carried out under 4-probe nano-manipulator under FESEM using Keithley power sourse.

4. Results and Discussion:

A schematic illustration for the integration of the FLG/CNT heterostructure in TSVs and in BEOL-via is shown in the Fig. 2, where vertical vias are filled with the VACNTs, while traditional horizontal metal-lines are replaced with FLG layer in 3DIC stacking in local-to-global spanning chip architecture.

Generally, small-vias in the BEOL structures provide signal-transfer connectivity between the individual logic devices on the same plane-level. The main signal trace-lines are connected to the TSV vias, which allows for data transfer from one stack/level to the devices on the other stack at the next level for chip-to-chip interconnectivity in a three-dimensional framework.

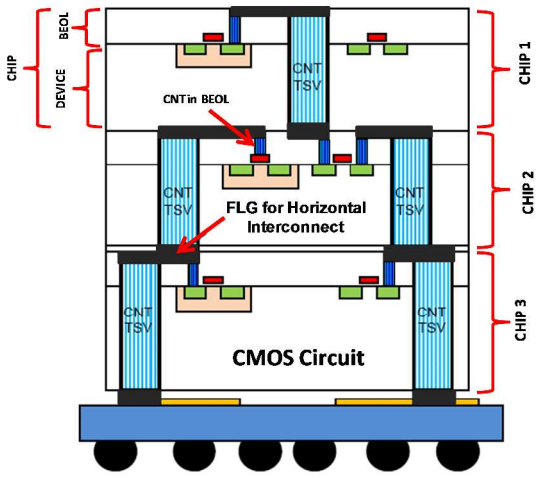

Figure 2: A schematic for the implementation of the FLG and VA-MWCNTs in a 3D-IC structure in CMOS circuits. The arrows marks the position of one of the TSV in the middle chip where-in the vertically aligned CNT (VACNT) growth has taken place which is connected to a graphene-line on horizontal plane. The VACNTs are also present in the vertical vias at the BEOL structure.

Fig. 3 shows SEM image of the VACNT bundles growing through the TSV structures of about 4 µm diameter on top of the Cu-metal lines. CNT-bundles are electrically isolated from the bulk silicon by ~500 nm thick conformal coating of the SiO_2 layer. Fig. 3(*a*) shows a cross-sectional perspective of the CNT bundles growing through a via from the bottom metal line, while Fig. 3(*b*) depicts the top-view of the TSV holes at an angle of about 30 degrees to the horizontal plane; giving a visual confirmation of bottom-up growth of the CNT bundles inside TSV-via.

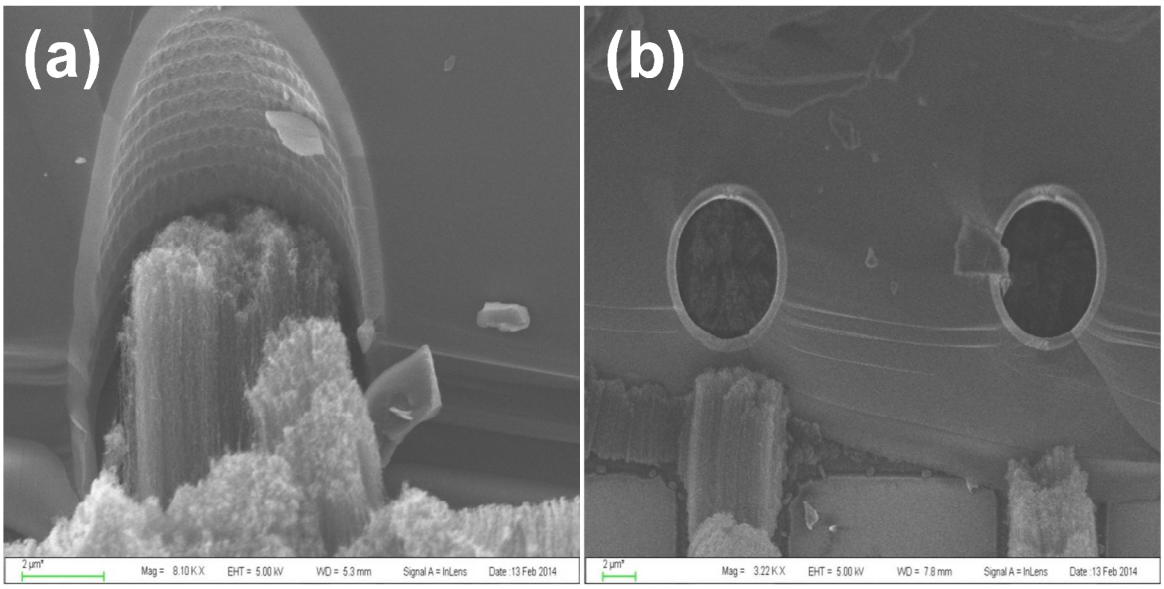

Figure 3: SEM image of the cross-section of the VACNT bundles growing through the TSV via (*a*) cross-sectional, and (*b*) top view of the CNT-TSV structures.

The process-flow for the integration of the Graphene/VACNT starts on top of the bare Si-Substrate, shown in Fig 4. A thermal oxide layer of ~500 nm thickness is first grown on top of the bare silicon wafer. A previously, separately grown, free-standing FLG film is transferred using a standard wet-chemical process for transfer on top of the oxide-coated Si-wafer.[30] A thin layer of Ti (~1 nm) is deposited on the graphene film for protection against oxidation during the following oxide-deposition. Then, plasma-enhanced tetra-ethyl-ortho-silicate (PETEOS) oxide is deposited (1 μm) on top of graphene. Positive photo-resist (PR), S1813, is spin-coated to standard thickness of 1.25 μm followed by pre-baking at 110 ºC for 4 minutes in a nitrogen flow chamber. Subsequently, the process continues with lithographic patterning (UV @ 365 nm, exposure intensity for 6s), development (65 seconds) using TMAH developer (**Step: A; Fig. 4**), and hard-baking for about 20 minutes at 110 ºC in a sequential order. This patterned PR mask

helps to selective area oxide etching (**Step: B; Fig. 4**) down to graphene film in buffered oxide etchant (BOE:- NH_4OH:HF) solution for about 7 minutes; the thin Ti layer also gets etched away in this step. In order to deposit a catalyst layer for initiating the CNT growth, a 1 nm thin Fe layer is sputtered on this sample followed by the PR lift-off in acetone solution. Thus the catalyst islands are formed inside the

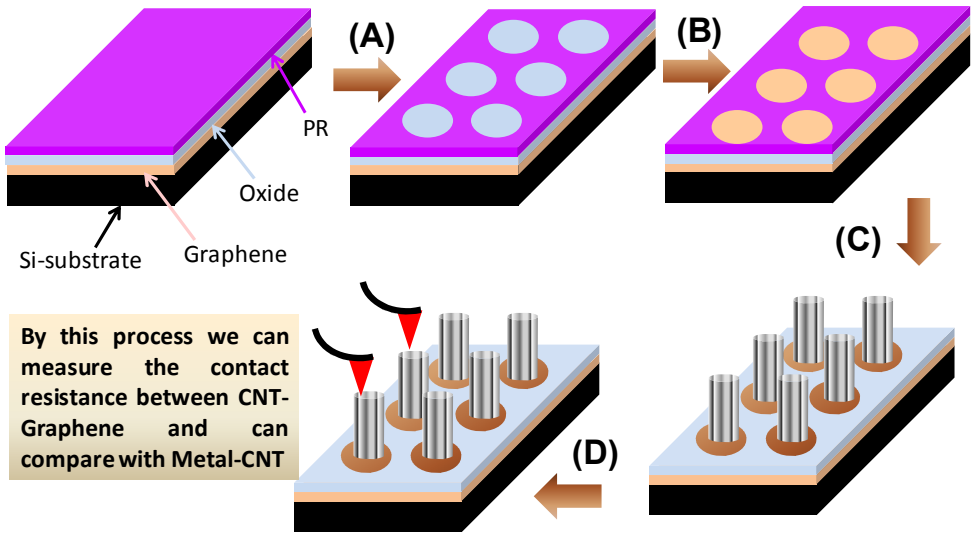

Figure 4: A graphic illustration of the process-flow steps that are involved in the growth of the VACNT on top of a patterned FLG layer using Fe catalyst, followed by nanoprobe characterization of contacts.

PETEOS oxide vias patterned on top of graphene film (**Step: C; Fig. 4**), signified by amber colored circles. This is followed by growth of the VACNTs in the Aixtron-Black-Magic thermal CVD system at 550ºC temperature in 150:50 sccm Acetylene: Hydrogen flow. The as-grown CNT bundles are marked by the vertical columns. The earlier mentioned methods of 4PP/2PP were used for electrical characterization of the FLG/CNT contacts at their interfaces (**Step: D; Fig. 4**). The details of the steps taken for the implementation of the process-flow are further described below.

In Fig. 5, a FLG layer is grown on a copper-foil which is placed inside a glass-furnace at 1000 ºC temperature for upto 5 minutes of growth under the laminar flow of methane (CH_4) at the rate of 100 sccm diluted with 10% of hydrogen gas (Fig. 5A). To separate the graphene film from the copper foil, the PMMA coated FLG is dipped in ferric-nitrate solution ($Fe(NO_3)_3$ overnight (following the standard process, reported widely in the literature),[30] and is shown in Fig. 5(B,C). The free-standing FLG/PMMA film of 10 cm x 8 cm area is then transferred to the oxide-coated wafer, and optically characterized by Raman spectroscopy. The corresponding G/2D ratio for our

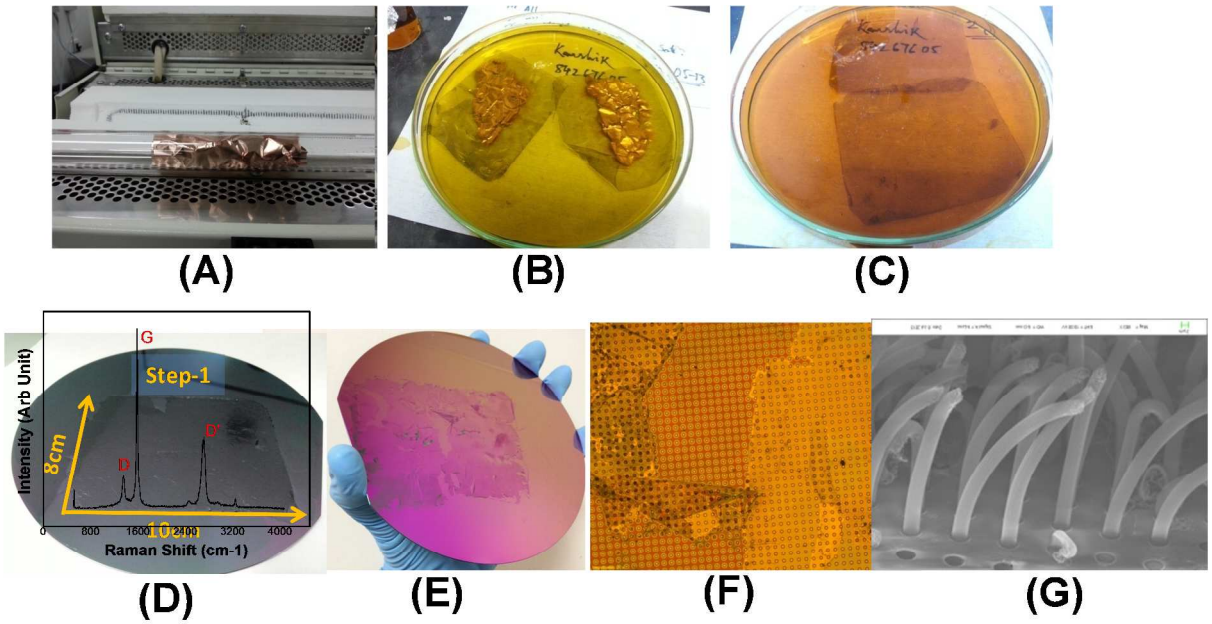

Figure 5: The images in this figure depict the steps involved in growth of the FLG, it's transfer to the silicon wafer, characterization, followed by the patterning and thermal-CVD growth of the VACNTS bundles through the oxide vias.

G/2D ratio for our as-transferred FLG is ~2.34 which provides confirmation that the FLG consists of 4-5 layers of graphitic layers (Fig. 5D).[31] Due to the crumpling of the copper foil, the as-grown FLG film has fracture-lines and sometimes leads to scrolled graphene layer that folds-

up along the edges (Fig. 5E,F). The transferred FLG film after deposition of the PETEOS oxide layer and patterning is shown in Fig. 5F, which is then processed for the growth of VACNTs through the oxide (PETEOS) via, and is shown in the Fig. 5G post-growth. However, from these images it is hard to prove and verify that a seamless contact exists at the FLG/VACNT interfaces, and thus is a need for further analytical structural characterization. For the low-resistance, high electrical conductivity contacts, it is essential that the carbon atoms in the FLG layer are covalently (sp^2 hybridized) bonded to the carbon atoms of the Vertically aligned CNT (VACNTs).[32] Thus, we performed cross-sectional HR-TEM imaging together with the elemental mapping at the interfaces of the carbon-carbon heterostructure.

The cross-sectional view of the focused-ion-beam (FIB) cut lamella of the FLG/CNT heterostructure in the vicinity of the interface is shown in perspective as inset to the Fig. 6(*a*), while a detailed structure of the small selected area marked by the red colored box is shown in the zoomed-in view, where one can notice discretely identifiable vertical growth of the CNT on top of FLG layer. TEM analysis provides further precise evidence that the growth of the CNT is rooted in the FLG substratum/supporting-layer, in Fig. 6 (*b,c*). However, high-energy ion beam used for the preparation of the lamella damages the graphitic fringes of both the CNT and FLG, while the deposition of the tungsten pre ion-bombardment in the course of TEM sample preparation makes it hard to image the sharp graphitic fringes. This inability to decisively perform high-quality TEM imaging, meant that we have to find another way to gain conclusive

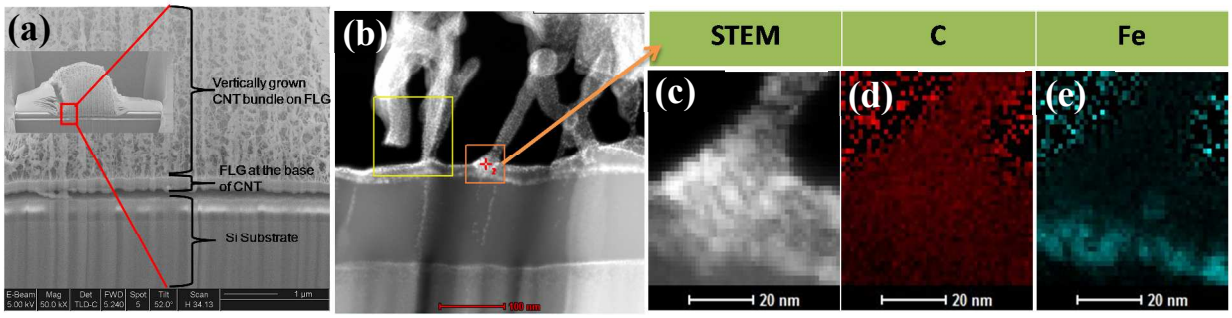

Figure 6: (a-c) Cross-sectional views of the TEM Lamella and images from TEM and STEM characterization in perspective, showing distinctly the interface at the border between the VACNT and the horizontal FLG on top of Si-substrate. On the right, images (d,e) show the spatial distribution of the carbon and iron atoms with the respect to the position of the interface.

evidence of existence of a seamless *C-C* heterostructure at the interface. Thus, we performed EDX based spatially resolved elemental mapping for deeper insights. Some results of the elemental mapping are shown in Fig. 6(*d*), wherein the spatial distribution of the localized carbon is resolved and indicates the creation of covalent bonds between FLG and CNT at their interface. Whereas, the imaged spatial distribution of the Fe atoms at the interface implies that some of the iron atoms are getting intercalated in between the graphitic layers.[33-35] The presence of the iron atoms near the interface is known to cause an enhancement of the electrical conductivity of the heterostructure, and thus could be a possible reason of low-resistivity values that are obtained for our heterostructure.

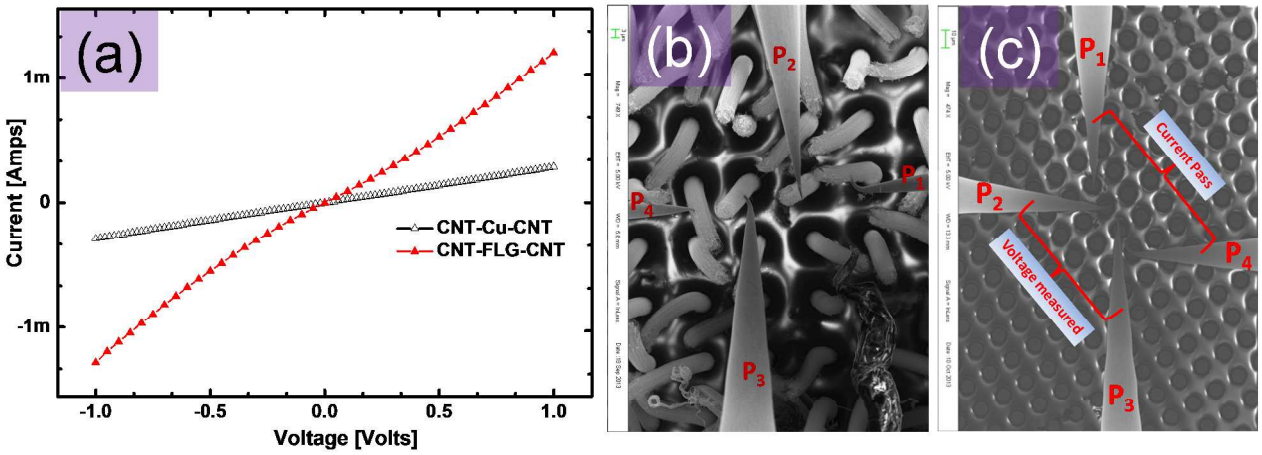

Figure 7: (a) Comparative *I-V* characteristics of the FLG/CNT and Cu/CNT heterostructure, where $R_{C\ (FLG/CNT)}$ (5.8 kΩ) of a single CNT is about ~6x smaller than the $R_{C\ (Cu/CNT)}$ (35.15 kΩ) and **(b-c)** SEM images from the corresponding studies using nanoprobe system from Zyvex in the 4PP configuration: red and black triangles symbols represent the measured data points, and the corresponding lines connecting the respective data points are there to guide the eye.

To get detailed quantitative insights into the electrical characteristics of our FLG/CNT heterostructure, so as to be able to compare their performance with that of the Cu/CNT heterostructure, we did several 4PP measurements. In this experiment we first keep our sample on SEM sample holder where we adjusted the 4-point probes from Zyvex at the near vicinity of the sample. Under the FESEM all the probes are aligned in same height via XY and perpendicular (Z) displacement of all probes stages, Followed by the sample stage is bring upward to the same plane along with the probes tips. Then the all four tungsten tips are landed to the pre-decided CNT bundles for *I-V* characteristics. Here the probes like; P_1 and P_4 is used for current supply and P_2 and P_3 are used for voltage measurement for both Cu-CNT and Graphene-CNT hetero architecture. Fig. 7(a) shows the *I-V* curves that are obtained, and a distinctly noticeable improvement in the current-conduction of the FLG/CNT is seen and marked by the

red-triangles. At an applied bias of +/-1 V, the current flow through the CNT-FLG-CNT pathways was enhanced by ~4.5x times in comparison to that in the CNT/Cu/CNT structures, in a similar probing configuration. Detailed calculations from our 4PP measurements, showed that the FLG/CNT contact resistance, $R_{C\ (FLG/CNT)}$ (5.8 kΩ) of a single CNT is about ~6x smaller than the $R_{C\ (Cu/CNT)}$ (35.15 kΩ). This is a confirmation of our initial hypothesis that the seamless integration of horizontal and vertical carbon-carbon interconnects have a strong potential for the replacement of the metal from the silicon industry, giving an added push to the feasibility of integration of carbon nanomaterials in the semiconductors.

5. Conclusion:

In summary, the 3D integration and chip-stacking are going to play in the next generation leading technology. Carbon based nano-materials offer a low-cost, low-power, high thermal-conductivity and serve design platform for carbon-based interconnects which are critical for the future of reliable, high-speed, high-performance 3D-interconnects. In that direction, we have demonstrated the technical feasibility of integrating the graphene and CNTs heterostructure in 3D-IC interconnect at CMOS compatible process temperatures. This design purports to be metal-free complete carbon based technology and possibly allows for total replacement of the metal based interconnects in CMOS process. Integration of the graphene layer provides high-mobility, low-resistivity charge transport, which makes it feasible for application in future high-speed devices. This Low-resistive barrier interface of vertical and horizontal interconnects is due to seamless covalent sp^2 bonding amongst *C*-*C* atoms of Graphene-CNT network. As a results, our measurements shows that $R_{FLG/CNT}$ is about $1/6^{th}$ of the $R_{Cu/CNT}$, and is about $1/15^{th}$ of the total via

resistance. Approximately 15 times higher thermal conductivity of the carbonaceous materials compared to copper, provides excellent pathways for the effective heat-transfer from hotspots to the heat-sinks in a multi-chip stacked configurations. The integration of inexpensive graphene-CNT heterostructure in high-aspect ratio TSVs would lead to manifold benefits to the industry, and the forwarded idea is both commercially viable and practically implementable for mass volume production.

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References:

[1] http://www.itrs.net/Links/2012Winter/1205%20Presentation/Interconnect_12052012.pdf

[2] N. Chiodarelli, K. Kellens, D. J. Cott et. al., "Integration of vertical carbon nanotube bundles for interconnects" *ECS Transactions*, 19(24) pp. 11–24, 2009.

[3] A. Srivastava; Y. Xu and A. K. Sharma, "Carbon nanotubes for next generation very large scale integration interconnects" *J. Nanophotonics;* 2010, 4, 041690, p.1-20.

[4] K. M. Mohsin, A. Srivastava, A. K. Sharma and C. Mayberry, "A Thermal Model for Carbon Nanotube Interconnects", *Nanomaterials,* 2013, 3, p. 229-241.

[5] W. Lee; H. Jang; B. Jang; J.H. Kim and J.H. Ahn. "Stretchable Si Logic Devices with Graphene Interconnects" Small 11 (47),6272–6277, 2015.

[6] E. Jabari and E. Toyserkani. "Micro-scale aerosol-jet printing of graphene interconnects" Carbon 91, 321–329, 2015.

[7] http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_Interconnect.pdf

[8] Leduc, P.; Assous, M. ; Di Cioccio, L. ; Zussy, M. ; et.al., "First integration of Cu TSV using die-to-wafer direct bonding and planarization" *3D System Integration, IEEE International Conference on 3DIC; 2009; pp.1-5.*

[9] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt. "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller" *J. Appl. Phys*., 2005, 97(2), p. 023706.

[10] A.D. Trigg, L.H. Yu, C.K. Cheng, R. Kumar, D.L. Kwong, T. Ueda, et al. "Three Dimensional Stress Mapping of Silicon Surrounded by Copper Filled through Silicon Vias Using Polychromator-Based Multi-Wavelength Micro Raman Spectroscopy" *Applied Physics Express*; 2010; 3; 086601.

[11] J. Vanpaemel, M. Sugiura, Y. Barbarin,*et*. *al*. "Growth and integration challenges for carbon nanotube interconnects" *Microelectronic Engineering*, *2014, 120*, *188-193*

[12] H. Kawarada *et. al..Applied Physics Lett*; 2007; 91; 263101

[13] H. Kawarada *et. al..IEEE conference* 2008; P-237

[14] John Robertson*et. al..IEEE Microwave Magazine* Dec 2011**;** p-42

[15] Nicolo' Chiodarelli*et. al..Journal of The Electrochemical Society*; 2010; 157; K211-K217

[16] Nicolo' Chiodarelli*et. al..Nanotechnology*2011;22; 085302

[17] Nicolo' Chiodarelli*et. al..Interconnect Technology Conference and 2011 Materials for Advanced Metallization (IITC/MAM),* 2011; PP 1-3

[18] Jianmin Miao et al. *Applied Physics Lett*; 2007; 91; 042108

[19] Johan Liu *et. al.. Nanotechnology*; 2009; 20; 485203

[20] Johan Liu *et. al..IEEE Electron Device Lett*, March2012**;** Vol. 33; NO. 3

[21] Johan Liu *et. al.. ECS Trans.*2012, Vol 44, Issue 1, pp 683-692.

[22] Johan Liu *et. al..Carbon*; 2010; 48; 3795

[23] Johan Liu *et. al..Adv. Mater.* 2010; 22; 5039

[24] ITRS Interconnect, 2011 Ed., <www.itrs.net>.

[25]T. Wang, Johan Liu, *et. al*.; *Small* 2011, 7(16) 2313–2317

[26] C. Zhang, F. Yan, *et. al*.; *J. Appl. Phys*. 2012, 111, 064310

[27] A. Schulze *et. al.*; *Nanotechnology* 2012, 23, 305707

[28] J. Robertson, G. Zhong,*et. al*.;*Microelectronic Engineering* 2013, 107, 210–218

[29] M. Nihei, A. Kawabata, *et. al*.; "CNT/graphene technologies for future carbon-based interconnects" *Solid-State and Integrated Circuit Technology (ICSICT), IEEE 11th International,* 2012, pp. 1-4

[30]A. Pirkle, J. Chan, A. Venugopal, *et. al*.; *Applied Physics Lett* 2011, 99, 122108

[31] Z. H. Ni, H. M. Wang, *et. al*.; *Nano Lett* 2007, 7(9), 2758-2763

[32] Y. Zhu, L. Li, *et. al*.; *Nature Communications* 2012, 3, 1225

[33] M. Lukas, V. Meded, A. Vijayaraghavan, *et. al*.; *Nature Communications* 2013, 4, 1379

[34] N. Kim, K. S. Kim, *et. al*.; *Nano Lett* 2011, 11, 860–865

[35] S Tongay, K Berke, *et. al*.; *Nanotechnology*, 2011, 22, 425701

Graphene-CNT Hetero-Structure for Next Generation Interconnects

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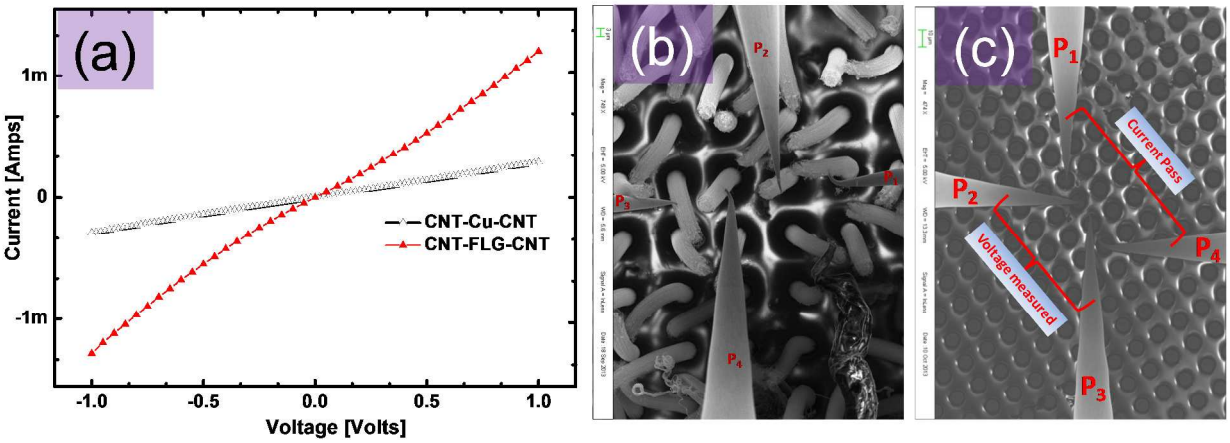

A novel growth and fabrication technique have demonstrated for the heterostructure of the CNT/Graphene materials for replacing horizontal metal lines, and metals in the vertical interconnects. In this approach, CNT replaces the conventional metals in the vertical interconnects, while Graphene is used to replace the traditional horizontal metal-lines on the integrated chips (IC) at back-end level, and at the inter-chip interconnects levels using TSV vias. The innovative idea is to create a low-resistance CNT/Graphene connection at their mutual interfaces for high-speed signal propagation, which is realized by formation of covalent (sp^2) bonds between carbon atoms in the CNT and few-layer Graphene (FLG). The Comparative *I-V* characteristics of the FLG/CNT and Cu/CNT heterostructure is shown in Fig. **(a),** where $R_{C\ (FLG/CNT)}$ (5.8 kΩ) of a single CNT is about ~6x smaller than the $R_{C\ (Cu/CNT)}$ (35.15 kΩ) and Fig. **(b-c)** are the SEM images from the corresponding studies using nanoprobe system from Zyvex in the 4PP configuration: red and black triangles symbols represent the measured data points and the corresponding lines connecting the respective data points are there to guide the eye.