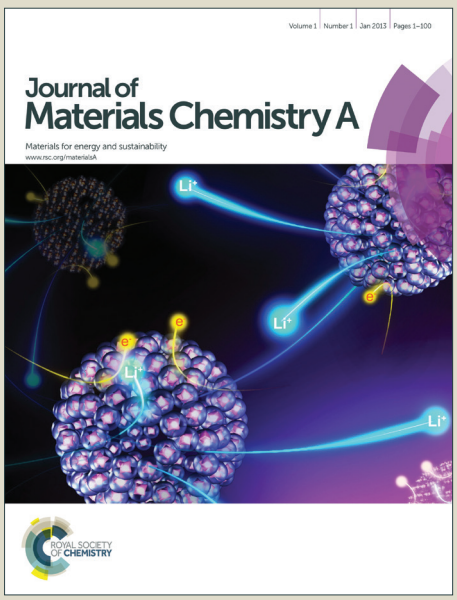
Journal of Materials Chemistry A

Accepted Manuscript



ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/materialsA

Integration of CNT in 3D-IC Interconnects: A Non-Destructive Approach for Precise Characterization and Elucidation of Interfacial Properties

K. Ghosh* [1,2], **Y. K. Verma**[1] **and C. S. Tan*** [1]

[1]**School of Electrical and Electronic Engineering, Nanyang Technological University,50 Nanyang Avenue, Singapore 639798;** [2]**Institute of NanoScience & Technology, Habitat Centre, Phase-10, Sector-64, Mohali, India 160062**

Abstract:

Multi-Walled Carbon Nanotubes (MWCNT) are one of the most promising nanomaterials having an array of novel functionalities and performance advantages which make them highly likely candidates to replace metals, like copper and aluminum, in the low-dimensional interconnects in three-dimensional (3D) integrated circuits (3D-IC) and sensors. Low-resistivity, large current-density, high thermal-conductivity (10□ times that of copper), and a low-coefficient of thermal expansion (CTE) make MWCNTs as a prime choice for integration in next-generation 3D-chip stacks. However, growth of carbonaceous nanomaterials on top of metals gives rise to issues of high interfacial resistance at the Metal/MWCNT interfaces due to largedifferences in their potential work-functions. Though it has become feasible to grow vertically aligned MWCNTs on metal lines, it has not been possible to systematically and precisely determine the interfacial contact resistance values between the as-grown single-, or bundle-MWCNTsand the base metal-lines.Here, we report a novel experimental method for measurement of metal/carbon interface contact resistance with aid of nanoprobing setupthereby eliminating undesirable metal-pad deposition step;must in the conventional techniques.In the present approach, nanoprobes are placed in contact with individual CNT-bundles making direct electrical contacts. Two-point-probe (2PP) and four-point-probe (4PP) measurements are systematically performed toaccurately estimate values of the contact-resistance at the Metal/CNT interface. The asmeasured interfacial contact resistance for a Bundle in2-5μm diameteroxide-*via*is found to be~730Ω, while on a per-CNT

basis the Metal/MWCNT contact resistance is ~35 kΩ. The here reported values of interfacial contact resistance are quite lower than those reported elsewhere in the literature. The characteristic novelty of current experimental approach lies intotal elimination of any steps involving further chemical, mechanical or physical processing which cause deformation and/or damage to the intrinsic properties and morphology of as-grown CNT-bundles. Uniquely, no alteration needs to be made to properties or environment of as-grown MWCNTs. Theadvantages of this approachresults in relatively more accurate and error-free determination of the Metal/CNT interfacial resistance values than any of earlier techniques.

Carbonaceous nanomaterials are poised to provide significant enhancements to material performance,providing technical-means for acceleration of the ongoing scaling trend in the Semiconductors industry.[1,2]Future advancements in the key areas of design and fabrication of high-performance and multi-functional sensors, Very/Ultra Large Scale Integrated circuits (VLSI/ULSI) depends critically on the promise of development of novel technologies and scientificcapabilities which enable the ongoing trend of scaling of dimensions to continue further.[3-7]Only-when this becomes feasible, the oxide-*via* interconnectsat the Back-End-of-Line (BEOL) will be able to keep-pace with ITRS roadmap projections for aspired high-density coverage of the chip real-estate. Successful three-dimensional (3D) stacking of the disparate,integrated chips with logical, RF, sensors, memory, and CCD circuit elements can be realized by incorporation of an extensive network of‘Through Silicon Via’(TSV) based interconnects.[8-17]However, continuous downscaling of the interconnect dimensions has reached a technical roadblock, and faces several performance challenges ofinput/output (I/O) bottlenecks, significantly higher*RC* signal-delays, reliability and durabilityissues, new design complexities hindering effective integration, and void-free conformal filling of the *Vias.*[2,18-24]

The scaling trend of continuous miniaturization of feature-sizesofmetal-lines and interconnectshas reached a critical stageas small dimensions giverise to novel, non-classical quantum-effects that undermine the system’s performance.[25]At low-dimensions, new problems arise in form of unexpectedly high-resistivity values of interconnects due to enhanced charge-scattering and large-number of grain-boundaries.[26-28]The serious issues of undesirable deterioration of the overall system performance due to scaling of the metal-lines,[29]are compounded further by the challenges of heat dissipation in low-dimensional features.[30] Current-crowding and phonon-blockage are other detrimental phenomena that cause significant performance-degradation in interconnects; including problems of (i) electro-migration of metal atoms,[31,32] (ii) de-lamination of thin-filmsdue to the creation and multiplication of voids,[33-36](iii) generation of thermo-mechanicalstresses due to mismatch in the coefficient of thermal expansion(CTE) between bulk-silicon and *via*-filling materials,[32,37-39](iv) creation of hot-spots inside the interconnects;all of which,together contribute to degradation ofcombined performance of the system.[32,40]Thus, there is a strong need for development of next generation materials that provide desirable and robust physical,

electrical and thermal properties that lend them technical feasibility for integration in nanolelctronics and semiconductor devices.

Carbon nanotubes have some quite extraordinary physical, mechanical, chemical and morphological properties that make them one of the most attractive nanomaterials for various applications in wide range of nanoelectronics devices. Multi-Walled Carbon Nanotubesoffer metallic conductivity, and are proposed as the possible nanomaterials for replacement of metals like copper and tungsten in interconnects.[1]CNTs have highest of the known coefficient of thermal conduction,[41,42]low resistivity, and low- CTE values[43,44] between ±0.4 □10^{-6} $K^{-1}$and can support high current densities[45,46] ~10^{9} mA/cm^{2}which makes them highly attractive for implementation in back-end, and global interconnects.Creation of reliable, robust andseamlesscontacts between CNT/Metal heterostructures, along withlow thermal/electricalcontact resistanceat their mutual interfaces, and its precise experimental measurement are some of the key-fundamental challenges, and critical technical issues that need to be resolved. When reasonably accurate solutions to these issues are realized, the objective of large-scale integration of CNTs in interconnectswill become technically feasible in the nanoelectronics and semiconductor industry.

Current research-endeavors areactively focused on issues related to realization of low-interfacial-resistance contacts at the CNT/Metal interface[47-49] and have relied on differenttechniques in their quest for low-barrier-resistance CNT/Metal contacts.According to the prevailing scientific research directions, primarily three approaches are more common and widely prevalent. These can be mainly categorized into (a) additive techniques;involving sequential steps of oxide-deposition, trimming of protruding CNTs and planarization of top-surface by Chemical Mechanical Polishing (CMP), followed by metal-padding through either electrochemical, or physical vapor deposition (PVD) methods, (b) destructive approach of scanning spreading resistance microscopy (SSRM); involvingstepwise material removal in successive scanning steps, with aid of doped, ultra-sharp, diamond probes.[47]

CMP process for wafer-planarization involve trimming of the protruding CNT top-ends and opening of MWCNT's inner-walls, which leads to creation of new electrical pathways, parallel channels for charge conduction. This leads to significant decrease of the overall *via-*

resistance from 36 Ω to 0.9 Ω.[45,50-52]Next step is creation of top-bottom electrical contacts through the CNT *vias*, by (a) PVD deposition of metal pads covering hundreds of TSV-*vias*, or (b) spatially selective, electrochemical deposition of metal electrodes over top of individual CNT-filled *vias*. On the other hand, recently demonstrated electrical atomic force microscopy (AFM) based destructive-approach of SSRM[47] does not require deposition of any metal pads on the top for measurement of the contact resistance. Rather, SSRMrelies on the art of successive slice-and-view approach of material elimination for acquisition of two-dimensional (2D) maps of resistance values at different heights, which are then stacked together to form3Dtomographic representation of resistance values,right down to the CNT/Metal interface.

However, there are significant disadvantages and systematic errors intrinsic to the above-mentioned techniques thatare inherently inaccurate,impreciseand non-scalable,and thus not suitable for universal scientific and technological implementation. CMP process involve extensive exposure of the as-grown CNT bundles to hostile-processing environment and harsh-chemicals that potentially contaminate and thereby cause physio-chemical alterations to the chemical properties, and also result in deformation of the physical morphology of the CNT bundles and *via*-structures; adversely affecting their electrical properties critical to overall performance of the system. During deposition of the top-metal pads in electrochemical processon top of individual *vias*, a potential-difference is applied across top and bottom ends of oxide-*vias*. This method creates a high-possibility for downward seepage of the metal particles inside the *vias*; more than 40% of the as-grown CNT volume being void. Thediffusive but steady percolation of metal particles inside the oxide-*vias* leads to creation of continuous metallic-filaments thatforman unbroken conductive path from top to bottom electrodes.[53,54] Formation of such channels creates undesirableelectrical conduction pathsbetween *via*'s two-ends; in parallel to that through the CNT-Bundle. Creation of metallic conductive pathways in *vias* will cause significant reduction of the oxide-*via* resistance,giving erroneous results and imprecise values for the measured contact resistance values.Similarly, PVD deposition of metal-pad provides a continuous coverage over large surface-area that includes hundreds of oxide-*via* tops as also theintermediate oxide-area between *vias.*[18,55]But, this leads to creation of new, unwanted, charge-trapping and charge-leakagecausing paths that will highly-likely electrically-connect top and bottom

electrodes,even through the intermediate oxide-barrier-layer. These undesirable electrical/charge conduction pathways are source oferroneous and false contributions in the measured interface resistance values.

Further, SSRM is basically a destructive approach involving creation of irreversible mechanical and physical changes to the native structure of few-CNTs even while being measured.[47]Consequently, this method cannot be an exact or an error-free way to determine the CNT-bundle, and CNT/Metal interface resistance values. Additionally, due toits gradual and non-scalable nature, this method is not appropriate for large-scale adoption, or forfacileincorporation into the process-integration flow in nanoelectronics and semiconductormanufacturing.

Hence, there'sa strong and urgent need for finding a suitable novel approach, which is repeatable, readily scalable, non-destructive, widely adoptable by the industry, and which precludes steps involving a need for exposure of the CNTs to any form of harsh chemicals, undesirable physical alteration or morphologicaldamage.The optimum approach should allow for *in-situ* measurement of electrical and other properties of the as-grown CNT-bundles in interconnects, without introducing any changes to their thermal, mechanical, chemical or physical properties.

Despite of an extensive number of methods for the estimation of CNT/Metal contact resistance, there is anobvious lack ofa standardized techniquefor exact estimation of CNT to metal contact-resistance values. Detailed survey of existing literature brings to light a variety of approximations and assumptionsadopted for determination of CNT/Metal interfacial contact resistancesby different research groups.[47-52]This creates valid scientific concerns about the approachesmentioned being essentially non-equivalent and non-comparable with each other. Further, complicating the matter, samplesfor different studies are fabricated in different conditions, using disparate and non-equivalent growth techniques (variable catalysts/metals/growth-temperatures/isolation-layers and process-flow),which makes it hard to compare the results in a straightforward manner.

In the reported work, we present experimental details for relatively more precise determination of individual contributions of the (i) CNT bundle resistance (R_{CNT}), (ii) contact

resistance ($R_{CNT/Cu}$) from the total *via*-resistance (R_{Via}), in a non-destructive, facile, reliable and repeatable approach. State-of-the-artelectrical characterization techniques of four-point-probe and two-point-probe, 4PP/2PP,are used for high-precession, electrical nano-probing measurements that are done with aid of nanoprobe-setup integrated with a standard SEM system.

Further information about the growth, fabrication and process-engineering steps are elucidated and stated in greater detail elsewhere.[56] Briefly, the process-flow starts with bulk 6" diameter primesilicon wafers(Bonda Technology PTE Ltd) that are cleaned following a standard RCA process, followed by thermal growth of 200 nm silicon-dioxide in the furnace following a standard oxide-deposition recipe.Wafer is then patterned using standard lithographic techniques(Karl Suss MA-6, Double Side Aligner) with use of S1813 photoresist (PR), followed by sequential deposition of (i) 10 nm of Ti (99.999%) to prevent copper diffusion into silicon, (ii) 100 nm of Cu (99.999%), (iii) 6 nm of Al (99.999%), and (iv) 4 nm of Al_2O_3(99.999%)inside E-Beam evaporator at nominal vacuum of 5 x10^{-6} mbars at room-temperature conditions(Edwards DP, Auto 306); distance between the targets and the substrate is fixed at 15 cm. The thin Al_2O_3 layer acts as an anti-diffusion, barrier layer for CNT catalyst. Afterwards, lift-off is done using acetone (60°C; 20 minutes), and leads to manifestation of underlying metal-lines that will work as electrically conducting pathways connecting different VACNT bundles.This, integrated, system of multiple metal thin-films deposited as a vertical stack defines the metal-lines. Then, 1 μm thick PETOS oxide layer is then deposited by thermal decomposition of tetraethyl-ortho-silicate (MRL LPCVD TEOS, LT).

Second lithographic step is used to transferfeatures of secondary mask on top of the as-deposited oxide layer while ensuring itsperfect alignment with the aid of top-side alignment (TSA) marks created in a previous step. Subsequently, wet-etching (Buffered-Oxide-Etchant (BOE)) process leads to creation of a large-scale array of oxide-*vias* on top of pre-deposited metal lines. Following this, ~1 nm iron (Fe) catalyst thin-film is deposited (Denton thin-film sputtering system, 10^{-6} mTorr Vaccum at room-temperature), and lift-off is done in acetone (1 hour, 60 °C), followed by UV-Ozone treatment (30 W: 30 sccm O_2: 3 mins) for evaporation of excess of adhering PR particles from top of the catalyst layer.

The wafer is thenready for dicing, and is diced into small 1" x 1" sizes dies, and placed inside Axitron's Black-Magik System (BM) for growth of VACNTs in thermal Mode (550 °C, H_2:50 sccm, C_2H_2:150 sccm, Ar:100 sccm). In this approach, precursors are showered from top-head giving rise to uniform growth of CNTs all over the die surface. Vertically aligned MWCNTs, length ~10 µm, grow in duration of 2 minutes.

Structural characterization of the as-grown CNT samples is doneusing scanning electron microscope (LEO 1550) to image the sample topography. The TEM-lamella is prepared from the as-grown CNT samples using Focused Ion Beam (FIB: DA300, FEI Inc) system operating with gallium ion-beam at 30 keV power. Detailed structural insights are gained with aid of ultra-high-resolution transmission-electron microscope (HRTEM) Tecnai X-TWIN system working with an electron beam-power of 200 KeV providing 0.14 nm resolution. The high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM)imaging allowshigher, better contrast imagesshowing intrinsic details of the CNT morphology. EDX, attached to the same TEM setup,provides further insights through spatially-resolved quantitative elemental mapping which imagesprecise distribution of elements at cross-sectional interfaces.

Further, DC electrical characterizationstudies are done using commercially available Zyvex S100 Nanomanipulator system,in the four-point-probe and two-point-probe (4PP/2PP) configurations.After cleaving the CNT-containing die into small pieces, samples are transferred to tilted sample-holder attached to a custom-designed sample-stage inside the SEM system:whole nanoprobing setup being located in the vacuum chamber of SEM. The 50-nm sharp tips-ends of the tungsten (W) allow for individual manipulation of CNT bundles, and measurement of their characteristic *I-V* curves (Keithley 4200 DC parameter analyzer).

Thermal-PECVD grown VACNT Bundles through the oxide-*vias*on top of copper- metal-lines are shown in Fig. 1. SEM images confirm the uniform and dense CNT-pillars, Fig. 1(a), with a bundle-diameter of ~10 µm and aspect ratio of ~ 1. Fig. 1(b) shows a close-up image of a selected CNT-bundle. The as-grown CNT bundles are electrically connected with each other through a network of underlying copper-metal lines, which allows electrical characterization in typical 4PP and 2PPmeasurement architectures.Fig. 1(c) shows top-view

of the four tungsten (W) nanoprobes making electrical-contact with top-end of the CNT-bundles in the 4PP configuration, where probes P_1 and P_4 conduct current while, simultaneously, probes P_2 and P_3 measure the corresponding potential difference. Figs. 1(d)-(e) show the images of nano-probing contacts made in 2PP architecture for electrical characterization between different *vias* varying from 1 to 20, whereas Fig. 1(f) illustrates a global-view of the schematic adopted for *I-V* measurements.

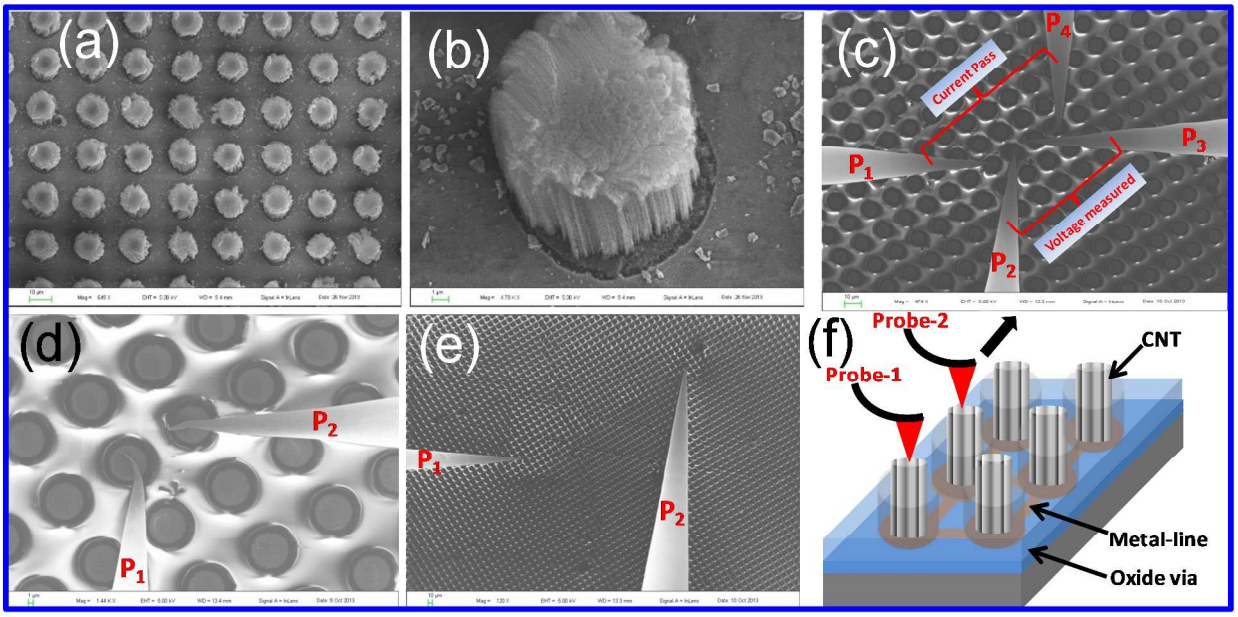


Fig. 1. Growth of CNT bundles on Cu-metal lines through oxide via and the estimation of Cu-CNT contact resistance **(a)** Low magnification image of the array structure; **(b)** zoomed in view of 3µm height, dense CNT-bundle growth through individual via of 1µm depth and 5µm diameter; **(c)** 4-probe measurement setup in nano-manipulator, where probes (P_1 to P_4) are kept in a sequence of one via gap interval of the array structure and terminal probes (P_1 and P_4) are passing the current and middle probes (P_2 and P_3) are measuring the voltage; **(d)-(e)** 2-probe measurement setup where P_1 is kept fixed and P_2 moves in a sequence of 1,2,3,4,5,10 and 20 via number and the corresponding current-voltage is measured; **(f)** Schematic of nano-probe architecture and setup, showing electrical connectivity amongst all CNT-bundles through underlying network of metal-lines.

Further structural & interface characterization studies are done to acquire detailed insights about the Cu/CNT hetero-structures. Fig. 2(a) shows a cross-sectional view of the CNT bundles post deposition of ~25 nmSiO_2,which protects CNT's crystalline graphitic structure

during the course of FIB sample-preparation step. Deposition of a thin oxide-layer leads to the densification of the CNT bundles,[57] reducing their diameters to ~ 6 µm. Fig.2(b) images the tip-regions of the vertically aligned CNT bundles on the TEM grid, without any FIB treatment, while Fig. 2(c) shows a high-resolution TEM (HRTEM) image of individual CNTs. One finds that the CNT wall numbers vary from double to four walls, having an average diameter of ~5 nm. To obtain deeper insights into Metal/CNT heterostructure's interface, a TEM lamella is prepared following the standard FIB processing steps.The three distinct segments corresponding to the Si/SiO_2//Metal, Metal/CNT interfaces are clearly visible in the TEM image, Fig.2(d).

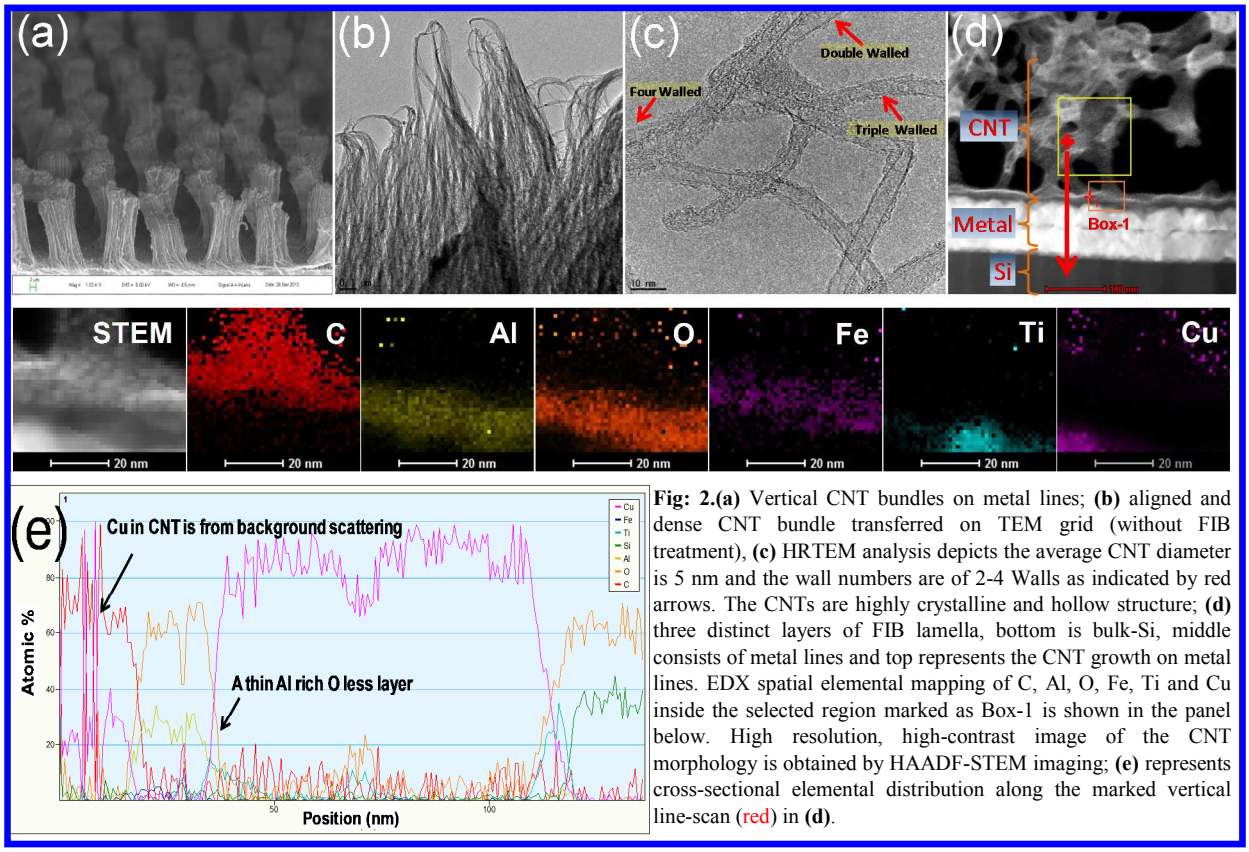


Fig: 2.(a) Vertical CNT bundles on metal lines; **(b)** aligned and dense CNT bundle transferred on TEM grid (without FIB treatment), **(c)** HRTEM analysis depicts the average CNT diameter is 5 nm and the wall numbers are of 2-4 Walls as indicated by red arrows. The CNTs are highly crystalline and hollow structure; **(d)** three distinct layers of FIB lamella, bottom is bulk-Si, middle consists of metal lines and top represents the CNT growth on metal lines. EDX spatial elemental mapping of C, Al, O, Fe, Ti and Cu inside the selected region marked as Box-1 is shown in the panel below. High resolution, high-contrast image of the CNT morphology is obtained by HAADF-STEM imaging; **(e)** represents cross-sectional elemental distribution along the marked vertical line-scan (red) in **(d)**.

Elemental analysis of selected area, marked by Box-1, with EDX reveals the spatial distribution of the elements like C, Al, O, Fe, Ti and Cu inside the region. The distribution of these elements is shown in color by images in the middle-panel of Fig. 2. On the other hand, high-resolution, high-contrast image of the CNT morphology is obtained withSTEM-HAADF imaging. Further, cross-sectional elemental distribution of these elements along the

vertical (red) arrow-line in (d) is represented in the Fig. 2(e). The observed peak for Copper intensity in the elemental line-scan at the location of the CNT is a proof of directcontact between CNT and Cu that creates a conductive path from metal-lines to the vertical CNT enabling facile electrical-charge transfer from horizontal to vertical interconnects. Presence of Cu near to the CNT-bottom ends implies that the copper atoms diffuse upwards through the thin, porous Al/Al_2O_3 layer. Likewise, impressions of Ti inregion of copper thin-film, and near Cu/Al interface indicates that Ti atoms have diffused through macroscopic grain-boundaries during annealing and CNT growth steps.

To reduce significant barrier-resistance at the Metal/CNT interface, a smart and logical fine-tuning of the interface material properties is adopted with bilayer deposition of Al_2O_3 on top of Al, creating less resistive, aluminum-rich, aluminum-oxide alloy. The standard thickness of the catalyst-sintering barrier-layer of $Al_2O_3$is minimized from 10 nm to 4 nm, which is deposited on top of Al thin-film(6 nm). The method offers unique advantage in that during the subsequent annealing steps, prior to the CNT growth, aluminum and copper atoms from the bottom-layer diffuse into the top Al_2O_3 layer,Fig. 2(e). The upward diffusion of metal atoms is of great advantage as it leads to significant reduction of overall barrier-resistance at the CNT/Metal interface, as confirmed afterwards by*I-V* characterization investigation.

From the perspective of CNTs potential applications in the TSVs,electrical properties of the as-grown CNT-bundles in 1µm deep oxide *vias*are measured using a nano-manipulator setup integrated inside the chamber of the regular SEM system. Characteristic *I-V* data measurements are done in the 2PP architecture mode, and typical representative data obtained are plotted in Fig. 3(a). The plots correspond to variation of *I-V*and implicitly of resistance values with increasing distance between measured TSV-*vias*.Electrical properties are also measured in 4PP architecture, whichenables direct electrical-contact with the CNT-bundles. The inset to the Fig. 3(a) shows comparative *I-V* data for adjacent *vias* in 2PP and 4PP modes. In both configurations, the experimentally measured resistance of CNT-TSVs is greater than 1 kΩ; implying thesufficiency of 2PPmode for further electrical characterization studies. Thus, all further results discussed are for studies done in the 2PP mode configurations only.

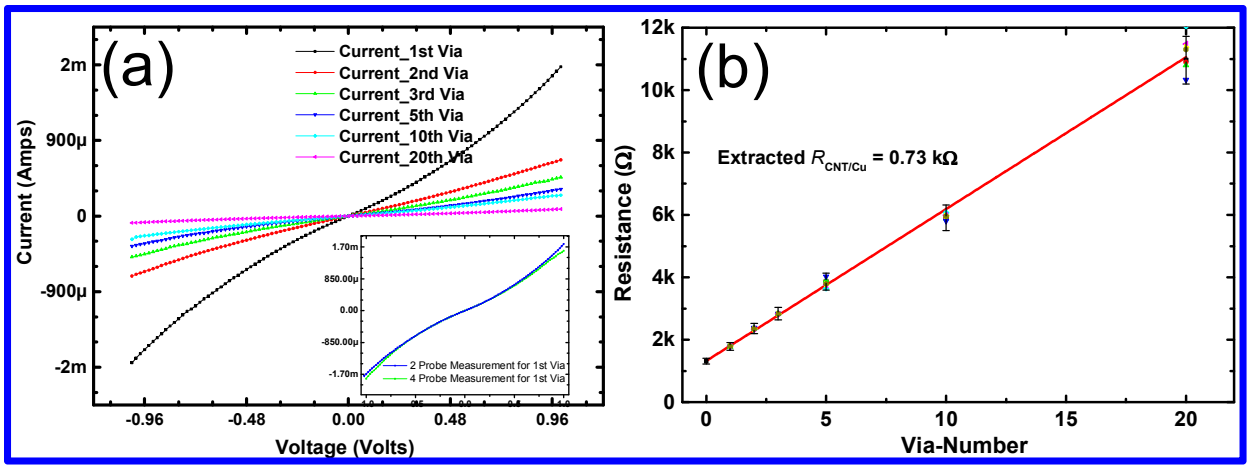


Fig. 3. Current-Voltage characteristics of CNT-Cu-CNT structure and extraction of CNT-Cu contact resistance using 2PP technique **(a)** *I-V* plots of variable via gaps where probe-1 is fixed and probe-2 is shifted from 1st, 2nd, 3rd, 5th, 10th and 20th via gap and the corresponding resistance values varied from ~1.8 kΩ to 11.3 kΩfrom 1stto 20th via; the inset to this plot refers to the comparative study of the *I-V* characteristics when measured by 2PP & 4PP techniques for same sample. Plot **(b)** shows a linear-fit through the averaged resistance-values in the voltage-range of ±0.5V to ±1V for each via. The linear relationship between Resistance versus Via-number allows for extrapolation to the zeroth-via refers to the $R_{CNT/Cu}$ contact resistance of 0.73 kΩ.

The observed *I-V* trends, Fig. 3(a), are quite linear, indicating almost ohmic contacts between the metal-lines and CNTs. The enhanced conductivity at the Metal/CNT interface can be attributed to the smaller thickness of oxide barrier-layer between metal-lines and the CNTs. The increase of the overall resistance of extracted $R_{Cu/CNT}$ with the distancecanbe explained by (i) nonlinear increase in the number of charge-trapping centers with the dispersion area, as the probe-tips move farther from each other, (ii) charge spreading-effect which happens due to increase in the number of pathways through which leakage current or charges can flow from one pointto another; getting trapped in the process. Plausibly, increase of charge trapping occurs because of numerous defects that exist at the metal/CNT interfaces, as also due to increasing number of Cu/CNT contacts as the area under test is incrementally enlarged.

A careful observation reveals that*I-V* characteristic curves become increasingly non-linear as the *via*-gap reduces from that between the 1st and 20th*via*to that of two-adjacent *vias*due to decrease in the linear part of the measured total resistance of the metal line. As a result of

which, relative percentage of the non-linear contribution due to Schottky effect becomes slightly higher. The Schottky effect arises due to difference in the work-functions of the copper and MWCNT, as well as due to the presence of an Al-rich, Al_2O_3(~4 nm thin).Separately, a detailed analysis of the non-linear component of the *I-V* curves shows that percentage-wise contribution of the non-linearity increasesfrom ~14.6% to about 18%at particularly given voltage (0.4 V), as the distance between probed *vias* decreases from equivalent to that of twenty-*via*to a group of adjacent*vias*.

The so calculated average resistance values, taken from the respective individual *I-V* curves with voltages in range of ±0.5 Volts to ±1 Volts are plotted in the Fig. 3(b), which show an almost linear-dependence of resistance on *via*-to-*via*distance. Further, a linear-fit is done to the plotted values of resistance versus *via*-number trend-line to better elucidate their mutual correlation. These values are used for extrapolation of the fitted trend-line to the distance of zeroth-*via*, in order to obtain the self-resistance of an individual *via*, R_{Via}. The resistance R_{Via} includes the contributions from several components, such as $R_{Probe/CNT}$, R_{CNT}, and $R_{CNT/Cu}$,

$$\boldsymbol{R_{Via} = R_{Probe/CNT} + R_{CNT} + R_{CNT/Cu}}$$

where one can safely neglect minorcontributions from the underlying metals-lines (< 20 Ω);metal-line resistance magnitudesbeing smaller than 0.5% of the measured R_{Via}. To identify the contributions of $R_{CNT/Cu}$ from the total *via*-resistance, we separately measured the $R_{Probe/CNT}$and R_{CNT} resistance values on a single CNT-bundle, Fig 4(a) and (b), in the 2PP and 4PP configurations, respectively, which are then subtracted from the R_{Via} to obtain $R_{CNT/Cu}$. Fig. 4(c) shows the *I-V* curves corresponding to the measurements on single CNT Bundle in 2PP and 4PP arrangements. Thereby, the estimated $R_{CNT/Cu}$ resistance value is found to be 0.73 kΩ in the present report.

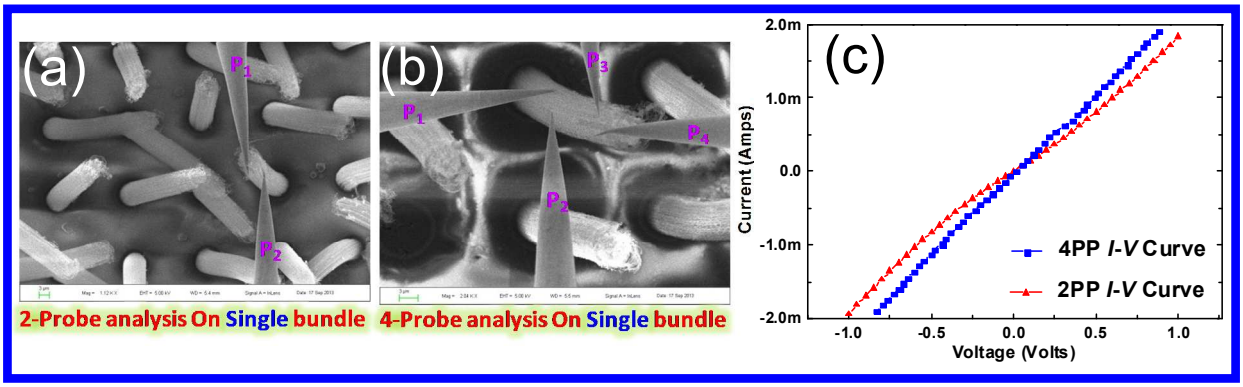


Fig. 4.SEM images of the 2PP & 4PP methods use to extract R_{CNT} and $R_{CNT/Probe}$resistances **(a)** depicts the two-point-probes of the nanomanipulator setup where contact has been made to a CNT bundle, while **(b)** shows the architecture for four-point-probe measurement used to measure the resistance of a single CNT bundle, and **(c)** plots the *I-V* values obtained in 2PP and 4PP modes wherefrom one can estimate the R_{CNT} and $R_{CNT/Probe}$ to be 1.2 kΩ and 0.3 kΩ, respectively.

ITRS roadmap projections concerning integration of the CNTs in interconnect technology postulates the contact resistance, R_C, to be ~10% of the single-CNT resistance, R_{CNT}, in *via*.[1,29]But, a thorough literature search does not brings-up published reports that provide details for precise determination of the individual resistance values, R_C and R_{CNT}.Also, as per literature, CNT-*via* resistance varies over a wide-range, from 25 Ω[6]upto200 kΩ,[58] whereas resistivity values are in the range of 0.8-12mΩ□cm for the CNT-bundles grown on top of metal-lines (Au, Co-Silicide).For the case of single-CNT to metal (TiN) contact-resistance, the value rangesbetween 2.8 kΩ to 4.8 kΩ.Vanpaemel *etal*.[59]studied the characteristic CNT-*via*resistance in dependence on presence and absence of an isolation layer between the individual nanotubes; for instance, without Al_2O_3 isolation layer the 4PP resistance,R_{CNT}, of single-CNT grown on top of TiN is 51 kΩs, whereas with isolation layer it ranges from 4.9 - 6.3 kΩ.

On the other hand, Chiodarelli *etal*.[18] report R_{CNT} bundle resistance values to bebetween 100-140 kΩ, i.e. about three-orders of magnitude higher than in other reports. However still, the values quoted in these reports do not separate the different contributions from the R_C and R_{CNT}. Schulze*etal*.,[47]follow an innovative approach for the measurement of R_{CNT} using tomography based 3D 'Scanning Spreading Resistance Microscopy' (SSRM). They are able

to measure the interfacial contact-resistance of CNT-bundle/Metal heterostructure with high-precision using a slice-and-view approach. The R_C varies from ~146-541 kΩ per CNT (single-shell conducting), that is ~36% of the measured total *via* resistance. Whereas, in an earlier work on a similar sample, Chiodaralli *etal*. estimate the R_C from measurements ~~done~~ on about 576 CNT-*Vias* connected multiply (in-parallel) under each metal-pad to be around ~1.16 kΩs;there being 100 CNTs per bundle.[49]The ratio of the CNT/Metal contact resistance to the total *via* resistance in their report is found to be about 22%. In both of above cases, the R_C:R_{Via} is much larger than the postulated values by the ITRS guidelines.

In comparison, for our case the R_{Via} is ~1.2 kΩ, which is equivalent to a resistivity of ~66.2 mΩ□cm per bundle. Further, taking into account the total number of CNTs in contact with the probe-tip (~75 CNTs), the R_{Via} per single-CNT is about ~136 kΩ, out of which the $R_{CNT}$is ~90 kΩ; that is, ~66% contribution to the *via*-resistance is by the single-CNT, whereas, the $R_{CNT/Probe}$ resistance is ~11.3 kΩ. Thereby, remaining contribution to the total *via* resistance comes from CNT/Metal-line contact resistance, R_C. This means that the CNT-to-metal contact resistance, $R_{C,}$ is in our case is ~ 35 kΩ for a single CNT/Cu contact, that is~ 39% of the single-CNT resistance, which is in the same range as values reported elsewhere[47,48,55] and is almost 4□ higher than the postulated 10% limit of the ITRS roadmap.[1,29]There is further scope for reduction of the contact resistance between vertical-CNT pillars and horizontal conductive paths, in both local and global interconnects.

Conclusion:

In summary, major object of this study is to precisely measure and report the CNT/Metal contact resistance at their mutual interface as a step towards enabling the widespread integration of CNT in the TSVs. Towards this goal, a repeatable, non-destructive, and reliable approach is adopted based on the technique of nanoprobing in the four-point-probe and two-point-probe modes. A highly effective and smart approach has been implemented for the reduction of the undesirably high barrier-resistance of the conventional 10 nm Al_2O_3 layer, by introduction of an aluminum-rich, aluminum-oxide alloy. The, thin and porous

Al_2O_3 allows easy diffusion of the metal atoms from underlying metal-layer to the bottom-end of the CNT matrix, thereby reducing the CNT/Metal interface's barrier resistance. Detailed, high-definition, structural investigations provide conclusive evidence that the CNTs are anchored seamlessly to the metal-lines. Further, improvements to the process-flow, and fine-tuning of the fabrication and growth steps will enable the CNT-TSV technology to find a wide-scale acceptance by the nanoelectronic and semiconductor industry, and allow CNT heterostructures based interconnect technology to reach a point of commercial viability that will allowtechnical and manufacturing feasibilities for further, universal, integration with next generation interconnects.

Acknowledgement:

This research was supported by the Agency for Science Technology and Research (A*STAR) through the public sector fund (#1121202004). Authors are grateful to the support and resources from the Silicon Technologies Centre of Excellence (Si-COE). K. Ghosh, Y. K. Verma and C. S. Tan, are affiliated with NOVITAS (Nanoelectronics Centre of Excellence) at NTU.

References:

(1) International Technology Roadmap for Semiconductors ITRS-(2014). Available, http,//www.itrs.net/Links/(2013)ITRS/Home(2013).htm

(2) Y. Hayamizui, T. Yamada, K. Mizuno, R.C. Davis, D.N. Futaba, M. Yumura, K. Hata, *Nature,***2008**, 3,289-294.

(3) P.S. Peercy, *Nature,***2000,**406, 1023-1026.

(4) M.F.L.D. Volder, S.H. Tawfick, R.H. Baughman, A.J. Hart, *Science*, **2013**, 339, 535-539.

(5) T.H. Kim, T.H. Zhang, D.M. Nicholson, B.M. Evans, N.S. Kulkarni, B. Radhakrishnan, E.A. Kenik, A.P. Li, Ping. *Nano Lett*.,**2010**, 10,3096–3100.

(6) T. Wang, K. Jeppson, J. Liu, *Small*, **2011**, 7, 2313-2317.

(7) H. Okuno, A. Fournier, E. Quesnel, V. Muffato, H.L. Poche, M. Fayolle, J.C.R. Dijon, *Physique,* **2010**,11,381-388.

(8) J.H. Ahn, H.S. Kim, K.J. Lee, S. Jeon, S.J. Kang, Y. Sun, R.G. Nuzzo, J.A. Rogers, *Science,***2006**, 314, 1754-1757.

(9) D. Jiang, T. Wang, L.L. Ye, K. Jeppson, J. Liu*, ECS Transactions,***2012**, 44,683-692.

(10) K. Banerjee, S.J. Souri, P. Kapur, K.C. Saraswat, *Proceedings of the IEEE,***2001**, 89, 602-633.

(11) Q.Y. Tong, U. Gosele, Semiconductor Wafer Bonding, *Science and Technology* (John Wiley, New York), **1999**.

(12) C. Xu, H. Li, R. Suaya, K. Banerjee, *IEEE Trans. on Elec. Devs*.,**2010**, 57, 3405 – 3417.

(13) C. Xu, H. Li, R. Suaya, K. Banerjee, *Electron Devices Meeting (IEDM 2009) IEEE International*, **2009**, DOI:10.1109/IEDM.(2009).5424307, 1 –4.

(14) R. Xie, C. Zhang, M.H.v.d. Veen, K. Arstila, T. Hantschel,B. Chen, G. Zhong, J. Robertson,*Nanotechnology*, **2013**,24, 125603-7.

(15) K. Banerjee, S.J. Souri, P. Kapur, K.C. Saraswat, *Proc. IEEE,* **2001**, 89, 602–633.

(16) G.L. Loi, B. Agrawal, N. Srivastava, S.C. Lin, T. Sherwood, K. Banerjee, *Proc. 43rd ACM/IEEE DAC*, **2006,** 991–996.

(17) C. Xu, H. Li, R. Suaya, K. Banerjee,*IEDM Tech. Dig.,***2009**, 521–524.

(18) N. Chiodarelli, K. Kellens, D.J. Cott, N. Peys, K. Arstila, M. Heyns, S.D. Gendt, G. Groeseneken, P.M. Vereecken, *J. The Electrochemical Society,* **2010,** 157, K211-K217.

(19) J. Dijon, A. Fournier, P.D. Szkutnik, H. Okuno, C. Jayet, M. Fayolle, *Diam. &Relt. Mater*.,**2010**, 19,382-388.

(20) N. Sillon, A. Astier, H. Boutry, L.D. Cioccio, D. Henry, P. Leduc,*IEDM Tech. Dig*.,**2008**, 595–598.

(21) F. Liu, R.R. Yu, A.M. Young,J.P. Doyle, X. Wang, L. Shi, K.N. Chen, X. Li, D.A. Dipaola, D. Brown, C.T. Ryan, J.A. Hagan, K.H. Wong, M. Lu, X. Gu, N.R. Klymko, E.D. Perfecto, A.G. Merryman, K.A. Kelly, S. Purushothaman, S.J. Koester, R. Wisnieff, W. Haensch, *IEDM Tech. Dig*. **2008**, 599–602.

(22) J.V. Olmen, A. Mercha, G. Katti, C. Huyghebaert, J.V. Aelst, E. Seppala, Z. Chao, S. Armini, J. Vaes, R.C. Teixeira, M.V. Cauwenberghe, P. Verdonck, K. Verhemeldonck, A. Jourdain, W. Ruythooren, M. Broeck, M.P. Ten, A. Opdebeeck, T. Chiarella, B. Parvais, I. Debusschere, T.Y. Hoffmann, B.D. Wachter, W. Dehaene, M. Stucchi, M. Rakowski, P. Soussan, R. Cartuyvels, E. Beyne, S. Biesemans, B. Swinnen, *IEDM Tech. Dig*. **2008**,603–606.

(23) N. Miyakawa, E. Hashimoto, T. Maebashi, N. Nakamura, Y. Sacho, S. Nakayama, S. Toyoda, *ACM J. Emerg. Technol. Comput. Syst*., 2**008**, 4, Article 20, p-15.
Available, http,//portal.acm.org/citation.cfm?doid=1412587.1412593

(24) G. Katti, A. Mercha, J.V. Olmen, C. Huyghebaert, A. Jourdain, M. Stucchi, M. Rakowski, I. Debusschere, P. Soussan, W. Dehaene, K.D. Meyer, Y. Travaly, E. Beyne, S. Biesemans, B. Swinnen, *IEDM Tech. Dig*., **2009**, 357–360.

(25) W. Steinhögl, G. Schindler, G. Steinlesberger, M. Engelhardt, *Phys. Rev. B,***2002**, 66,075414-4.

(26) T.H. Kim, X.G. Zhang, D.M. Nicholson, B.M. Evans, N.S. Kulkarni, B. Radhakrishnan, E.A. Kenik, A.P. Li, *Nano Lett*.**2010**, 10,3096–3100.

(27) R.H. Koch, J.R. Lloyd, J. Cronin,*Phys. Rev. Lett*., **1985**, 55, 2487-2490.

(28) E. Glickman, M. Nathan, *J. Appl. Phys*., 1**996**, 80, 3782-3791.

(29) *International Technology Roadmap for SemiconductorsITRS* 2005. Available, http,//public.itrs.net

(30) R.H. Havemann, J.A. Hutch, *Proceedings of the IEEE,* **2001**, 89,586-601.

(31) M.P. Oxley, L.J. Allen, *J. Appl. Cryst*., **2003**, 36, 940–943.

(32) T. Gupta, *Copper Interconnect Technology***2009**, Chapter 7, 301-345.

(33) (i) K.H. Lu, S.K. Ryu, J. Im, R. Huang, P.S. Ho, *IEEE Int. Reliability Physics Symposium***2011**. (ii) Y. Chai, P.C.H. Chan, Y. Fu, Y.C. Chuang, C.Y. Liu, *IEEE Electron Device Lett*.,**2008**, 29, 1001–1003.

(34) T. Sullivan, *Int'l. Reliab. Workshop(IRW) Final Report***1998**.

(35) C.K. Hu, L. Gignac, R. Rosenberg, *Microelectron. Relib*.**2006**, 46,213-231.

(36) K.H. Lu, S.K. Ryu, Q. Zhao, X. Zhang, J. Im, R. Huang, P.S. Ho, *Electronic Components and Technology Conference* (ECTC) **(2010)** Proceedings 60th, pp, 40-45.

(37) J.A. Nucci, Y.S. Diamond, J.E. Sanchez, *Appl. Phys. Lett*.,**1995**, 66,3585-3587.

(38) V.R. Hunter, *IEEE Trans. Electron. Dev*.,**1997**, 44, 304-309.

(39) M. Jung, D.Z. Pan, S.K. Lim, DAC '12 *Proceedings of the 49th Annual Design Automation Conference*, **2012**, 317-326.
Available:http,//dl.acm.org/citation.cfm?id=2228360.2228419&coll=DL&dl=GUIDE&CFID=399613405&CFTOKEN=87098390

(40) K. Athikulwongse, A. Chakraborty, J.S. Yang, D.Z. Pan, S.K. Lim, *Proc. IEEE Int. Conf.Computer-Aided Design***2010**.

(41) (i) A. A. Balandin,Nature Materials 10**(2011)**569–581 (ii) E. Pop, D. Mann, Q. Wang, K. Goodson, H. Dai, *Nano Lett*.,**2006**, 6,96-100.

(42) D. J. Yang, Q. Zhang, G. Chen, S.F. Yoon, J. Ahn, S.G. Wang, Q. Zhou, Q. Wang, J.Q. Li, *Phys. Rev. B,* **2002**, 66, 165440-6.

(43) H. Jiang, B. Liu, Y. Huang, K.C. Hwang, *J. Eng. Mater. & Tech*., 2**004**, 126,265-270.

(44) A. Sinha, J.A. Mihailovic, J.E. Morris, H. Lu, C. Bailey, IEEE *Nanotechnology Mater. & Devices Conference* (*NMDC*), **2010**, 262-266.

(45) A.M. Ionescu, J. Dijon, J. Robertson, *Microwave Magazine IEEE,* **2011**, 12,42-50.

(46) K. Banerjee, L. Hong, N. Srivastava,*Proc. 8th IEEE Conf. Nanotechnology (NANO'08), Aug*. **2008**, 432–436.

(47) A. Schulze, T. Hantschel, A. Dathe, P. Eyben, X. Ke. W. Vandervorst, *Nanotechnology*, **2012**, 23, 305707-8.

(48) T. Wang, K. Jeppson, N. Olofsson, E.E.B. Campbell, J. Liu, *Nanotechnology*,**2009**, 20, 485203-6.

(49) N. Chiodarelli, S. Masahito, Y. Kashiwagi, Y. Li,K. Arstila, O. Richard, D.J. Cott, M. Heyns, S.D. Gendt, G. Groeseneken, P.M. Vereecken, *Nanotechnology,* **2011**, 22,085302-7.

(50) D. Yokoyama, T. Iwasaki, T. Yoshida, H. Kawarada, *Appl. Phys. Lett*., **2007**,91,263101-3.

(51) M. Nihei, M. Horibe, A. Kawabata, Y. Awano, Jpn. *J. Appl. Phys*.,**2004**,43 (4B), 1856–1859.

(52) N. Chiodarelli, A. Fournier, J. Dijon, *Appl. Phys. Lett*., **2013**,103, 053115-4.

(53) L. Mihalache, A. Radoi, C. Munteanu, M. Kusko, C. Kusko, *Organic Electronics,***2014**,15, 216–225.

(54) J. Li, Q. Ye, A. Cassell, H.T. Ng, R. Stevens, J. Han, M. Meyyappan, *Appl. Phys. Lett*., **2003**,82, 2491-2493.

(55) N. Chiodarelli, Y. Li, D.J. Cott, S. Mertens, N. Peys, M. Heyns, S.D. Gendt, G. Groeseneken, P.M. Vereecken, *Microelectronic Engineerin,* **2011**,88, 837-843.

(56) K. Ghosh, Y.K. Verma, C.S. Tan,*Carbon***2014** (*under review*).

(57) T. Wang, K. Jeppson, J. Liu, *Carbo,* **2010**,48, 3795–3801.

(58) C. Zhang, F. Yan, B.C. Bayer, R. Blume, M.H.v.d. Veen, R. Xie, G. Zhong, B. Chen, A.K. Gericke, R. Schlögl, B.D. Capraro, S. Hofmann, J. Robertson, *J. Appl. Phys*.,**2012**,111, 064310-6.

(59) J. Vanpaemel, M. Sugiura, Y. Barbarin, S.D. Gendt, Z. Toekei, P.M. Vereecken, M.H.v.d.Veen,*Microelectronic Engineerin,* **2014**, 120, 188-193.