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Thin film transistors based on two dimensional graphene and graphene/semiconductor heterojunctions

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During the past few years, two-dimensional (2D) layered materials have emerged as the most fundamental building blocks of a wide variety of optoelectronic devices. The weak van der Waals (vdW) interlayer forces allow the 2D monolayers to isolate and restack into arbitrary stacking heterojunctions. The recently developed chemical vapor deposition (CVD) technique shows great promise for the production of large domain building blocks of 2D heterostructures with vertical and lateral stacking and much better device performance. This review is the first of its kind to discuss the research progress of flexible FETs based on graphene/semiconductor heterostructures, in which graphene acts as both electrode and semiconductor material.

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1. Introduction

Two-dimensional (2D) materials, such as nano-films, superlattices and quantum wells, refer to the materials in which the free movement (plane motion) of electrons takes place only in the two dimensional non-nanoscale. Graphene is the most significant among all the 2D materials proposed up till now¹ and has single (or several) atomic layer thickness. Beyond graphene, 2D materials also include transition metal oxides (*e.g.* MnO₂, ZnO), transition metal carbides and/or carbonitrides (MXene), transition metal chalcogenides (*e.g.* MoS₂), hexagonal boron nitride (h-BN), topological insulators (*e.g.* Bi₂Se₃, Sb₂Te₃), silicene, germanene, black phosphorus (BP) and so on (Fig. 1).^{2–5} 2D materials as promising building blocks for novel nanoelectronics include semiconductors, insulators, transparent conductors and transducers,^{6–8} because amongst other considerations, these atomic sheets afford the ultimate thickness and scalability, which is desired in a variety of essential material categories. 2D semiconductors exhibit high carrier mobility, high on–off current ratio and excellent bendability that suit for future low-power consumption and flexible electronics.^{9–12} These materials are laterally composed of strong covalent bonds, which provide great in-plane stability. On the other hand, the weak van der Waals (vdW) interlayer forces allow us to isolate 2D monolayer and restack them into arbitrary stacking heterojunctions without the need to consider the

atomic commensurability in contrast to their bulk counterparts. van der Waals (vdW)-bonded layered materials offer great variety in both structural and electronic properties, opening up new avenues for scientific research to obtain better device design and desired device functionalities by assembling heterostructures based on distinct 2D layers. Although, all-2D vdW heterostructures offer unique properties and functionalities compared with conventional devices, it still remains a challenge to produce entire families of 2D materials and their heterostructures over large areas with high electronic quality. Furthermore, control of doping type, carrier concentration and stoichiometry is quite difficult for most 2D materials, limiting the scope and progress of all-2D vdW heterostructures.¹³

Graphene is the first truly 2D crystalline material, which is composed of periodic honeycomb lattice formed by sp² hybrid orbitals of covalently bonded carbon atoms (Fig. 1b and c).^{12,14–17} The p orbital of coplanar carbon atoms overlap each other and form large conjugated π bonds. There is a freely moving electron at each grid point, which endow graphene to have super high electron mobility ($2 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) at low temperature ($\sim 5 \text{ K}$).^{1,18} Graphene is theoretically considered as zero bandgap semiconductor and the electronic conduction velocity and theoretical resistivity of graphene are $8 \times 10^5 \text{ m s}^{-1}$ (ref. 19) and $10^{-6} \Omega \text{ cm}^{-1}$,²⁰ respectively. Excellent electrical property of graphene favors the development of graphene based field effect transistors²¹ and the supercapacitors.²² In addition, graphene has high optical transparency²³ and has broad applications in the transparent conductive thin film solar cells, photon detectors and so on,^{24–28} due to its unique optical properties. In addition, graphene also exhibits ultrahigh mechanical strength (1.0 TPa),²⁹ exceptional thermal conductivity ($5000 \text{ W m}^{-1} \text{ K}^{-1}$),³⁰ half-integer quantum Hall effect at room temperature,³¹ Klein tunneling effect,³² and so on.

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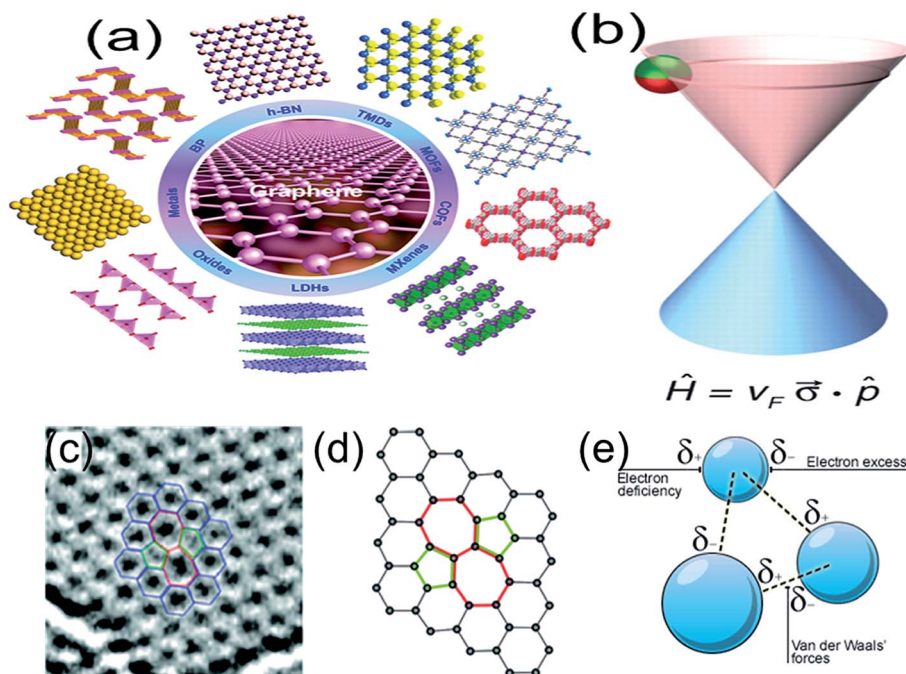


Fig. 1 (a) Schematic illustration of different kinds of typical ultrathin 2D nanomaterials, such as graphene, h-BN, TMDs, MOFs, COFs, MXenes, LDHs, oxides, metals, and BP. Reprinted with permission from ref. 3. Copyright 2015 ACS Publications. (b) Charge carriers in graphene are called massless Dirac fermions and are described by a 2D analog of the Dirac equation, with the Fermi velocity $v_F \approx 1 \times 10^6 \text{ m s}^{-1}$ playing the role of the speed of light and a 2D pseudospin $\vec{\sigma}$ describing two sublattices of the honeycomb lattice. Reprinted with permission from ref. 12. Copyright 2009 AAAS. (c) TEM image, reprinted with permission from ref. 13. Copyright 2011 ACS Publications. (d) Atomic structure of graphene obtained by DFT calculation. Reprinted with permission from ref. 14. Copyright 2008 ACS Publications. (e) vdW forces in a 2D layered structure. Reprinted from <http://bbc.co.uk>.

Transistors are the central device building blocks of all modern electronic systems. The first thin film transistors (TFTs) can be dated back to 1962,³³ which used vacuum evaporation technique along with shadow masks to deposit gold electrodes, an n-type polycrystalline cadmium sulfide (CdS) semiconductor channel and a Si monoxide gate insulator on a glass substrate. The integration of TFTs on flexible substrates is of considerable interest for diverse applications including electronic-paper, wearable display and artificial skin, and can enable a new generation of flexible, wearable and disposable electronics.^{34–37} The major challenges for the realization of high performance electronics on flexible substrates are the difficulties in achieving TFTs with a high carrier mobility, high on/off ratio, low operating voltage and using a low temperature-compatible fabrication process.

The highest carrier mobility, excellent optical transparency, high mechanical strength as well as atomic thickness of graphene layers make it extremely useful for flexible FET application. Fabrication of FETs using 2D graphene crystals as an active component can significantly contribute in the evolution of next generation flexible thin film electronic devices and there have been quite a few reviews summarizing the graphene-based TFTs and their applications.^{38–45} Keeping in view the high demand of graphene based flexible electronics, in this review, we summarize recent development of flexible FETs based on graphene and/or graphene/semiconductor heterojunctions, consistent

with the role of graphene as channel layer and/or electrodes in FETs.

2. Graphene acting as channel material in thin film transistors

For field-effect transistors (FETs), the level of its carrier mobility often determine the level of some other important performance parameters, such as current density, energy efficiency, switching delay, and so on. High mobility is beneficial to realize the maximum static control,⁷ optical transparency,⁴⁶ sensitivity⁴⁷ and flexibility,^{48,49} and broaden the application fields of TFTs. In this regard, graphene is one of the best choice for transparent conductive thin films in FETs, due to its excellent electronic, mechanical, optical properties and good stability as mentioned above.^{18,23,29}

Graphene transparent conductive thin films have been usually used as the conducting channel layer for graphene-based field effect transistors (GFETs). The main opportunities for graphene in both high-performance and low-power applications stem from the atomic thinness achievable in graphene-based devices, which lead to an almost perfect control of the channel potential. Very recently, Johari *et al.*⁵⁰ have reviewed the electrical performance of GFETs using various architectures and different geometries of graphene conducting channel layer. Graphene has great advantage for its use in flexible electronics but at the same time it needs



an opening of band gap for TFTs. Researchers had tried to get the good on/off ratio in graphene based FETs by fabricating the graphene as a channel layer. For example, graphene nanoribbon (a kind of graphene with width below 10 nm (ref. 51)) has been one of the most widely used conducting channel materials for GFETs. Wang *et al.*⁵² successfully synthesized graphene nanoribbons with smooth edges and size smaller than 10 nm. They demonstrated that the on/off ratio of GFETs increases with the decrease in width of graphene nanoribbon and at room temperature, the on/off ratio and carrier mobility were up to $\sim 1 \times 10^6$ and $\sim 200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. Processing graphene sheets into nanoribbons with widths of less than 10 nm can open up a bandgap that is large enough for room-temperature transistor operation, but nanoribbon devices often have low driving currents or transconductances. In comparison with graphene nanoribbons, the graphene nanomesh, which can be viewed as many graphene nanoribbons arrange orderly and periodically in another conducting channel material, cannot only introduce the band gap for graphene, but also dramatically increased the driving current of GFET devices.⁵³⁻⁵⁵ For instance, Bai *et al.*⁵⁵ successfully obtained the graphene nanomesh with width of 5 nm, on/off ratio of the GFET based graphene nanomesh was about 100, and the current density of GFETs based graphene nanomesh was about 100 times to that of GFETs based on graphene nanoribbons. They prepared the nanomeshes with variable periodicities and neck widths as low as 5 nm using block copolymer lithography.

3. Graphene acting as electrode material in thin film transistors

The conventional electrode of field effect transistors (FETs) is mainly metal or metal oxide with limited applications as a result of their disadvantages such as insensitivity, opacity, non-flexibility as well as large contact resistance between the metal electrode and the active layer of FETs. However, graphene electrode effectively overcomes the above disadvantages of the metal electrode for FETs. Therefore, graphene transparent conductive films are widely used as an electrode material for GFETs,⁵⁶⁻⁶² with a heterojunction structure between graphene electrode and the inorganic and/or organic semiconductor active layer.

Heterojunctions refer to an interface between two different semiconductors (electron donor and electron acceptor), where the electronic band structure near the interface is changed according to electrostatics.⁶³ The semiconductor heterojunctions have been applied in many solid-state devices, such as solar cells, photo detectors, semiconductor lasers, and light-emitting diodes (LEDs). In 1960, Anderson⁶³ successfully prepared high quality heterojunctions for the first time, and provided a detailed energy band diagram and theoretical models. Due to the great influence of the semiconductor junction in our daily life, Nobel Prize in physics was awarded to Zhores I. Alferov, Herbert Kroemer and Jack S. Kilby for their contributions towards the development of semiconductor heterostructures.^{64–66} The weak van der Waals (vdW) interlayer forces in 2D materials allow us to isolate 2D monolayer and restack them into arbitrary stacking heterojunctions without

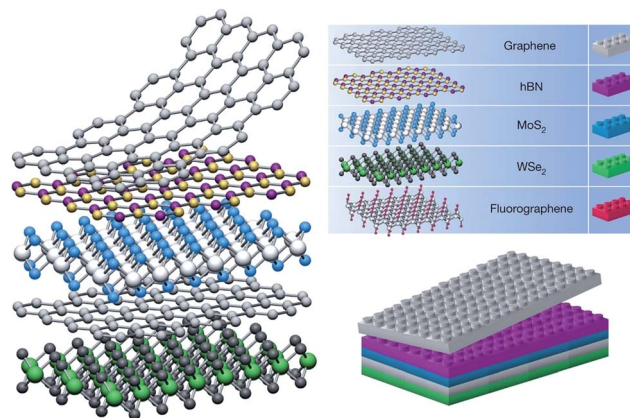


Fig. 2 Schematic 2D heterostructures based on van der Waals inter-layer force. Reprinted with permission from ref. 67. Copyright 2013 Nature Publishing Group.

the need to consider the atomic commensurability in contrast to their bulk counterparts. Hence, a new research field of heterojunctions formed by 2D layered materials has emerged since 2013.⁶⁷ The vertically stacked 2D layers can be formed by mechanical stacking, serving as a quick and convenient way of forming heterostructures (Fig. 2). In comparison with the horizontal (lateral) heterojunction, the vertical heterojunctions usually have higher electron transition efficiency due to their larger bonding area between two different heterostructured components.

3.1 Preparation of graphene/semiconductor heterojunctions

The semiconductor heterojunctions play an important role in modern electronics, being used as an essential building block of solid state devices, such as photo sensors, solar cells, light-emitting diodes and semiconductor lasers. Two-dimensional (2D) materials have the advantages of possessing unique optical bandgap structures and large surface area. Owing to the layered structures of 2D materials, the formation of heterostructures can be in vertical or lateral fashion. Depending on the architecture of the heterostructures, the fabrication methods vary. Here, we sort the fabrication processes into two categories, one is the mechanical stacking method and the other is the direct synthesis.

3.1.1 Mechanical stacking method. Owing to the invention of exfoliation and transfer methods of layered materials,¹ the mechanically or chemically exfoliated 2D flakes can be manually stacked to form 2D heterostructures, where the interlayer vdW forces hold the heterostructure securely. The 2D flakes can be mechanically/chemically exfoliated from bulk materials or isolated from the synthetic 2D layers on substrates. The stacking order and the interface of the heterojunctions are critical for their electrical and optical properties. The possibility to form various stacking lattice orientations provides the heterojunction interface with tunable physical properties depending on the interaction strength of the two layered materials. For example, the carrier mobility of graphene on SiO₂ is normally limited by the scattering effect of charged impurities, substrate

Year	Layer structure	Mobility/cm ² V ⁻¹ s ⁻¹	On/off ratio	Reference
2010	Graphene/h-BN	6×10^4	—	19
2012	h-BN/graphene/h-BN/graphene/h-BN	—	1×10^4	78
2012	h-BN/graphene/MoS ₂ /graphene/h-BN	—	50	78
2013	Graphene/h-BN/MoS ₂	~45	10^4 to 10^6	8
2013	Graphene/WS ₂ /graphene/h-BN	—	$>1 \times 10^6$	76
2013	Graphene/MoS ₂	—	$>10^3$	73
2014	Graphene/MoS ₂	—	$\sim 10^5$	71
2014	Graphene/h-BN/MoS ₂ /graphene	~33	$>10^6$	75
2015	h-BN/graphene/h-BN	3×10^4 to 3.6×10^4	—	74
2016	Graphene/BP	—	~800	72

^a Note: — indicate it is not mentioned in the references.

a wide range of van der Waals heterostructures (vdWHs) without the constraints of lattice matching and processing compatibility.⁶⁹ Since the discovery of graphene, it became clear that when a graphene nanosheet is combined with some inorganic semiconductors, the zero-gap shortcomings, that limit the on/off current ratio of graphene-based transistors, could be considerably reduced or even avoided.

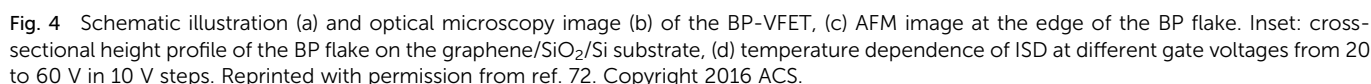
Graphene/inorganic semiconductor heterojunctions could be classified as binary^{19,70–74} and ternary^{8,75,76} heterostructures according to the components in the heterostructures (Table 1). Graphene-based binary heterojunctions usually include graphene/h-BN,^{19,77} graphene/MoS₂,⁷³ graphene/WS₂,⁷⁰ graphene/BP,⁷² and so on. For example, Yu *et al.*⁷³ reported the vertical integration of graphene/MoS₂ heterostructures of layered materials for the fabrication of a new generation of vertical field-effect transistors (VFETs) with a room temperature on/off current ratio >10³ and a high current density of up to 5000 A cm⁻² (Fig. 3a and b). Subsequently, Moriya *et al.*⁷¹ further improved the on/off ratio and current density of the VFETs based on graphene/MoS₂ heterostructures to 10⁵ and 10⁴ A cm⁻², respectively (Fig. 3c and e).

Very recently, Kang *et al.*⁷² presented a vertical field-effect transistor geometry based on a graphene/black phosphorus

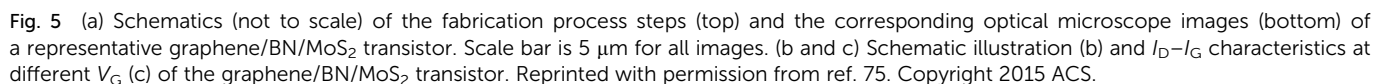
Figure 1 consists of five panels labeled (a) through (e). Panel (a) is a 3D schematic of the device structure. It shows a top electrode (drain) on a MoS₂ channel, which is connected to a source electrode. The channel is on a SiO₂ layer, which is on a Si (back gate) substrate. Graphene is used as a source/drain contact. Panel (b) is a scanning electron micrograph (SEM) of the device, showing the top electrode (drain), source, and gate stack. A scale bar of 5 μm is shown. Panel (c) is a cross-sectional diagram of the device. It shows the Au/Ti contacts, MoS₂ channel, SiO₂ gate, and n-Si substrate. The gate voltage V_g is applied to the SiO₂ layer. Panel (d) is a scanning electron micrograph (SEM) of the MoS₂ channel, showing the Au/Ti contacts. A scale bar of 2 μm is shown. Panel (e) is a plot of the on/off current ratio (I_{ON}/I_{OFF}) versus the gate voltage (V_g). The y-axis is logarithmic, ranging from 10⁻¹ to 10⁶. The x-axis is linear, ranging from 0 to 40 V. The data points show a clear ambipolar characteristic, with a minimum current around V_g = 15 V. The on-current (I_{ON}) is represented by red triangles and the off-current (I_{OFF}) by black circles. A dashed line indicates the trend of the on/off ratio.

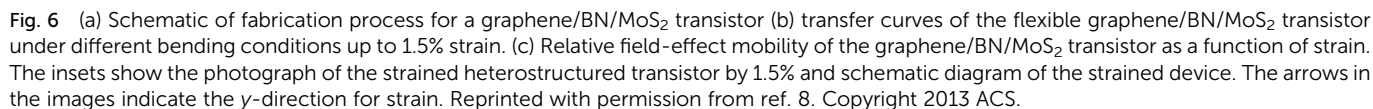
3.2 Graphene/inorganic semiconductor heterojunction TFT

Fig. 3 Schematic illustration (a and c) and optical images (b and d) of the vertically stacked graphene/MoS₂ heterostructured transistors. (e) The MoS₂ layer number dependence of the I_{on} (current density at $V_{\text{B}} = +0.5$ V and $V_{\text{G}} = +50$ V) and I_{off} (current density at $V_{\text{B}} = +0.5$ V and $V_{\text{G}} = -50$ V). Reprinted with permission from ref. 71 and 73. Copyright 2014 AIP Publishing LLC and 2013 Nature Publishing Group.



Some graphene-based ternary heterojunctions, such as graphene/h-BN/MoS₂ (ref. 75) and graphene/h-BN/WS₂,⁷⁶ have also been reported. For example, Roy *et al.*⁷⁵ successfully prepared a graphene/h-BN/MoS₂ heterostructured TFT in which graphene was used as the electrode and contacts material and MoS₂/h-BN heterojunction was used as the active layer (Fig. 5). This transistor exhibited n-type behavior with an ON/OFF current ratio of >10⁶, and an electron mobility of ~33 cm² V⁻¹ s⁻¹. Uniquely, the mobility does not degrade at high gate





Year	Layer structure	Mobility/cm ² V ⁻¹ s ⁻¹	On/off ratio	Reference
2014	Graphene/C ₈ -BTBT	—	~10 ⁶	87
2015	Graphene/pentacene	—	>10 ³	93
2015	Graphene/pentacene	—	8.7 × 10 ²	82
2015	Graphene/rubrene	<10	~10 ⁻¹	82
2015	Graphene/PTCDI-C ₁₃	—	3.8 × 10 ²	82
2015	Graphene/C ₆₀	—	2.0 × 10 ⁴	82
2015	Graphene/C ₆₀	—	>10 ⁴	83
2015	Graphene/C ₆₀	3000	8 × 10 ⁴	94
2015	Graphene/C ₆₀	—	3 × 10 ³	95
2015	Graphene/P3HT	—	>10 ³	91

Shih *et al.*⁸² synthesized a series of graphene/organic semiconductor heterostructured (*e.g.* graphene/pentacene, graphene/C₆₀) vertical thin film transistors (VFETs) with good optoelectronic properties (Fig. 7 and Table 2). Interestingly, they reported the first experimental evidence that the underlying mechanism of partially screened field effect and selective carrier injection through graphene dominate the electronic transport at the organic semiconductor/graphene heterointerface. They demonstrated flexible organic/graphene VFETs with bending

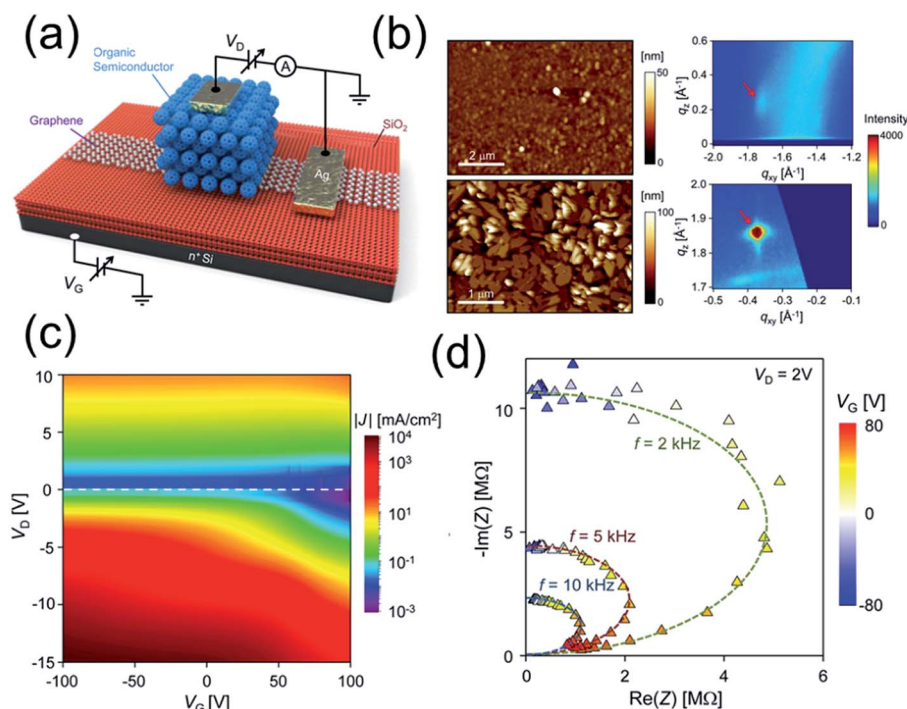


Fig. 7 (a) Schematic of graphene/organic semiconductor heterojunction VFET device. The black connections are associated with the setup for DC measurement. (b) AFM micrographs and the (112) reflection peaks in the GIXD images for ~ 100 nm PTCDI-BPE films on SiO_2 (top, edge-on phase) and graphene (bottom, face-on phase). (c) Transport color maps of J as a function of V_D and V_G for the pentacene VFETs on as-received SiO_2 substrate. (d) Trajectory of C_{60} impedance at fixed frequencies. By increasing V_G , the C_{60} layer is experiencing an insulator-conductor transition, moving from a pure dielectric towards a pure conductor. Reprinted with permission from ref. 82. Copyright 2015 ACS.

radius < 1 mm with the output current per unit area equivalent to that of the best oxide planar FETs.

As shown in Fig. 8, Hlaing *et al.*⁸³ reported organic thin film transistors based on vertical heterojunctions of graphene and organic semiconductors (pentacene and C_{60}). In these thin heterostructure devices, current modulation is accomplished by tuning the injection barriers at the semiconductor/graphene interface with the application of gate voltage. N-Channel devices fabricated with a thin layer of C_{60} show a room temperature on/off ratio $> 10^4$ and current density of up to 44 mA cm^{-2} . Because of the intrinsic ultra-short channel in the vertical structure, the device is fully operational at a driving voltage of 200 mV.

Kim *et al.*⁹³ demonstrated a flexible vertical Schottky Barrier (SB) transistor architecture based on a graphene-organic heterojunction and an ion gel gate dielectric. Specifically, an ion gel gate dielectric consisting of an ionic liquid within a network polymer was used to modulate the SB formed at the graphene-organic (p-type pentacene or n-type N,N' -dioctyl-3,4,9,10-perylenedicarboximide) heterojunction upon application of a bias at the gate located parallel to the source electrode. The resulting p- and n-type devices could be successfully operated at voltages below 1 V while yielding a high current density in excess of 100 mA cm^{-2} and a high on/off current ratio greater than 10^3 .

Liu *et al.*⁹¹ fabricated high-performance organic vertical thin film transistors (OVTFETs) based on graphene/organic



Fig. 8 (a) Schematic illustration of the three-dimensional and cross-sectional view of the vertically stacked graphene-organic semiconductor-metal VOTFT. (b) Semi-logarithmic I_D - V_{GS} transfer characteristics of an n-type VOTFT measured at V_{DS} values of 0.2 and 0.5 V. I_G is indicated by the dashed line. (c) On- and off-current density (top) and transconductance (bottom) at various drain voltages measured at fixed gate voltage of 3 V. The active area of the transistor measured is $3 \times 10^{-3} \text{ cm}^2$. Reprinted with permission from ref. 83. Copyright 2015 ACS.

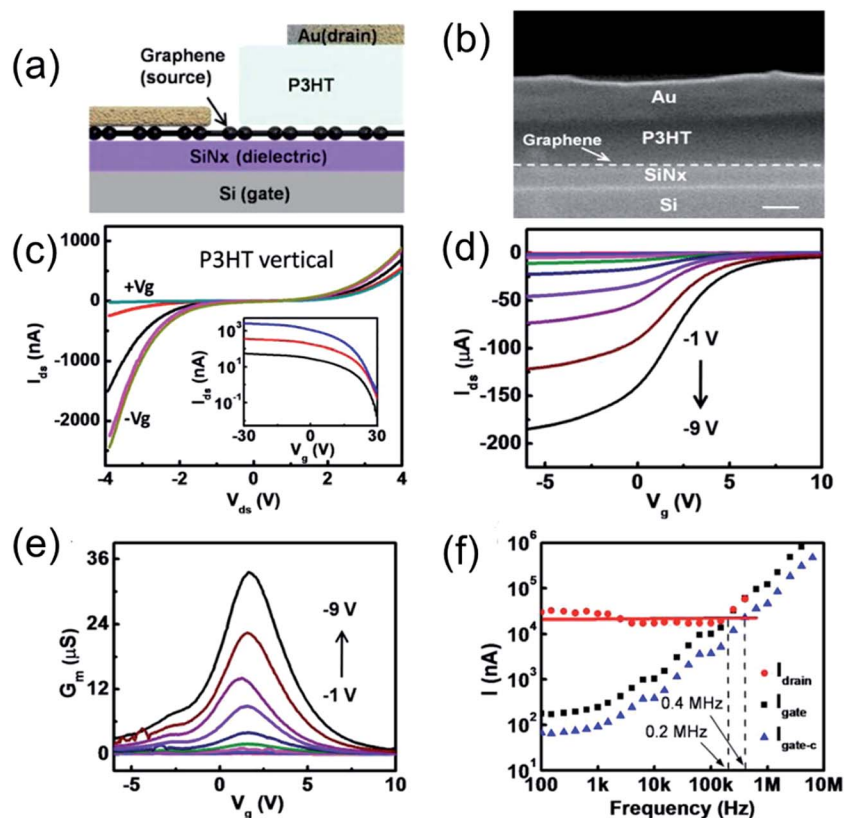


Fig. 9 (a) Schematic illustration of the cross-sectional view of the OVTFT device (b) cross-sectional SEM image of an OVTFT, clearly illustrating layers of the vertical stack. The scale bar is 100 nm. (c) I_{ds} - V_{ds} output characteristics of a graphene-P3HT-Au p-type OVTFTs at various gate voltages from -30 to $+30$ V (15 V steps). The transfer curve is semilog-plotted in the insets with various bias voltages where $V_{ds} = -1$ V (blue), -2 V (red), and -4 V (black). (d) Transfer characteristics of an OVTFT on glass at different bias voltages from -1 to -9 V (1 V steps). (e) Transconductance as a function of the gate voltage at different bias voltages. (f) Gate and drain AC current as a function of input frequency signal. The red dot is the measured drain current, and the black square is the measured gate current. The blue triangle is the calibrated gate current by considering the effective gate area and gate capacitance. Reprinted with permission from ref. 91. Copyright 2015 ACS.

semiconducting (P3HT, PBT7 and PCBM) thin film heterostructures through a general strategy of OVTFT fabrication with ultra-short channel length without using conventional high-resolution lithography processes (Fig. 9). Electrical studies show that those vertical transistors exhibit excellent switching behavior with an ON/OFF ratio greater than 10^3 and a high current density greater than 3.4 A cm^{-2} , and thus enable high cutoff frequency devices comparable to planar ultra-short channel organic transistors.

4. Conclusions and outlook

In this review, we have attempted to summarize recent development of flexible thin film transistors (TFT) based on graphene and graphene/semiconductor heterostructures according to the role of graphene which act as electrodes material as well as a channel layer in FET. Especially, we reviewed the progress of TFTs based on graphene/semiconductor (including inorganic and organic semiconductors) heterojunctions in which graphene act as electrodes materials in detail. It must be recognized that there are many caveats and challenges. For example, although the channel

material itself may be atomically thin, electric field lines can extend from the drain to the source through the underlying buried oxide, leading to drain-induced barrier lowering, or through the high- k gate dielectric, leading to so-called fringing-field-induced barrier lowering. On the other hand, there are still many challenges ahead in creating large-area and very flat ($<0.2 \text{ nm}$ surface roughness) 2D films, although graphene single crystals up to 5 cm in diameter have been grown on hydrogen-terminated germanium.⁹⁶ Certainly, graphene needs various technological issues to overcome, nevertheless it looks promising for flexible electronic applications, which are difficult to realize with conventional materials. In future, large-area integration of 2D materials, specifically graphene, with materials of other dimensionality is likely to have a sizable impact on semiconductor technologies. Furthermore, single-crystalline film quality and thickness uniformity with minimal cracks, voids, wrinkles, ripples and other contaminants are critical. Therefore, direct synthesis of high-quality 2D materials on insulating substrates should be a high priority. Overall, the vast integration possibilities presented by mixed-dimensional vdW heterostructures suggest considerable future growth potential for this field in both fundamental studies



and applied technologies. It is anticipated that further progress in 2D material growth, heterostructure formation and device fabrication shall lead to practical applications in future.

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