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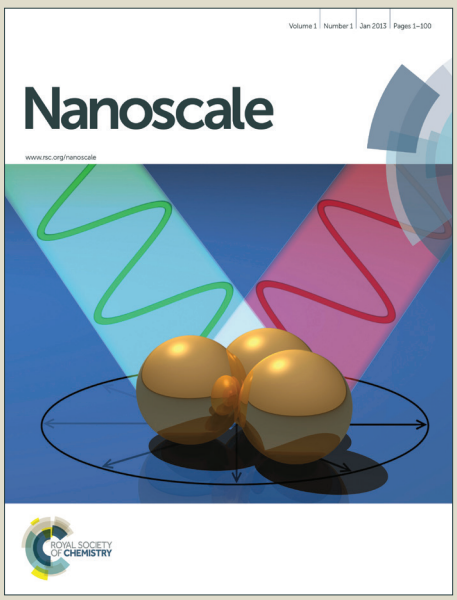

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Integrating Carbon Nanotubes to Silicon by means of Vertical Carbon Nanotube Field-effect Transistors

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Abstract

Single-walled carbon nanotubes have been integrated into silicon by means of vertical carbon nanotube field-effect transistors (CNTFETs). A unique feature for these devices is that silicon substrate and a metal contact are used as the source and drain for the vertical transistors, respectively. These CNTFETs show very different characteristics from those fabricated with two metal contacts. Surprisingly, the transfer characteristics of the vertical CNTFETs can be either ambipolar or unipolar (p-type or n-type) depending on the sign of the drain voltage. Furthermore, the p-type/n-type character of the devices is defined by the doping type of the silicon substrate used in the fabrication process. A semiclassical model is used to simulate the performance of these CNTFETs by taking the conductance change of the Si contact under gate voltage into consideration. The calculation results are well consistent with the experimental observation.

Keywords: Carbon nanotubes; Field effect transistor (FET); Semiclassical simulation; Single-walled carbon nanotubes; Electrical (electronic) properties.

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1. Introduction

Single-walled carbon nanotubes (SWCNTs), the perfect one-dimensional and mono-atomic layer material, have shown carrier mobility as high as 100000 cm^2/Vs,[1] and good compatibility with field effect transistor (FET) architecture and high-k insulators.[2] They are one of the most promising alternative materials for silicon (Si) in microelectronics as we reach the end of scaling roadmap.[3] The sub-2 nm diameter of the SWCNT can easily satisfy the body thickness requirement for a 5 nm node FET while it is unrealistic for Si technology as the mobility will be reduced by several folds due to the enhanced surface scattering and device variations. [4, 5] Recently developed CNTFETs with single SWCNT and sub-10 nm channel length have shown very impressive performance. [6] The switching behavior is comparable to the best Si devices, but the normalized current density, 2.41 mA/μm, shown at a low operating voltage of 0.5 V, is more than four time better than the best competing silicon devices.

Despite the promising progress in individual CNTFETs, some challenges remain for large scale transistor fabrication, including 100% separation of semiconducting SWCNTs (s-SWCNTs) from metallic SWCNTs, control of s-SWCNT chirality and diameter, precise assembly of SWCNTs into the transistor position. [7] From this point of view, there is still a long way to go for SWCNTs to replace Si, a mature technology that has been developed very successfully over the last four decades. Before this replacement comes true, the combination of Si technology and carbon nanotube seems a good approach to exploit the advantages of both Si and SWCNT. The combining of Si and graphene has produced an excellent graphene barrister.[8] In this study, we demonstrate the integration of SWCNTs and Si by means of vertical CNTFETs. In this structure,

the Si is used as one contact of the transistor while another metal contact is vertically stacked above the silicon. There is a dielectric layer between the top metal contact and the lower Si contact. SWCNTs are placed on the vertical side wall of the stack. This approach has some apparent advantages. First, it makes integration of Si and SWCNTs possible without changing the present Si technology. Moreover, it makes the fabrication of short channel CNTFETs easier because the channel length is exactly the thickness of the dielectric layer which can be precisely controlled. Channel lengths from 1μm to sub-10 nm can be realized without using those prohibitively expensive techniques, such as electron beam lithography. Furthermore, it could increase the integration density because these CNTFETs are developed vertically. It has been shown that vertical metal-oxide-semiconductor field effect transistors (MOSFETs) occupy smaller space than their planar counterparts. [9] This advantage is especially attractive for active-matrix organic light-emitting diode (AMOLED) drivers in display technology. The aperture ratio of the AMOLED pixel can be significantly increased by decreasing the transistor area.

The objective of this work is to assess the feasibility of integration of SWCNTs to Si by means of vertical CNTFETs. The experimental results confirm this approach. In addition, the performance of such CNTFETs is different from those with two metal contacts. The transfer characteristics of the CNTFETs depend on both of the sign of drain voltage and the Si type. The experimental results are well simulated using a semiclassical method.

2. Experimental

Figure1 schematically illustrates the configuration of the vertical CNTFETs. The fabrication procedure is as follows. First, Si wafers were cleaned using buffered oxide etch (BOE) to remove the thin natural oxide layer on Si surface. Then, silicon nitride (SiN_x) film with thickness of 600 nm was deposited on Si using plasma enhanced chemical vapor deposition (PECVD). SiH_4 (23 sccm), NH_3 (20 sccm) and N_2 (980 sccm) were used as reaction gases with deposition pressure of 850 mTorr. The forward power and substrate temperature were 20 W and 300 °C, respectively. After the SiN_x deposition, the metal contact composed of 20-nm Cr and 50-nm Au were fabricated using electron beam evaporation (Denton, base pressure 4×10^{-6} Torr) and lithography. The SiN_x outside the CNTFETs were etched using reactive ion etching (RIE). The CHF_3 flow, SF_6 flow and chamber pressure were 90 sccm, 10 sccm and 10mTorr, respectively, in the etch process. SWCNTs were placed on the side wall of the vertical stack by dropping SWCNT aqueous surfactant solution (Nanointegris, IsoNanotubes-S, semiconductor purity 99%) onto the Si wafer and evaporated the solution at 200 °C. To eliminate the surfactant contamination, the wafer was baked at 250 °C for 0.5 hr. Before the deposition of the gate dielectric layer, The SWCNTs beyond the transistor channels were etched using RIE to isolate the CNTFETs from each other. The power, pressure, oxygen flow and etch time were 150 W, 50 mTorr, 30 sccm and 1 min, respectively. The SWCNTs on the side wall of the vertical stack can be seen from the SEM image in the bottom right inset in Fig.1. They form carbon nanotube networks and bridge the top Cr/Au contact and bottom Si.

The gate dielectrics were of two layers of HfO_2. In the first step, 90 nm of HfO_2 was deposited by electron beam evaporation. This layer protected the SWCNTs from being etched from Ozone used in the subsequent deposition. After evaporation, the sample was transferred into the atomic layer deposition (ALD) chamber for the deposition of the second layer HfO_2 which was of high

quality and excellent step coverage for the trench like structure. The ALD HfO_2 (60 nm) was deposited at 200 °C using a commercial ALD system (Cambridge Nanotech, Savannach100). The precursor, Tetrakis(Dimethylamido)Hafnium and ozone were used in the deposition.

The gate electrode, 15 nm-Ti and 50 nm-Au, was subsequently deposited using electron beam evaporation and lithography. Finally, the source and drain contacts were exposed by etching the gate dielectric layer on top of the contacts using BOE. A SEM image of the typical transistor cross-section is shown in the bottom left inset in Fig.1.

3. Results and Discussions

First, the vertical CNTFETs have been fabricated on n-type Si (n-Si) wafer (doping level: $5.0 \times 10^{17}cm^{-3}$–$1.0 \times 10^{18}cm^{-3}$). The current variation from 8 samples is less than one order of magnitude. Figure 2 shows the typical characteristics of the CNTFETs. The metal contact and Si substrate are used as the drain and source of the CNTFETs, respectively. We can see that it presents ambipolar characteristics (in Fig.2a) if a large positive drain to source voltage, $V_d \geq 0.5$ V, is applied to the metal contact (Cr/Au). The current, I_d, decreases first with increasing the gate voltage, V_G, from -15 V and reaches a minimum point. Then, it increases with increasing the gate voltage to 15 V. This indicates the Fermi level of the contact lies approximately in the middle of the SWCNT energy band gap. [10] As a result, electrons and holes contribute to n-branch current at positive V_G and p-branch current at negative V_G, respectively. The minimum points corresponding to different V_d shift right side with increasing V_d. The reason is given later.

The p-branch current is slightly larger than n-branch current for V_d = 1 V. As V_d decreases, the p-branch current gradually becomes lower than the n-branch current. The ambipolar characteristics of the CNTFETs completely turn to n-type characteristics at negative V_d, as shown in Fig.2b. It can be seen clearly that the n-branch current is more than 3 orders of magnitude larger than the p-branch current. These phenomena have not been found in the CNTFETs fabricated with two identical metal contacts, which have presented the same characteristics at both positive and negative V_d, as shown in the Supplementary Information. The explanation can be found in the simulation paragraph.

The mobility of the vertical CNTFETs is calculated using

$$\mu = \frac{dI_d}{dV_g} \times \frac{L}{C \times W \times V_d} \quad (1)$$

where L and W are the channel length and width, respectively. C is the capacitance per unit area between the gate and the nanotube network. To take into consideration of the electrostatic coupling between carbon nanotubes, the capacitance is expressed as[11]

$$C = \left\{ \frac{1}{2\pi\varepsilon_{ox}\varepsilon_0} \ln\left[\frac{2\Lambda_0}{d} \frac{\sinh(2\pi t_{ox}/\Lambda_0)}{\pi} + C_Q^{-1} \right] \right\}^{-1} \Lambda_0^{-1} \quad (2)$$

where t_{ox}, Λ_0^{-1}, and C_Q are gate dielectric thickness, carbon nanotube density and quantum capacitance, respectively. The transconductance of the CNTFETs is in the range of 0.9~2.5 μS. Using L = 600 nm, W = 2 μm, $C_Q = 4\times10^{-10}$ F/m, Λ_0^{-1} = 5 tubes/μm, d = 1.4 nm, t_{ox} = 150 nm and

ε_{ox} = 14 for mixed HfO_2, we calculate that the mobility is in the range of 11~32 $cm^2/V{\cdot}s$. This result is comparable to the values reported by other group,[12, 13] and is higher than that obtained from our planar CNTFETs (in Supplementary Information) which were fabricated using exactly the same SWCNTs. The possible reason is that some SWCNTs can bridge the source and drain directly in the vertical CNTFETs due to the short channel. As a result, the channel resistance caused by contact between SWCNTs in vertical CNTFETs is much less than that in the long-channel planar CNTFETs, leading to a higher mobility for vertical CNTFETs. The mobility can be further improved by increasing the SWCNT density, [14] decreasing the oxide thickness and reducing the contact resistance by using an appropriate metal. [15]

In addition of using n-Si wafer, we also fabricated some vertical CNTFETs using p-type Si (p-Si) wafer (doping level: $5.0 \times 10^{17}cm^{-3}$–$1.0 \times 10^{18}cm^{-3}$). These CNTFETs also exhibit ambipolar characteristics as shown in Fig.3a, but at negative V_d, in contrast to those CNTFETs with n-Si. The ambipolar characteristics are changed to p-type characteristics (in Fig.3b) instead of n-type ones (in Fig.2b) for the CNTFETs with n-Si after reversing the sign of V_d. The metal contact and Si substrate are similarly used as the drain and source, respectively, in the measurement.

In order to understand the experimental observations, we simulate the performance of these vertical CNTFETs using a semiclassical method. [16-19] Since the gate overlapped part of the Si contact in experiment and the conductance of this part was also modified by the gate voltage, we propose that the channel is composed of a SWCNT and part of Si. Two metal contacts are used as source and drain of the CNTFET in the calculation. For short channel CNTFETs, the contact

resistance plays a more important role than the channel resistance in the transistor performance.[4] We therefore suppose ballistic transport in the channel for the simplicity of the calculation. The neglect of channel resistance can cause the simulation current is somewhat higher than that of actual transistors. The current is given by the Landauer-Büttiker formula.

$$I = \frac{4e}{h}\int [F(E) - F(E + eV_d)]T(E)dE \quad , \tag{3}$$

where V_d is the drain voltage, $F(E)$ is the Fermi function and T(E) is the energy-dependent transmission through the SB between the SWCNT/Si and electrodes. T(E) can be estimated using the Wentzel-Kramers-Brillouin (WKB) approximation

$$T(E) = \exp\left[-2\int_{z_1}^{z_2} k(z)dz\right] , \tag{4}$$

with the wave number

$$k(z) = \frac{2}{3aV_0}\left\{\left(\frac{E_g}{2}\right)^2 - \left[E + eV(z)\right]^2\right\}^{1/2} , \tag{5}$$

where a = 0.144 nm, E_g = 0.6 eV, and V_0 = 2.5 eV are the C-C bond length, the SWCNT band gap and the tight-binding parameter, respectively. V(z) is the electrostatic potential along the channel and is obtained by numerically solving the Laplace equation. The integration is performed between the two classical turning points, z_1 and z_2.[16] The temperature considered here is 300 K. The Fermi level, E_F, of the source and drain contacts is assumed at the middle of the SWCNT band gap. It locates 0.3 eV and 0.8 eV below the conduction band of n-Si and p-Si, respectively, for a Si band gap of 1.1 eV.

The calculated transfer characteristics of the CNTFET with n-Si are shown in Fig.4. We can see that the CNTFET shows ambipolar characteristics at large positive V_d (in Fig.4a), and n-type characteristics at negative V_d (in Fig.4b), being well consistent with the experimental results. These characteristics can be understood based on the energy band diagrams of the channel. First, let's consider the band change and the transfer characteristics at a large positive bias ($V_d \geq 0.5$ V). If a positive V_G is simultaneously applied, the center of the channel band moves downward relative to that at $V_G = 0$ V, the Schottky barrier (SB) between source and Si for electron at the source becomes thinner with increasing V_G as shown in Fig.5a. Electrons from the source can tunnel through this SB into the channel and reach the drain to form electron current. At the drain, the SWCNT band bends downwards at $V_d > 0$ V, the hole injection from drain is possible, but the injected holes are blocked by the large forbidden band of Si at the source. Therefore, the electron current generated from the source plays a critical role for the n-branch current at $V_d > 0$ V and $V_G > 0$ V. At negative V_G, the center band of the channel shifts upwards in Fig.5b, blocking the above mentioned electron current. However, on the one hand, the upshift of the center band results in a sufficiently thin hole SB at the source, making holes injected from drain tunneling through it and reaching the source possible. On the other hand, the downward bending of the SWCNT band at the drain due to large positive V_d cause the sharp point of the hole SB at the drain (point A in Fig.5b) is lower than that of the SB at the source (point B in Fig.5b), the holes can reach the source without energy barrier. Therefore, the hole current from drain contributes to the p-branch current of the ambipolar characteristics while the electron current is suppressed at $V_G < 0$ V. Since the band energy between the Fermi level and the conduction band of n-Si is 0.3eV which is equal to that between the Fermi level and the valence band of the SWCNT, the

electron current from the source at positive V_G is comparable to the hole current from the drain at the corresponding negative V_G. As a result, the n-branch current is in the same order of magnitude as the p-branch current, leading to the ambipolar characteristics. The n-branch current and p-branch current increase monotonically with V_G and V_d - V_G, respectively. [10] Therefore, the minimum current happens at V_G = ½ V_d, and it shifts to right side with the increasing of V_d, being consistent with the experimental observation in Fig.2. If V_d is not large enough, say V_d = 0.25 V, the SB for holes at the drain is higher than the SB at the source, both hole energy and transmission probability are greatly reduced and the hole current is much less than that at higher positive V_d. Consequently, the CNTFET presents n-type characteristics at small positive V_d, being in agreement with the experimental result as shown in Fig.2a.

We now turn to the impact of the negative V_d at which the SWCNT band at the drain bends upwards. At V_G > 0 V, the center of the channel band moves downwards as shown in Fig.6a. The electron SB at the drain is thin enough for electrons tunneling through it and being collected by the source, contributing to n-branch current. As V_G increases, the channel band shift lower and the SB becomes more transparent, the electron current from the drain increases with increasing V_G. In contrast, the hole transport from source to drain is blocked by the large forbidden band of n-Si. The thermionic emission of holes over the valence band is in the order of 1×10^{-17} A, much less than the electron current from the drain. Therefore, the electron injection from drain to source dominates the n-branch current at V_G > 0 V. For V_G < 0 V, the center band of the channel moves upwards as shown in Fig.6b, building large barrier for electron transport from drain to source. The electron current, therefore, is much less than that at V_G > 0 V. At a smaller V_G, for example, V_G = -1 V, the electron current is mainly from thermionic emission of electrons over

the barrier. Since the electron current is small, the total current at this situation depends, to a large extent, on the hole transport from source to drain. However, the hole current is also negligible although the hole SB between the source and n-Si becomes thinner due to the upward movement of the center band. This is because the density of holes at energies around the sharp SB is very small due to the large forbidden band of n-Si, or the large energy distance from the sharp SB point to the Fermi level of the n-Si. The calculated hole current from source to drain is less than the electron current from thermionic emission at drain. As a result, the total current at V_G = -1 V is five orders of magnitude less than the current at V_G = 1 V, leading to the n-type characteristics of the CNTFETs at V_d < 0 V. This calculation results explains the experimental observation in Fig2b.

In the case of p-type Si being used in the simulation, the calculated results exhibit ambipolar and p-type characteristics at V_d < 0 V and V_d > 0 V, respectively, as shown in Fig.7. They are well in agreement with the experimental results shown in Fig.3. The reason for the ambipolar characteristics at V_d < 0 V is that both hole tunneling (p-branch current) from the source to drain at V_G < 0 V and electron tunneling (n-branch current) from drain to source at V_G > 0 V are possible. In addition of this, their corresponding SBs have the similar height and width, leading to comparable n-branch current and p-branch current. On the contrary, there is only hole injection (p-branch current) from drain to source at V_G < 0 V and V_d > 0 V. The electron transport from source to drain at V_G > 0 V and V_d > 0 V is prohibited by the large band gap of p-Si. Consequently, the CNTFET exhibits p-type characteristics at V_d > 0 V.

4. Conclusions

We have developed vertical CNTFETs on both p-Si and n-Si. The Si substrate and Cr/Au are used as the source and drain of the CNTFETs, respectively. The SWCNTs are placed on the sidewall of the vertical stack of Si/dielectrics/metal contact to bridge source and drain. The sub-1μm channel is defined by the thickness of the dielectric layer, offering a simple method to fabricate short channel CNTFETs. The CNTFETs show ambipolar characteristics at positive and negative V_d for n-Si and p-Si source contact, respectively. If the V_d sign is reversed, the CNTFETs presents n-type/p-type characteristics depending on the n-type /p-type Si used in the fabrication. By taking Si as part of the channel, a semiclassical method is used to simulate the CNTFETs. The calculation results are well consistent with the experimental observation. The different behaviors of these CNTFETs are understood through analyzing the band diagram of the Si and SWCNT in the channel. In addition of the unique transfer characteristics shown here, the development of vertical CNTFETs offers an approach for the integration of SWCNT and Si.

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Figure captions

Figure1. Schematic configuration of the vertical CNTFET. Bottom left inset: SEM image of the cross section of the transistors. Bottom right inset: SEM image of the SWCNTs on the side wall of the vertical stack of Si/Si_xN/metal contact (Cr/Au).

Figure 2. Transfer characteristics of the CNTFETs on n-Si at $V_d > 0$ V (a) and $V_d < 0$ V (b). The metal contact and n-Si substrate are used as the drain and source of the CNTFETs, respectively.

Figure 3. Transfer characteristics of the CNTFETs on p-Si at $V_d < 0$ V (a) and $V_d > 0$ V (b). The metal contact and p-Si substrate are used as the drain and source of the CNTFETs, respectively.

Figure 4. Calculated transfer characteristics of the CNTFETs on n-Si. (a) and (b) are for $V_d > 0$ V and $V_d < 0$ V, respectively. The n-branch current for $V_d = 0.25$ V overlapped with that for $V_d =$ 1 V, 0.75V and 0.5V, respectively in (a).

Figure 5. Energy band diagrams of the CNTFETs at $V_d = 0.75$ V, $V_G = 0.5$ V (a) and $V_G =$-0.5 V (b). Blue and green lines are conduction band and valence band of the channel, respectively. E_{FS} and E_{FD} represents the Fermi level of the source and drain, respectively. The green and red arrows indicate the injection of electrons and holes from the contact, respectively.

Figure 6. Energy band diagrams of the CNTFETs at $V_d =$ -0.75 V, $V_G = 0.5$ V (a) and $V_G =$ -0.8 V (b). Blue and green lines are conduction band and valence band of the channel, respectively. E_{FS} and E_{FD} represents the Fermi level of the source and drain, respectively. The green and red arrows indicate the injection of electrons and holes from the contact, respectively.

Figure7. Calculated transfer characteristics of the CNTFETs on p-Si. The p-branch current for $V_d =$ -0.25 V overlaps with that for $V_d =$ -0.5 V, -0.75 V and -1 V, respectively.

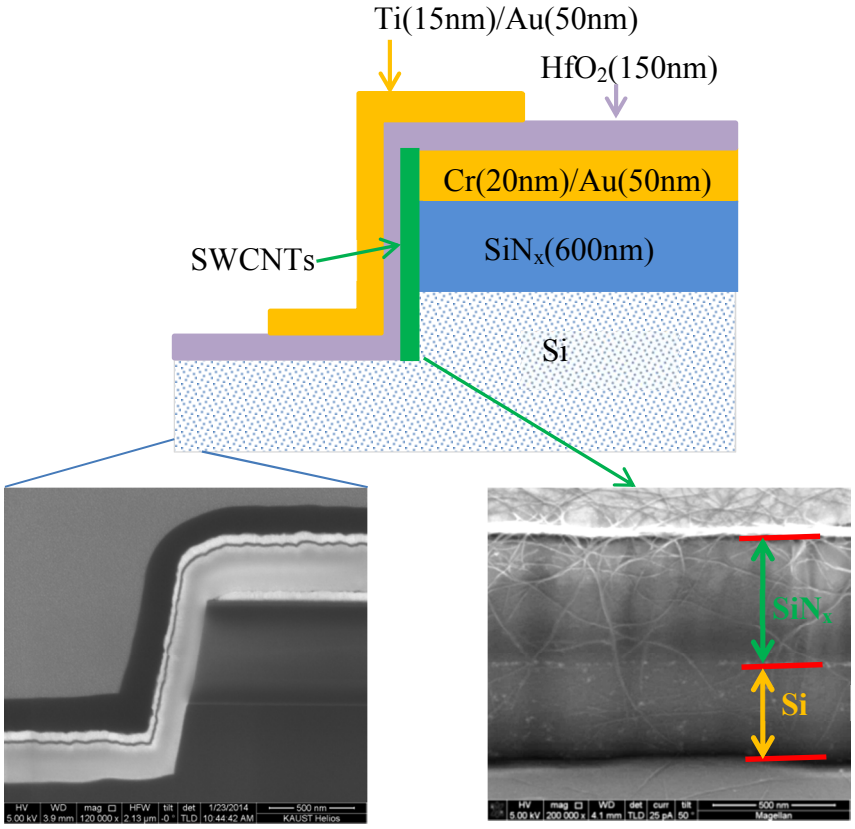


Figure 1

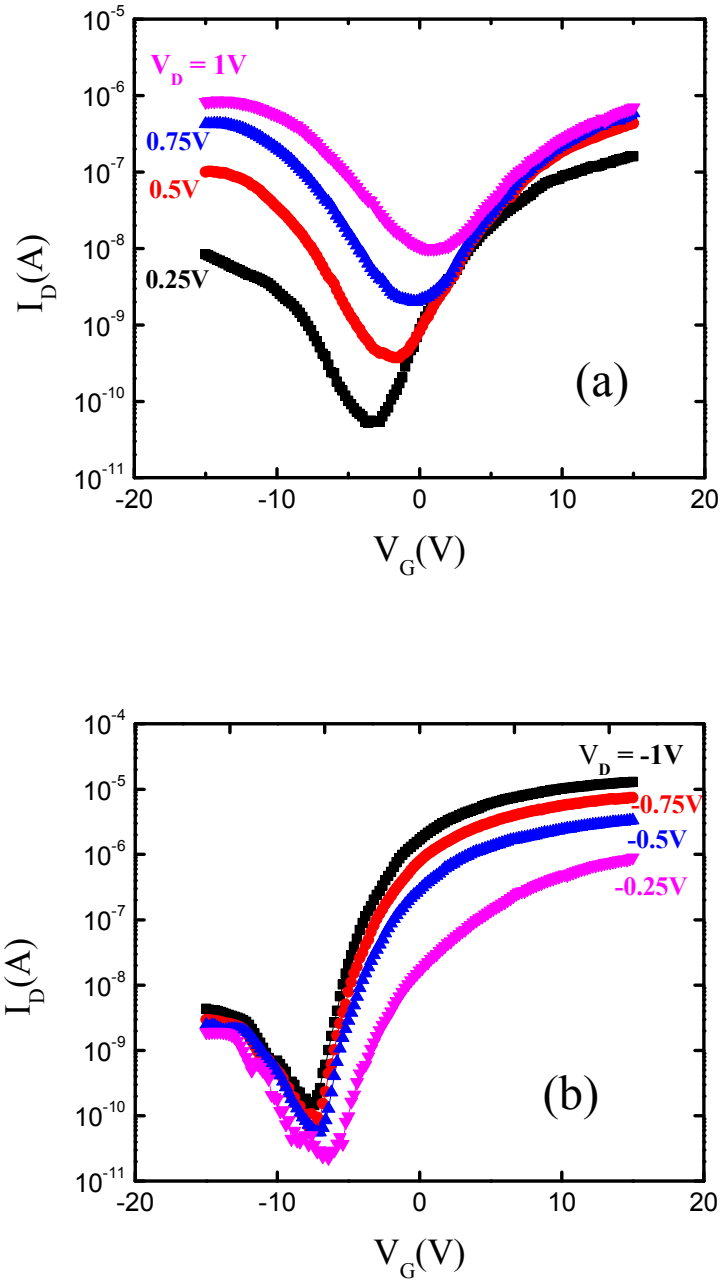
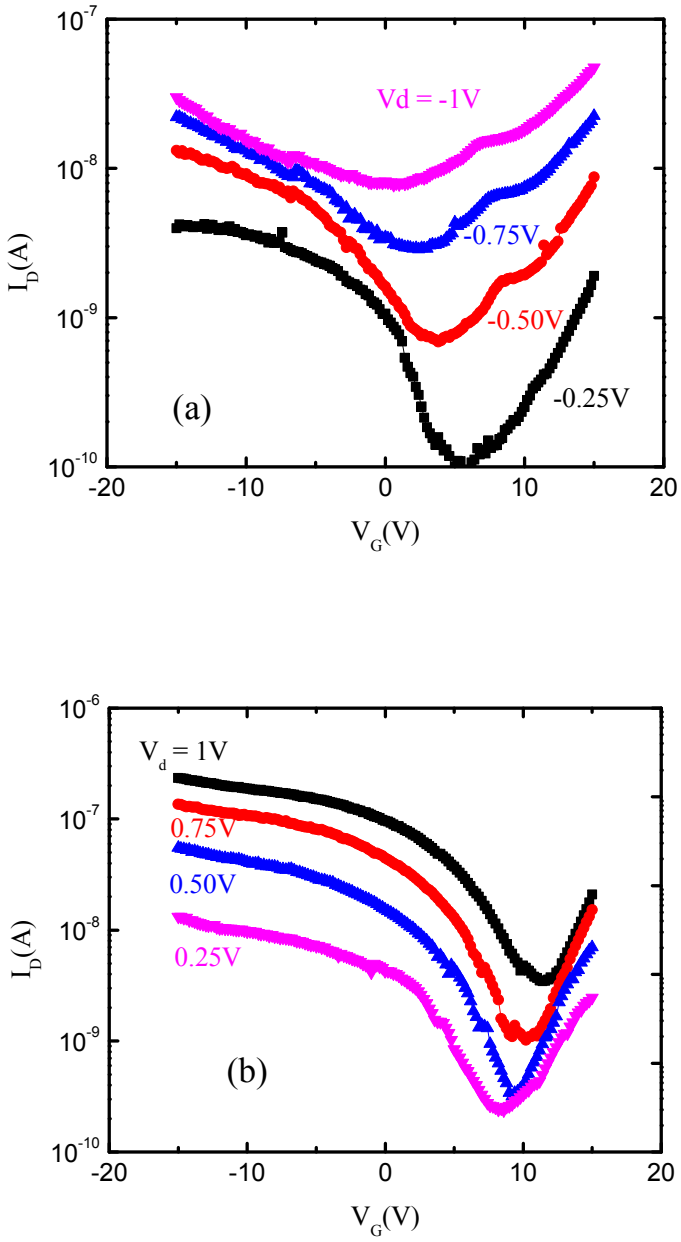


Figure 2



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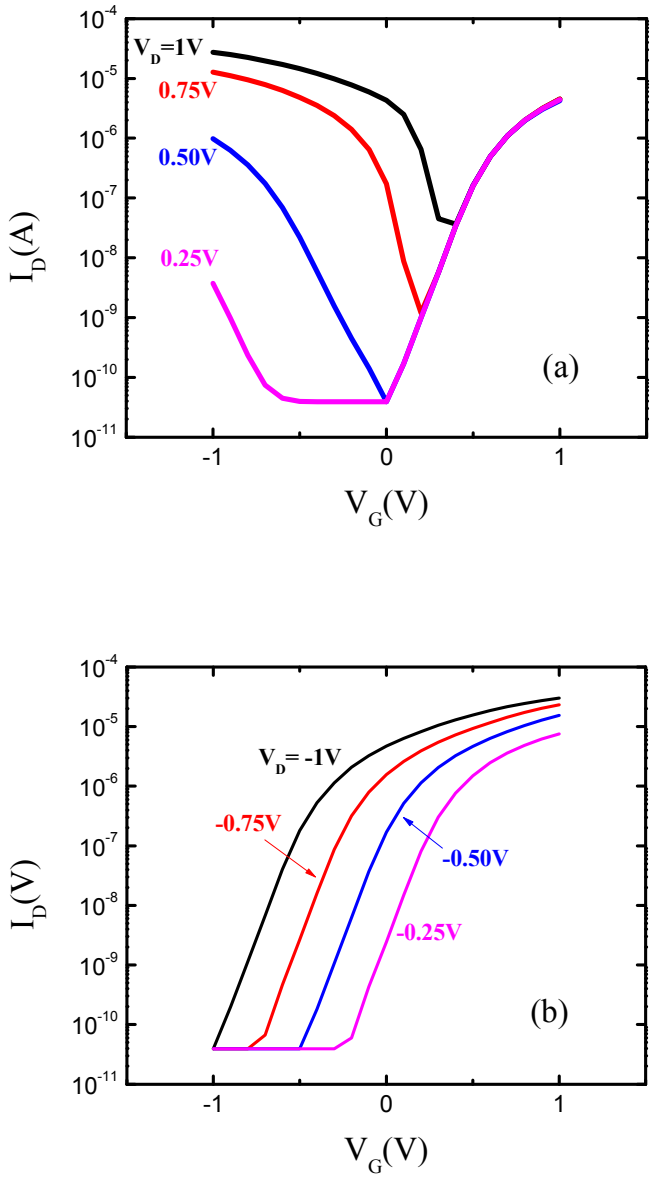

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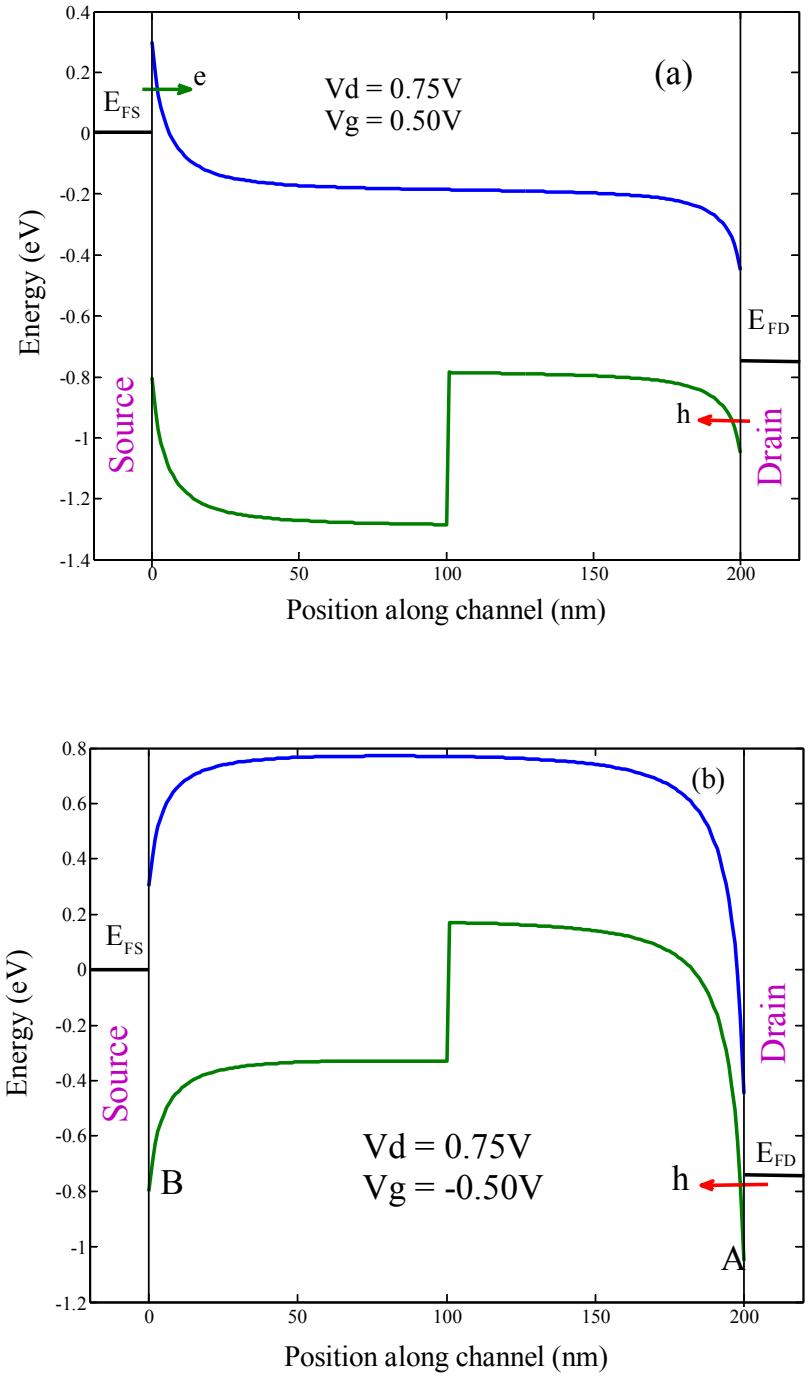

Figure 5

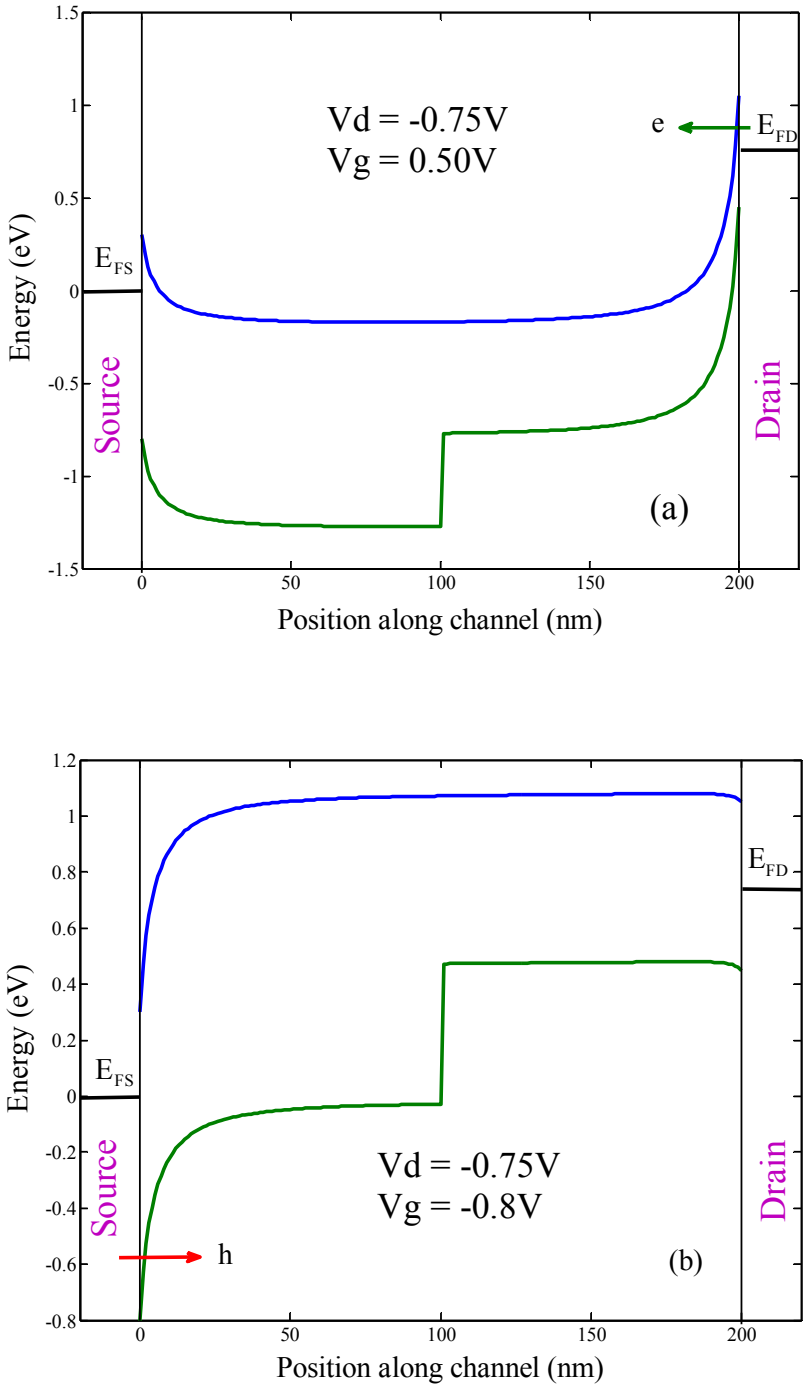

Figure 6

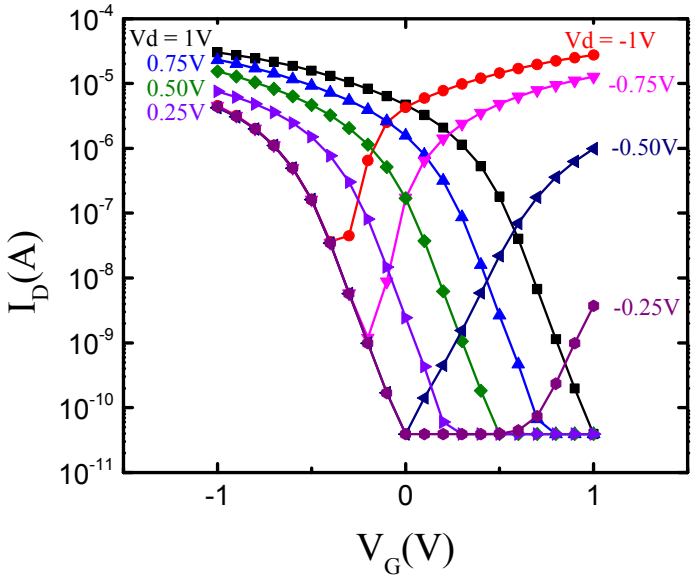

Figure 7