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Near room temperature multilevel resistive switching memory with thin film ionic liquid crystals†

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In this study, we demonstrate multilevel operation of nonvolatile resistive random-access memory (ReRAM) devices using thin films of an ionic liquid crystal (ILC), 1-dodecyl-3-methylimidazolium tetrafluoroborate ($[C_{12}mim][BF_4]$), as a resistive switching layer. The present ILC-based ReRAM devices exhibit bipolar resistive switching behavior between the high resistance state (HRS) and the low resistance state (LRS) in the SmA phase of $[C_{12}mim][BF_4]$ at near-room-temperature (30 °C) with an endurance of over 50 cycles and retention up to 2000 s. The observed resistive switching behavior of the device is caused by the formation and rupture of conductive filaments composed of trapped charges in the $[C_{12}mim][BF_4]$ thin film, where the current conduction at the LRS follows the space charge limited current mechanism. Furthermore, multilevel resistive switching is achieved by controlling the voltage sweep rate and the reset voltage during the voltage sweep with stable endurance and reversibility. These findings indicate that ILC-based ReRAM devices have potential for application not only as next-generation information storage devices but also as neuromorphic devices owing to their multilevel resistive switching function.

1. Introduction

There has been an increasing demand for new memory technologies,[1] as traditional information storage devices are facing development bottlenecks. Among many possible next-generation memory devices, the resistive random-access memory (ReRAM) devices have been extensively studied in recent years owing to their scalable structure, low power consumption, high storage density, and fast switching speed.[2–5] A typical ReRAM device has a simple two-terminal structure where the resistive switching layer is sandwiched between the top and bottom electrodes. In response to the voltage stimulation applied between the electrodes, this device can switch its resistance from a high state to a low state, and *vice versa*. The two processes correspond to the writing and erasing of information, respectively, thereby functioning as a memory device through reading these two states. In order to gain more insights into the operation mechanism and further improve device performance, various materials have been used to develop better resistive switching layers.[6–9] They include not only solid materials such as inorganic oxides,[10,11] organic compounds,[12,13] and organic–inorganic hybrid materials,[14,15] but also liquid materials such as ionic liquids (ILs), which are non-volatile electrolytes with high thermal and electrochemical stability.[16] However, the fluid characteristics of ILs necessitate a solid framework for the construction of ReRAM devices, such as the holes in an oxide solid layer of, for example, HfO_2[6] and bulk glass tubes,[9,17] which may restrict the practical use of such ReRAM devices because of possible difficulties in their integration and miniaturization. To overcome this issue associated with the fluid characteristics of ILs, we previously proposed a new ReRAM device with a vacuum-deposited thin film of an ionic liquid crystal (ILC), specifically 1-hexadecyl-3-methylimidazolium hexafluorophosphate ($[C_{16}mim][PF_6]$),[18] utilized as the switching layer.[19] The $[C_{16}mim][PF_6]$-based ReRAM exhibited nonvolatile bipolar resistive switching behavior at temperatures above 75 °C,[20,21] a temperature of the crystal–liquid–crystal transition of $[C_{16}mim][PF_6]$, where the $[C_{16}mim][PF_6]$ thin film exhibiting the smectic A (SmA) phase allows the switching operation driven at voltages as low as ~1 V. However, against its practical use, the $[C_{16}mim][PF_6]$-based ReRAM still has a drawback of being not operable in the crystal phase at room temperature (RT). Hence, among the candidates commercially available we attempted to find ILC materials more suitable for practical ILC-based devices that can operate at RT. As a result, 1-dodecyl-3-methylimidazolium tetrafluoroborate ($[C_{12}mim][BF_4]$) has been found to be a good candidate for the resistive switching layer which enables near-RT-operating ReRAM devices, because it

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exhibits the SmA phase within the temperature range of 22 to 48 °C.[22–25]

In conventional ReRAM devices, digital memory application has been realized with their high resistance state (HRS) and low resistance state (LRS) represented as "0" and "1", respectively. However, in recent years, there have been growing efforts to apply ReRAM devices in the development of neuromorphic computing devices,[26–30] which aim to mimic the information processing functions of the brain. In such ReRAM applications, the realization of multilevel memory operations is essential. Multilevel memory in this context offers the advantage of storing more than two data levels in a single device.[31] Micro- or nano-channel conduction devices using liquid electrolytes such as ionic liquids as well as conventional solid-state ReRAM devices have been demonstrated in realizing such multilevel memory functions.[32–35] However, as mentioned before, an encapsulating liquid requires a specific structure in the device, making its integration and miniaturization more difficult. Hence, exploring multilevel memory operation of ReRAM devices with ILCs, which can be fabricated as solid thin films and have properties similar to ILs, would potentially overcome the limitations of liquid electrolyte systems, and can be an important step toward achieving practical electrolyte-based multilevel memory.

Based on this background, we here fabricate ReRAM devices using $[C_{12}mim][BF_4]$ as the resistive switching layer, sandwiched between the bottom electrode of a hydrogen-terminated heavily-doped Si(100) substrate and the top electrode of Ag (Ag/$[C_{12}mim][BF_4]$/H:Si(100)). Typical *I–V* curves display bipolar switching behavior with good endurance when the ILC film is in the SmA phase at RT. Moreover, the device shows multilevel resistive switching which is achieved by controlling the voltage sweep rate and the reset voltage.

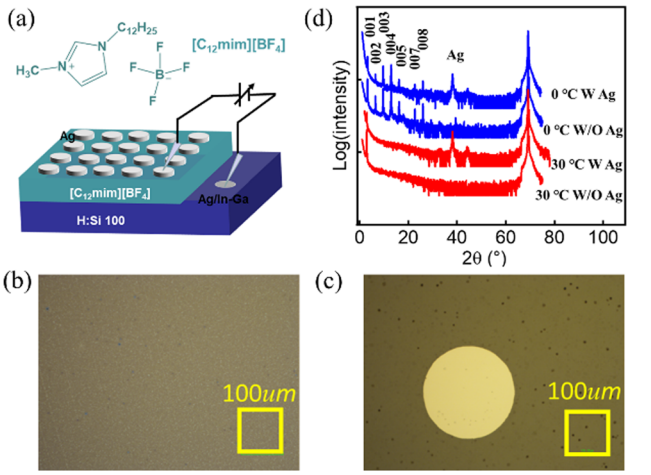

Fig. 1 (a) Molecular structure of $[C_{12}mim][BF_4]$ and the ReRAM device structure of Ag/$[C_{12}mim][BF_4]$/H:Si(100). Optical microscopy images observed at RT for $[C_{12}mim][BF_4]$ thin films (b) before and (c) after depositing Ag as top electrode pads. (d) Out-of-plane XRD patterns of the respective $[C_{12}mim][BF_4]$ thin films covered with and without a uniform Ag layer measured at 0 and 30 °C, respectively.

2. Experimental

2.1 Materials

$[C_{12}mim][BF_4]$ (>98%) was purchased from IoLiTec and used without any further purification. A heavily-doped n-type Si(100) wafer was cut into pieces with approximately 10 mm × 20 mm in size, which were used as the substrate. The substrate was ultrasonically cleaned with acetone, ethanol, and ultrapure water for 5 min each in that order, and then soaked in an SC-1 solution ($NH_3:H_2O_2 = 1:1$) at 75 °C for 5 min to remove organic and metallic particles, followed by rinsing with ultrapure water. Finally, the substrate was soaked in a HF buffer solution ($HF:NH_4F = 1:9$) for 10 min at RT, followed by rinsing with ultrapure water to obtain a hydrogen-terminated Si(100) (H:Si(100)) substrate.

2.2 Device fabrication

$[C_{12}mim][BF_4]$ film-based ReRAM devices were fabricated with a structure of Ag/$[C_{12}mim][BF_4]$/H:Si(100), using Ag and H:Si(100) working as the top and bottom electrodes, respectively (Fig. 1a). A $[C_{12}mim][BF_4]$ thin film with a thickness of ~100 nm was first deposited on a H:Si(100) substrate by a continuous-wave infrared (CW-IR) laser deposition technique under high vacuum.[36] To obtain a uniform $[C_{12}mim][BF_4]$ thin film without dewetting, the substrate temperature was kept at 0 °C during the deposition. After that, Ag top electrode pads with a diameter of 200 μm and a thickness of ~20 nm were deposited on the $[C_{12}mim][BF_4]$ thin film using a conventional thermal evaporation technique through a shadow mask. To minimize possible thermal damage of the $[C_{12}mim][BF_4]$ thin film caused by the Ag deposition, the substrate temperature was set below 0 °C during the Ag deposition.

2.3 Characterization

The phase behavior of $[C_{12}mim][BF_4]$ in a thin film device was studied by X-ray diffraction (XRD) (Bruker D8 Discover with a Cu Kα radiation source) using a custom-made chamber with a temperature-variable sample stage. A nitrogen gas (0.2 L min^{-1}) was flowed through the chamber during the XRD measurement. For electrical performance measurement of the Ag/$[C_{12}mim][BF_4]$/H:Si(100) devices, the H:Si(100) substrate surface was partially coated with In–Ga and Ag pastes to ensure the ohmic contact between the probe needle and the substrate electrode. Current–voltage (*I–V*) characteristics of the devices were measured using a vacuum probe station (~10 Pa) equipped with a variable temperature stage, using a source-measure unit (B2902A, Keysight). The voltage sweep for the *I–V* measurement was carried out in quasi-static sweep mode, in which the applied voltage was changed in a staircase manner at a stair step voltage of 0.01 V with a duration of 100 ms (which corresponds to the sweep rate of 0.1 V s^{-1}), except for the multilevel memory operation which was tested for different times. In the measurements, the positive voltage was defined as the voltage applied to the top electrode relative to the bottom electrode.

3. Results and discussion

3.1 Morphology and structure of $[C_{12}mim][BF_4]$ thin films

The morphology of a $[C_{12}mim][BF_4]$ thin film as-deposited on a H:Si(100) substrate showed a uniform and smooth surface in the optical microscope image, as shown in Fig. 1b. Even after deposition of Ag as the top electrode, the $[C_{12}mim][BF_4]$ thin film maintained a uniform morphology without any visible thermal damage (Fig. 1c). To investigate the effect of Ag electrodes capping the surface of thin film $[C_{12}mim][BF_4]$ on its phase change with temperature, XRD patterns of the respective thin films covered with and without a uniform Ag layer were compared for different measurement temperatures, as shown in Fig. 1d. First, the thin film without the Ag layer exhibited strong diffraction peaks at 0 °C. These peaks can be assigned to the 00*l* reflections corresponding to a layered structure with a layer spacing of 2.73 nm, which originate from the crystal phase (Cr I) or the low-temperature smectic (LtSm) phase of $[C_{12}mim][BF_4]$,[37,38] a supercooled Sm phase with a higher order of lamellar stacks. On the other hand, only one peak attributed to a larger layer spacing of 3.00 nm originating from the layered structure of the SmA phase[37,38] was observed at 30 °C. Next, we measured the XRD patterns of the sandwich sample of Ag/$[C_{12}mim][BF_4]$/H:Si(100), in which the Ag layer fully covered the $[C_{12}mim][BF_4]$ layer. The temperature dependent XRD patterns of the sandwich sample were almost identical to those of the sample without the Ag layer, as depicted in Fig. 1d, confirming that the impact of the Ag layer on the $[C_{12}mim][BF_4]$ underlayer was negligible.

3.2 Electrical properties of the $[C_{12}mim][BF_4]$-based device

Fig. 2a and b show typical *I*–*V* curves of an Ag/$[C_{12}mim][BF_4]$/H:Si(100) device measured with a voltage sweep between −3 V and +3 V and at 0 °C and 30 °C, respectively. When the $[C_{12}mim][BF_4]$ thin film was in the LtSm or CrI phase at 0 °C, as shown in Fig. 2a, the current increased slightly (from $\sim10^{-8}$ to $\sim10^{-7}$ A) in the positive voltage sweep (0 to +3 V) while it increased significantly (from $\sim10^{-8}$ to $\sim10^{-5}$ A) in the negative voltage sweep (0 to −3 V). The voltage sweep in either direction, however, showed no hysteresis in the current flow, that is, no memory behavior was observed in the *I*–*V* curves at 0 °C. In contrast, the $[C_{12}mim][BF_4]$ thin film in the SmA phase at 30 °C showed an obvious hysteresis (Fig. 2b). In the positive voltage sweep, the current increased slowly and initially stayed in the HRS. Then, there was an abrupt increase of current when the voltage reached a certain threshold voltage (approximately +1 V in this case), and the current reached the order of $\sim10^{-5}$ A and then became almost constant in the LRS, probably because the current was levelled off by a self-compliance current. This resistive switching behavior from the HRS (off state) to the LRS (on state) is a typical set process in a ReRAM device, and this threshold voltage is called the set voltage. The device stayed in the LRS throughout the subsequent reverse sweep from +3 V to 0 V. It should be noted that the observed self-compliance current phenomena are often reported in memory devices with barrier layers inserted.[39,40] In our case, despite no intentional use of a barrier layer in the device, it might be caused by a resistive oxide layer formed on the H:Si(100) substrate surface due to its possible incomplete hydrogen termination. In the negative voltage sweep, although the change in resistance was not as clear as in the positive voltage sweep, the current values when sweeping from −3 V to 0 V were all smaller than those when sweeping from 0 V to −3 V, suggesting a resistive switching from the LRS to the HRS at −3 V (reset process). The bipolar switching behavior observed at 30 °C clearly demonstrates that a near-RT-operating ReRAM device has become possible by using $[C_{12}mim][BF_4]$ as a resistive switching layer.

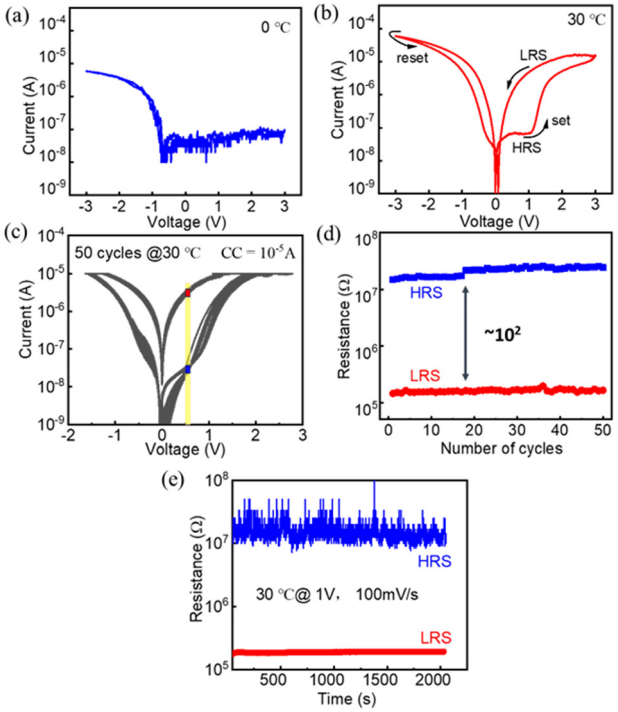

Fig. 2 Typical *I*–*V* curves of a Ag/$[C_{12}mim][BF_4]$/H:Si(100) device at (a) 0 °C and (b) 30 °C. (c) *I*–*V* curves in 50 consecutive voltage sweep cycles with a compliance current (CC) of 10^{-5}A at 30 °C. (d) Endurance characteristics of the device, where the resistance values in the HRS and LRS measured from (c) at 0.5 V (yellow line) are plotted, respectively, against the number of cycles. (e) Retention characteristics of the device, where the resistance values of the HRS and LRS measured at +1 V are plotted as a function of time.

The endurance property of the ReRAM at 30 °C was examined by 50 repeated voltage sweep cycles between −2 V and +2 V under a compliance current of 10^{-5} A, as shown in Fig. 2c. The resistance values measured at +0.5 V for the HRS (blue rectangle) and LRS (red rectangle) shown in Fig. 2c are plotted, respectively, against the number of cycles in Fig. 2d. The resistance values in the HRS and LRS remained nearly constant throughout the 50 cycles at $\sim2 \times 10^7$ Ω and $\sim2 \times 10^5$ Ω, respectively, with an on/off ratio of $\sim10^2$. Fig. 2e shows the retention characteristic of the device at 30 °C, where the resistance values for the HRS and LRS were obtained by applying a constant voltage of +1 V. The resistance values in the HRS and LRS remained nearly constant at 10^7–10^8 Ω and $\sim10^5$ Ω, respectively, with an on/off ratio of $\sim10^2$ maintained

over more than 2000 s. In addition, the device-to-device variation was confirmed to be acceptable from the basic electrical properties (*I*–*V* curves) measured for randomly selected 11 devices, as shown in Fig. S5 (ESI†).

3.3 Operation mechanism of the memory

To understand the switching mechanism of the present [C_{12}mim][BF_4]-based device, the set process was investigated with a careful analysis of the resistance in the LRS and HRS. Fig. 3a shows the resistance values in the LRS and HRS measured at +1 V plotted as a function of the diameter of the top electrode pad. The resistance in the LRS remained relatively constant at $\sim 5 \times 10^5$ Ω, regardless of the electrode pad size, with a small fluctuation. On the other hand, the resistance in the HRS showed an obvious decreasing trend from $\sim 1 \times 10^8$ Ω to $\sim 5 \times 10^6$ Ω as the diameter of the top electrode pad increases from 100 to 500 μm. These results indicate that the resistive switching behavior of the memory follows the conductive filament (CF) mechanism.[39,40] Under this mechanism, most of the current in the LRS flows through the CFs, and the current in the HRS flows through the total area of the resistive switching layer sandwiched between the electrodes.[39,40]

To understand the composition of the CFs, the respective I–V curves in the HRS and LRS were measured at different temperatures (10, 20, 30, and 35 °C) and shown in Fig. 3b and c, respectively. As the temperature increased, the current value in both the HRS and LRS increased (*i.e.*, a decrease in resistance), indicating that the CFs are not metallic.[41] As a non-metallic CF formation mechanism, a CF formation based on oxygen vacancies has been commonly proposed for oxide-based ReRAM devices.[42,43] However, considering that the materials constituting the device include no oxides, this mechanism could be excluded.

To gain insight into the conduction mechanism of the CFs in the present [C_{12}mim][BF_4]-based device, experimental *I*–*V* curves were replotted and fitted using possible theoretical conduction models. Fig. 3e and f show log*I*–log*V* curves under positive (set process) and negative (reset process) voltage sweeps at 30 °C, respectively. In the set process, the current under low voltages (black circle, below +0.3 V) in the HRS was well fitted by the Poole–Frenkel (PF) conduction model,[44,45] where the current–voltage relationship is described as $I \propto V\,exp(V^{0.5})$, *i.e.* a linear relationship between $\log(I/V)$ *vs.* $V^{0.5}$, as shown in the inset of Fig. 3e. When the voltage increased above +0.3 V, the log *I*–log *V* curve for the HRS could be divided into two regions (pink and blue circles) and fitted linearly with slopes of 2.38 (pink line) and 4.07 (blue line), respectively. Because these slope values are greater than 2, the trap charge limited current (TCLC)-based conduction mechanism[46,47] would be plausible to explain the conduction of the CFs in the [C_{12}mim][BF_4]-based device, and the increase of the slope indicates that the traps are gradually filled. Once the traps are completely filled, the device switches its resistance from the HRS to the LRS (purple circle) *via* the self-compliance current conduction (green circle). The LRS region was well fitted by a linear line with a slope of 1.43, indicating the conduction following the SCLC mechanism.[48,49] Based on this trap-assisted mechanism, the trap activation energy can be determined from the Arrhenius plot ($\log(J)$ *vs.* $1/T$).[50,51] From Fig. 3c, the activation energy (E_a) values were estimated to be around 0.4 eV, as shown in Fig. S6 (ESI†). This value is relatively larger than those of oxide-based devices in the literature, in which E_a values of $\sim$0.2 eV were reported.[50,51] The difference may be due to differences in the resistive switching layer materials. For the reset process (Fig. 3f), the trap-filled SCLC dominated the LRS with a slope of 1.49, followed by a resistive switching from the LRS to the HRS after applying a reset voltage (−3 V). During the reset process, the trapped charges are gradually released by the reverse electric field, with the eventual rupture of the CFs. The log *I*–log *V* curves in the HRS followed the TCLC mechanism with a slope of 2.92 (purple line) when the applied voltage was between −3 and −0.6 V. In the subsequent sweep from −0.6 to 0 V, the current conduction was explained by Schottky emission (SE)[52] with a linear relationship between log *I* and $V^{0.5}$, as shown in the inset of Fig. 3f. From these fitting analyses, the conduction and resistive switching mechanisms in the present device could be explained based on the formation and rupture of CFs composed of trapped charges[53] in the [C_{12}mim][BF_4] resistive switching layer.

As a result, these mechanisms are essentially the same as those of [C_{16}mim][PF_6]-based ReRAM devices that we reported previously.[19] In such electrolyte-based resistive switching

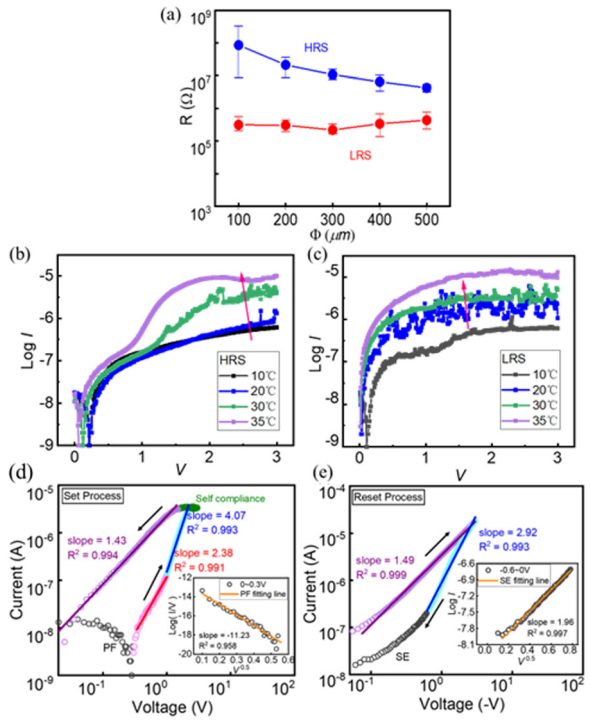

Fig. 3 (a) Resistance values in the LRS and HRS measured at +1 V depending on the diameter (*Φ*) of the top electrode pad, and the resistance value at each diameter is the average of those taken from ten devices. Respective *I*–*V* curves of the same device at different temperatures (10, 20, 30, and 35 °C) in the (b) HRS and (c) LRS. The fitting results of replotted *I*–*V* curves in (d) set and (e) reset processes (see details in the main text).

layers, the electric double layer (EDL) at the interface between the electrode and the ILC thin film is expected to play an important role in providing a sufficient electric field concentrated at the interfaces for charge injection from the electrodes to the ILC, contributing to lowering the required switching voltage.[19] In fact, the existence of EDL in the present [C_{12}mim][BF_4]-based device was also confirmed (Fig. S1, ESI†) with no thickness dependent capacitance in the SmA phase. The consistency and universality of the operation mechanism of the ILC-based memory devices, as schematically illustrated in Fig. S2 (ESI†), would highlight strategies for finding more suitable ILC materials and for optimizing the device properties in future developments.

3.4 Multilevel operation of the memory

Inspired by the multi-state of the IL-based two terminal devices,[30–33] we explored the possibility of multi-level operation of our [C_{12}mim][BF_4]-based memory. Fig. 4a shows the *I–V* curves of the memory for three consecutive reset processes after a one-time set process (positive voltage sweep up to +4 V) obtained upon increasing the voltage sweep range. The maximum applied voltages in the reset processes of the first, second and third sweep were −1, −2, and −4 V, respectively. Upon widening the voltage sweep range of the reset process, three levels of HRS (off state), marked as HRS1, HRS2 and HRS3 in Fig. 4a, were obtained with the resistance increasing in that order, indicating the multilevel operation.[54,55] This multilevel operation in the off state can be understood as a result of different reset voltages to be applied, and the higher the reset voltage, the more trapped charges will be released, with a greater degree of rupture of CFs in the [C_{12}mim][BF_4] thin film.[55] We also investigated the possibility of achieving different levels of conduction in the set process by varying the reset voltage (Fig. S3, ESI†). As a result, upon decreasing the reset voltage from −3 to −1 V, the conductivity increases in both the LRS and HRS of the set process. The modulation of this current level according to the reset voltage is unfortunately small in the present case and a further improvement will be required, but the results suggest that the [C_{12}mim][BF_4]-based device has a possible operation as a multilevel memory device.

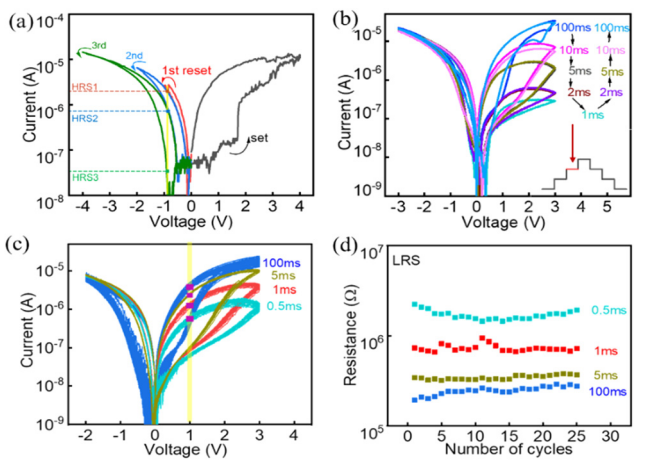

Fig. 4 (a) *I–V* curves of a device for three consecutive reset processes after the first set process up to +4 V with different reset stop voltages (1st, 2nd, and 3rd reset stop voltages are −1, −2, and −4 V, respectively). (b) *I–V* curves of the device for different durations in the quasi-static voltage sweep. The duration was changed in the following order: 100 → 10 → 5 → 2 → 1 → 2 → 5 → 10 → 100 ms as plotted in different colors. (c) 25 consecutive *I–V* curves for each duration. (d) Endurance characteristics for different durations, where the respective resistance values in the LRS measured at +1 V for different durations (red rectangles on the yellow band in Fig. 4c) were plotted against the number of cycles.

Furthermore, it has been reported that the multilevel operation of ReRAM devices can be achieved by controlling not only the set/reset voltage but also the duration in the voltage sweep.[56] In fact, the multilevel operation was clearly observed also in our memory as shown in the *I–V* curves measured at different durations in the voltage sweep (Fig. 4b). When the duration was set to 100 ms, the current values measured at +1 V in the LRS and HRS were 6.9×10^{-6} A and 4.0×10^{-7} A, respectively; on the other hand, a shorter duration time of, for example, 1 ms resulted in smaller current values, 1.8×10^{-7} A and 7.9×10^{-8} A, in the LRS and HRS, respectively. The duration dependence of the current readings at +1 V (Fig. S4, ESI†) shows that for both the LRS and HRS, the current decreases as the duration becomes shorter. This result suggests that the dynamics of charges being filled into and released out of the trap sates in the [C_{12}mim][BF_4] resistive switching layer is much affected by the exposure time to the applied voltage, in accordance with which the respective current levels in the LRS and HRS can be set to different values as a multilevel current response.[56,57] Furthermore, the *I–V* curve was reversible with respect to the change in the duration of each set–reset voltage sweep cycle, demonstrating the controllability and stability of such multilevel states.

In order to examine the endurance characteristics at each level, 25 consecutive *I–V* curves were measured for each duration (Fig. 4c). The respective resistance values in the LRS measured at +1 V for different durations (red rectangles on the yellow band in Fig. 4c) were plotted against the number of cycles, as shown in Fig. 4d. The resistance values remained almost constant at $\sim 1.6 \times 10^6$ Ω, $\sim 6.9 \times 10^5$ Ω, $\sim 3.3 \times 10^5$ Ω, and $\sim 2.5 \times 10^5$ Ω for the durations of 0.5 ms, 1 ms, 5 ms, and 100 ms, respectively, without any overlap with each other during the voltage sweep cycles, confirming a good endurance of the device for multilevel operation. The near-RT operation of [C_{12}mim][BF_4]-based ReRAM multi-level devices demonstrates great potential of ILCs as switching layers, these devices not being inferior to other previously reported devices (as shown in Table S1, ESI†), leading to synthesis of a wider choice of switching layer materials.

4. Conclusions

ILC-based ReRAM devices with a structure of Ag/[C_{12}mim][BF_4]/H:Si(100) were fabricated and their memory operation at near-RT (30 °C) was demonstrated. A resistive switching between the HRS and the LRS was observed when the [C_{12}mim][BF_4] thin

film was in the SmA phase, but not when it was in the LtSm or crystal state. The electrode area dependence of the current values in the HRS and LRS concluded that the formation and rupture of CFs in the [C_{12}mim][BF_4] thin film was the most plausible origin of the resistive switching behavior. Further analyses through different conduction model fittings to the *I–V* curves of the devices suggested that the CFs are composed of trapped charges and the LRS conduction followed the SCLC mechanism. In addition, the multilevel operation of the devices was confirmed, where the different resistance values in the HRS and LRS could be set by controlling the reset voltage and the duration of the voltage sweep, and each resistance state was found to have good endurance and retention characteristics. The present [C_{12}mim][BF_4]-based ReRAM devices are not only more practical because they can be operated at near-RT but also more advanced because of their multilevel operation, than the [C_{16}mim][PF_6]-based devices we previously reported. These results highlight the significant potential of ILCs as resistive switching layers for ReRAM devices, promising next-generation information storage and neuromorphic devices.

Author contributions

S. M., Y. M., and K. K. directed this research; S. M. and Y. M. polished the manuscript; Z. W. performed the experiments and wrote the draft. All the authors contributed to the preparation of this manuscript.

Conflicts of interest

There are no conflicts to declare.

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