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Gate-controlled rectification and broadband photodetection in a P–N diode based on TMDC heterostructures†

Ehsan Elahi, [ID] ‡*[a] Sobia Nisar,‡[bc] Muhammad Rabeel,[bc] Malik Abdul Rehman,[d] Mohamed Ouladsamne,[e] Ahmad Irfan,[f] Muhammad Abubakr,[bg] Jamal Aziz,[h] Muhammad Asim[a] and Ghulam Dastgeer [ID] *[a]

van der Waals (vdW) heterostructures in two dimensions have electrical and optoelectronic characteristics that make them a suitable platform for the creation of sophisticated nanoscale electronic devices. Outstanding p–n heterojunctions made of two-dimensional atomic layers are essential for the realization of superior integrated optoelectronics. This article shows how WSe_2 and SnS_2 layers are stacked by vdW heterostructures to build a p–n junction diode over Si/SiO_2 substrates; Raman mapping confirms the heterostructure even further. The WSe_2/SnS_2 vdW heterostructure's electrical attributes show ultra-low dark currents because of the junction's depletion area and robust direct current passage when lit. An energy band diagram is also used to study and describe the charge transport process. When the back-gate voltage is swept effectively, 2.9×10^4 is the rectification ratio (RR). The photovoltaic characteristics of the WSe_2/SnS_2 heterostructure have been studied under irradiation of light with different wavelengths (λ). When 220 nm light is applied to the WSe_2/SnS_2 vdW heterostructure, a change in the photocurrent of 65 nA is observed. Under light irradiation of deep ultraviolet (DUV) light at $\lambda = 220$ nm and $V_{ds} = 0.5$ V, the device revealed a responsivity (R) of 1.31×10^5 m AW^{-1}, with a substantial EQE of 7.3×10^4 (%) and a detectivity (D^*) of around 3.13×10^{10} Jones. The creation of these superior p–n junctions opens the door for the production of logical and effective optoelectronic devices.

[a] *Department of Physics & Astronomy, Sejong University, Seoul, 05006, South Korea.*
E-mail: Ehsanelahi@sju.ac.kr, gdastgeer@sejong.ac.kr

[b] *Department of Electrical Engineering, Sejong University, 209 Neungdong-ro, Gwangjin-gu, Seoul, 05006, South Korea*

[c] *Department of Convergence Engineering for Intelligent Drone, Sejong University, Seoul, 05006, South Korea*

[d] *Department of Chemical Engineering, New Uzbekistan University, Tashkent, 100007, Uzbekistan*

[e] *Department of Chemistry, College of Science, King Saud University, Riyadh, 11451, Saudi Arabia*

[f] *Department of Chemistry, College of Science, King Khalid University, Abha 61413, P.O. Box 9004, Saudi Arabia*

[g] *Graduate School of Optical Engineering, Sejong University, Seoul, 05006, South Korea*

[h] *School of Electrical, Information and Media Engineering, Bergische Universität Wuppertal, Lise-Meitner-Straße 13, Wuppertal 42119, Germany*

† Electronic supplementary information (ESI) available. The atomic force microscopy profile details of the individual flakes, Raman spectroscopy of each material, a process that shows the detailed calculation of ideality factor, and the rise and decay times for the photocurrent at $V_{ds} = 0.5$ V. See DOI: https://doi.org/10.1039/d3ma00786c

‡ Ehsan Elahi, and Sobia Nisar shared the 1st authorship equally.

1. Introduction

van der Waals (vdW) heterostructures based on atomically thin 2D materials have ushered in a new era in next-generation electronics and optoelectronics. This is a result of the ultrathin morphological features and the unique energy band alignments.[1–7] As opposed to typical semiconductor heterojunctions, these vdW heterostructures enable the development of configurations without the restriction of atomic lattice match and have high-quality integrations since there are no dangling bonds at the interfaces.[8,9] These ultrathin vdW nanostructures have demonstrated potential performance for light-emitting diodes (LEDs),[10] field effect transistors (FETs),[11,12] logic circuits,[13] photodetectors,[14–16] flexible devices,[17] and bipolar junction transistors.[5] In particular, 2D transition metal dichalcogenides (TMDCs)[18–21] are composed of an ordered stacking of building blocks and have a high carrier mobility[22,23] and numerous spin characteristics.[24–27] The most prevalent and essential p–n junctions are essential parts of optoelectronic and semiconductor devices. Since the development of atomically thin vdW 2D materials, a multitude of heterostructure-based p–n junctions have been created.[3,28] However, the majority of prior research used extra procedures that

produced p-type TMDCs, such as chemical doping, special metal contact, and electrical gating methods for developing p–n junctions, which have challenging and disruptive factors for vdW p–n junction practical applications.[29,30] Stacking individual layers of different 2D materials in a vdW heterostructure allows for the customization of energy band alignment and creates atomically sharp surfaces. This presents numerous opportunities for fundamental research into novel electrical and optical properties. As a result, most of the current investigations in the field of 2D TMDCs have been on TMDCs/TMDCs or TMDCs/graphene heterostructures.[3,31] Various TMDC-based heterostructures with diode rectification and photovoltaic properties have previously been described, including p-MoS_2/n-MoS_2,[32] $ReSe_2$/ReS_2,[33] and MoS_2/BP.[28] However, WSe_2/MoS_2 heterojunctions also exhibit a gate-tunable photovoltaic response,[3,34] and photovoltaic photodetectors utilizing $MoTe_2$/MoS_2 vdW heterojunctions are also revealed.[35,36] Due to the inadequate photocurrent flow without an external bias impact, these mentioned photovoltaic devices still have a poor response (< 0.5 A W^{-1}). To enhance the functionality of photovoltaic photodetectors based on TMDCs for upcoming nanoscale optoelectronic devices, further work is required.

Tin disulfide (SnS_2), a 2D material with an unusual band structure that is a IV–VI semiconductor with each layer of Sn atoms sandwiched between two layers of S atoms, interacts with other layers *via* vdW interactions. SnS_2, a significant n-type layered semiconductor, has garnered considerable interest due to its affordability, abundance on earth, non-toxicity, and environmental sustainability.[37] SnS_2 is intensively investigated in its bulk form, primarily for photovoltaics.[38] SnS_2 is an intriguing 2D TMDC because of its high carrier mobility[39,40] and potent excitonic effect (0.9 eV binding energy for a single layer).[41] 2D nanostructures combining p-type WSe_2 and n-type SnS_2 have recently attracted a great deal of attention. Zhang et al. showed the growth of a few layers of WSe_2 on randomly oriented SnS_2 microplates.[42]

In this study, we present the successful fabrication of WSe_2/SnS_2 van der Waals p–n junctions on a Si/SiO_2 substrate using the mechanical exfoliation technique. The two-dimensional nature of WSe_2 and SnS_2 allowed for a high-quality van der Waals heterostructure to be obtained, resulting in a p–n junction with an atomically sharp junction. The electrical characteristics of the WSe_2/SnS_2 vdW heterostructure are studied at various back-gate voltages varying from −60 to +60 V. The WSe_2/SnS_2 van der Waals heterostructure exhibited a suitable rectification ratio (RR) of 2.9×10^4, which indicates a reliable switching behavior. Additionally, the devices displayed a low leakage current and a fast photoresponse, making them well-suited for optoelectronic applications. The photoresponse of the devices was studied under illumination with various wavelengths of light. The measured photocurrent (I_{ph}) change was approximately 65 nA, revealing the excellent sensitivity of the fabricated p–n junction to the incident light (DUV). Furthermore, the device indicated a responsivity (R) of 1.31×10^5 mA W^{-1} with a significant external quantum efficiency (EQE) of 7.3×10^4 (%) and a detectivity (D^*) of about 3.13×10^{10} Jones. This value suggests that the fabricated devices are capable of converting a high percentage of incident photons

into electrical currents, making them ideal for use in energy-harvesting applications. The excellent photoresponse of the WSe_2/SnS_2 p–n junction under DUV light could be attributed to the efficient light absorption, built-in electric field, and high carrier mobility and the clean interface of the materials. The development of these van der Waals heterostructures represents a significant step forward in the design of high-performance integrated optoelectronic systems and products.

2. Device fabrication

A conventional dry transfer technique was adopted to build the WSe_2/SnS_2 vdW heterojunction device. Thin flakes of SnS_2 were initially exfoliated from the bulk (HQ graphene company) using scotch tape and then transferred onto a Si/SiO_2 substrate. Then, a few layers of WSe_2 were exfoliated onto PDMS and relocated onto a thin film of SnS_2 using an aligned transfer system under an optical microscope. The electrode was designed by the electron-beam lithography technique (EBL/SEM), and Cr/Au (5/60 nm) metal electrodes were deposited using a thermal evaporation system to fabricate the device for measurements. An optical microscope was used to examine the morphology of the vdW heterostructure based on WSe_2/SnS_2. An atomic force microscope was used to measure the thickness. Electrical measurements were performed using a Keithley system in a high vacuum environment at room temperature.

2.1. Results and discussion

The graphic illustration of the device based on the heterostructure WSe_2–SnS_2 p–n diode is demonstrated in Fig. 1(a). Fig. 1(b) shows the optical representation of the device-based WSe_2/SnS_2 vdW heterostructure with metal electrodes placed on the flakes. Fig. 1(c) shows the SEM image of the device. Fig. 1(d) and (e) points to the atomic force microscopy (AFM) image and profile height of the heterojunction WSe_2–SnS_2 of the p–n device. The thickness of the heterostructure WSe_2–SnS_2 is ≈ 12 nm. The individual thickness and AFM images of WSe_2 and SnS_2 flakes are illustrated in Fig. S1(a) and (b), ESI.† Raman spectroscopy is a power tool to characterize the material, two strong peaks of WSe_2 may be seen at 259 cm^{-1} (A_{1g}, out-of-plane mode), and 247 cm^{-1} (E^1_{2g}, in-plane mode), and SnS_2 has only one major peak (A_{1g}, out-of-plane) at 310 cm^{-1} as shown in Fig. 1(f). The specific Raman spectra of both materials are seen in Fig. S2(a) and (b), ESI.†

Raman intensity maps need an extensive understanding of the vdW heterostructure, material parameters, and Raman spectroscopy. To see how they were distributed spatially within the heterostructure, we checked intensity maps. The WSe_2 and SnS_2 grains are now perfectly cleaved laterally in the heterostructure avoiding the formation of alloy layers at their junction, as seen by the Raman intensity of WSe_2/SnS_2. In Fig. 1(b), the region chosen for Raman mapping investigation is outlined by yellow dashed lines. The graphical interpretation of the Raman intensity mapping of E_{2g} and A_{1g} for WSe_2, and A_{1g} for SnS_2 is shown in Fig. 2(a) and (c). The dark spaces in the figures show the placement of Cr/Au contacts and the space of
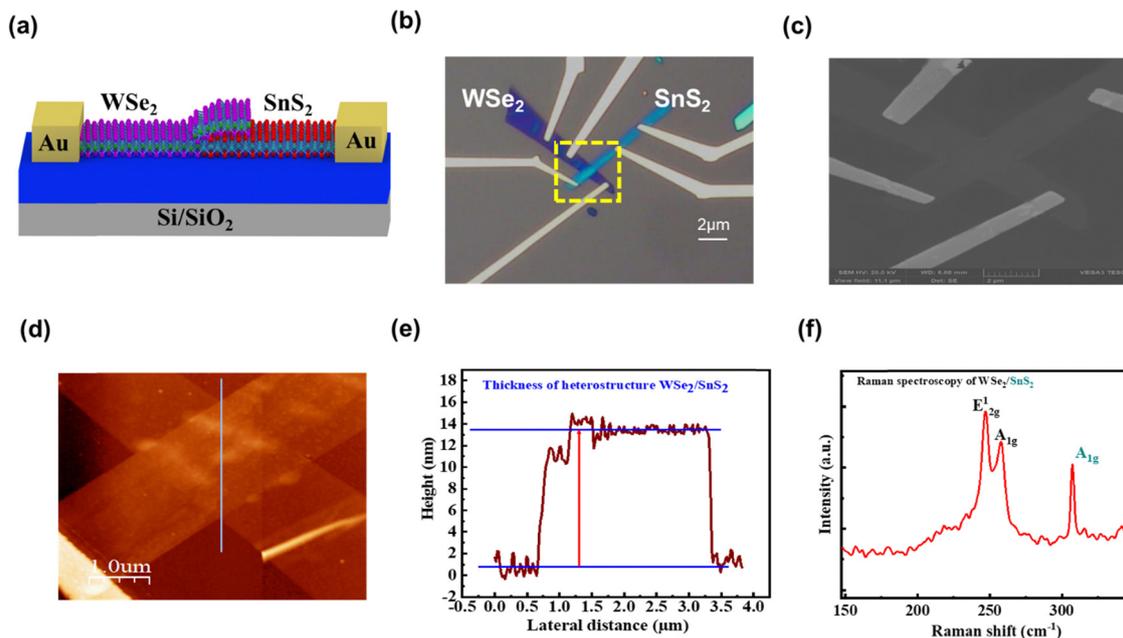
Fig. 1   (a) Graphical representation of the p–n device based on WSe$_2$–SnS$_2$ heterojunctions. (b) Optical image of the device that contains the flakes and metal electrodes. (c) SEM image of the device, and the scale bar is 2 µm. (d) AFM image of the device. (e) Height profile of the heterostructure. (f) Raman spectroscopy of the heterostructure WSe$_2$–SnS$_2$.

the heterostructure of both materials. These Raman intensity maps show the appropriate heterostructure developed by both materials WSe$_2$ and SnS$_2$.

The I–V curve of WSe$_2$ with a back-gate voltage is presented in Fig. 3(a), which shows a nonlinear curve due to the non-ohmic contact of Au/WSe$_2$. The I–V curve of SnS$_2$ with a back-gate voltage is represented in Fig. 3(b), which represents the linear curve due to the ohmic contact of Au/SnS$_2$. The transfer curves of WSe$_2$ with respect to back-gate voltages at V_{ds} = 0.2 V and 1 V are illustrated in Fig. 3(c), which demonstrates the dominant p-type behavior of WSe$_2$. Fig. 3(d) displays the transfer curves of SnS$_2$ with respect to the back-gate voltages at V_{ds} = 0.5 V and 1 V, which shows the dominant n-type behavior.

Additionally, the back-gate voltage (V_{bg}) was applied to measure the rectification characteristics of the WSe$_2$/SnS$_2$ vdW heterojunction diode. Fig. 4(a) illustrates the charge transport across the p–n junction for various V_{bg}, and the

maximum value of source–drain current is 47 µA. A p–n diode forms across the heterojunction, according to the clear current rectification behavior displayed by gate-tunable output curves. The increasing interlayer recombination is attributed to a substantial forward current (I_f), which may be controlled in TMDCs using V_{bg} (electrostatic gating) more successfully than in conventional materials. Due to the rise in the height of the potential barrier among the p-WSe$_2$/n-SnS$_2$ based diode, the reverse current is similarly reduced at a reverse bias (V_{ds} < 0). Fig. 4(b) shows the logarithmic plot of I–V curves at back-gate voltages. The rectification ratio (RR = I_f/I_r) is the ratio of forward-bias (I_f) to reverse-bias current (I_r). The variation in the RR with respect to V_{bg} is investigated and represented in Fig. 4(c), and the maximum value of the RR is about 2.9×10^4 at V_{bg} = −30 V. Because of the large drop in the leakage current, the magnitude of the RR is improved and adjusted more efficiently at a negative back-gate voltage (V_{bg} < 0 V). Because of the rise in the barrier
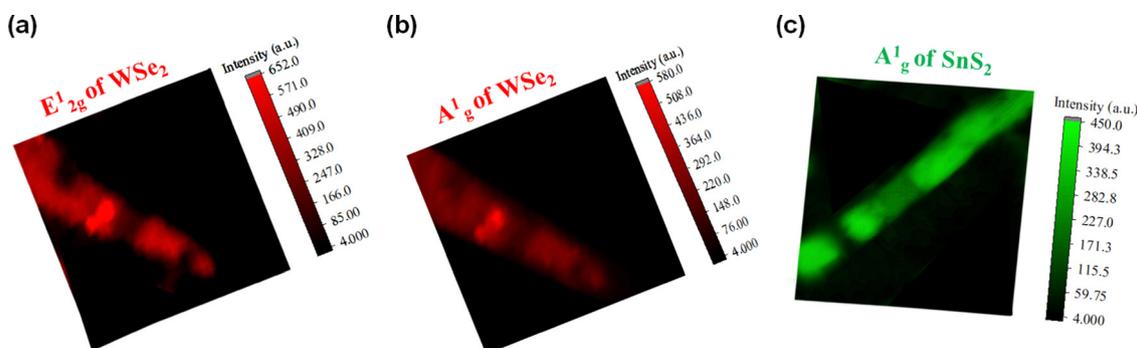

Fig. 2   Raman mapping for the heterostructure WSe$_2$–SnS$_2$. (a) Intensity maps of WSe$_2$ (E$^1_{2g}$) and (b) A$_{1g}$ of WSe$_2$. (c) Raman intensity map of SnS$_2$ (A$_{1g}$).
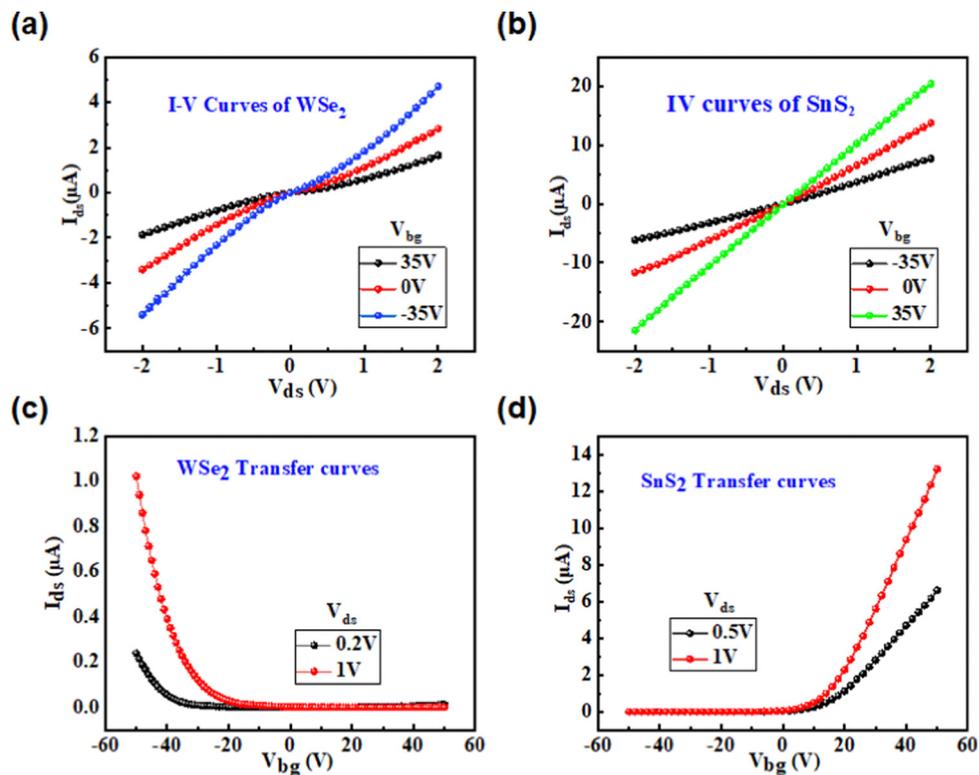
Fig. 3 (a) *I–V* curve of the multilayer flake of WSe$_2$, at different back-gate voltages (V_{bg}). (b) *I–V* curves of the multilayer SnS$_2$ flake at different back-gate voltages (V_{bg}). (c) The transfer curve of the WSe$_2$ flake clearly shows the dominant p-type behavior. (d) Transfer curves of SnS$_2$ show the n-type behavior.
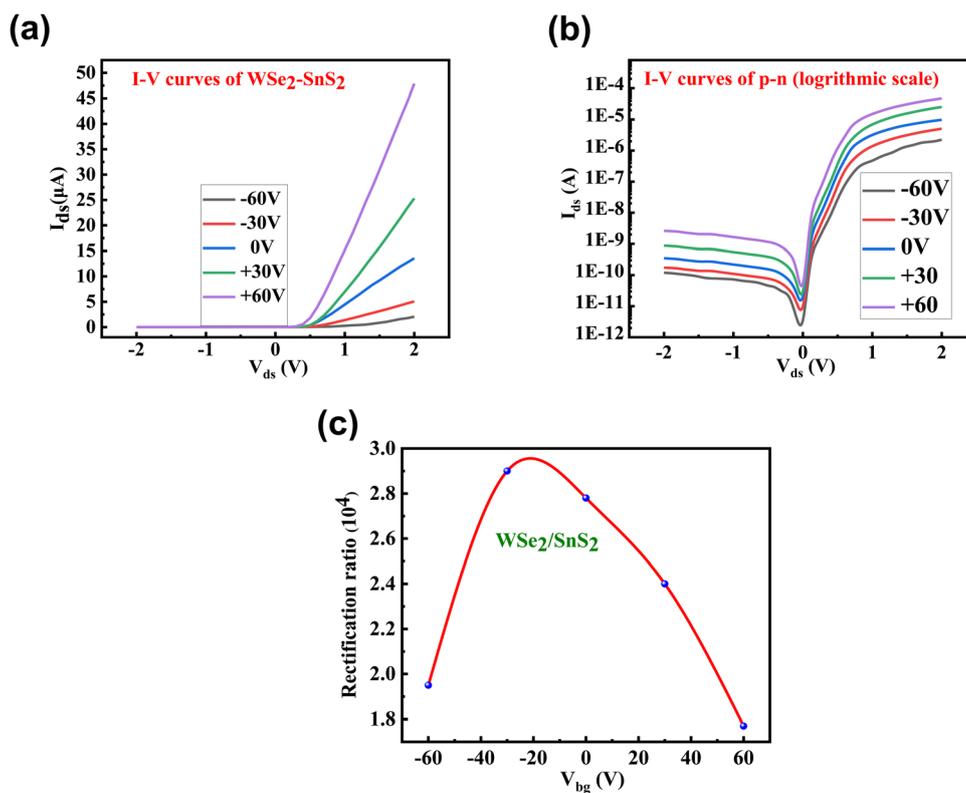

Fig. 4 (a) *I–V* characteristic curves of the heterostructure WSe$_2$–SnS$_2$ based p–n junction at various back-gate voltages. (b) *I–V* characteristic curve (logarithmic scale) of the p–n junction at different V_{bg}. (c) Change in the rectification ratio with respect to V_{bg}.

height at a low bias, I_r is decreased more efficiently than I_f at $V_{bg} < 0$ V. The ideality factor, also known as the diode ideality factor, is a parameter used to describe the deviation from ideal behavior in diodes or other semiconductor devices. The ideality factor (η) was calculated for the forward-biased zone by fitting the logarithmic I–V characteristics to the Shockley diode equation.

$$I_D = I_S \left[\exp\left(\frac{qV}{nk_B T} \right) - 1 \right] \qquad (1)$$

where I_D signifies the diode current, I_S symbolizes the reverse bias saturation current, V indicates the applied voltage, η signifies an ideality factor, T implies the temperature, q means the electronic charge, and k_B specifies Boltzmann's constant. The value of the ideality factor is $\eta = 1.41$ at $V = -30$ V. The specified estimate for the ideality factor is given in Fig. S3 (ESI†). In an ideal diode, the value of η is equal to 1. However, in practical diodes, the ideality factor is typically larger than 1, indicating non-ideal characteristics. The ideality factor considers various factors that affect the diode's behavior, such as recombination and trapping of charge carriers, series resistance, and deviations from the ideal energy-band structure. These factors can cause deviations from the exponential relationship described by the diode equation. In many diodes, the ideality factor falls in the range of 1 to 2, although it can vary depending on the diode technology, temperature, and other factors. A higher ideality factor indicates greater non-ideality and suggests the presence of additional mechanisms influencing the diode's behavior.

Fig. 5(a) shows the energy-band diagram with the work function, WSe$_2$ and SnS$_2$, conduction band minima, and valence band maxima. The band structure, carrier concentration, bandgap, device functioning, and optical features of a solid material, especially a semiconductor or an insulator, may all be understood from an energy band diagram. By understanding the energy levels and the occupancy of the bands, one can determine the availability of charge carriers and their behavior under different conditions, such as at equilibrium or under biasing.[43] For WSe$_2$, the Fermi level is close to the valence band, which exhibits p-type behavior, while in the case of SnS$_2$, it is close to the conduction band, which exhibits n-type behavior. The band diagram of the WSe$_2$/SnS$_2$ vdW heterostructure diode following

contact at zero V_{bg}, in which the Fermi level is positioned, is shown in the first section of Fig. 5(b). The zoom-in picture of the band alignment following the contact at zero V_{bg} is shown in the second section. As WSe$_2$ is the p-type semiconductor which will conduct because of the holes. These holes are controlled via a gate voltage and a threshold in current is observed during the transfer curve as the gate voltage is increased in the negative regime from 0 to -50 V. In contrast, the carrier transport in n-type SnS$_2$ is also regulated using the gate voltage because it conducts a high current due to electrons when the gate voltage is increased from 0 to $+50$ V (see Fig. 3c and d). The gate voltage plays a crucial role in controlling the charge carrier densities of holes and electrons in p-type WSe$_2$ and n-type SnS$_2$, respectively, and consequently influences the rectification ratio (RR). By manipulating the gate voltage, we can adjust the Fermi level. Specifically, at $V_{bg} < 0$ V, the Fermi level shifts away from the conduction band (CB), leading to an improvement in the potential barrier at the interface of the WSe$_2$/SnS$_2$ vdW heterojunction diode. This results in a higher rectifying current. Conversely, when the Fermi level moves toward the CB at $V_{bg} > 0$ V, the barrier height decreases, and the rectification ratio is reduced. Thus, the gate voltage serves as a powerful tool for modulating both charge carriers and band alignments in the WSe$_2$/SnS$_2$ vdW heterojunction diode, offering a versatile approach to designing highly efficient vdW heterostructures.

3. Photoresponse assessment for WSe$_2$/SnS$_2$

The photoresponse features of the p–n heterojunction WSe$_2$/SnS$_2$ were investigated using the schematic arrangement as shown in Fig. 6(a). The investigations were carried out by providing a drain voltage V_{ds} to WSe$_2$ (p-type, terminal "d") and grounding SnS$_2$ (n-type, terminal "s"). Time-resolved photoresponse experiments were done by turning on and off the laser light (220 nm, 11 mW cm^{-2}) to study the photoresponse of the WSe$_2$/SnS$_2$ p–n diode. With the on/off photo-switching trend at $V_{ds} = 0.3$ V and 0.5 V and no extra gate voltage, the photodetector demonstrates good stability and reliability. I_{ph} is the photocurrent, which is defined as $I_{ph} = I_{ight} - I_{dark}$, and the results obtained with a laser
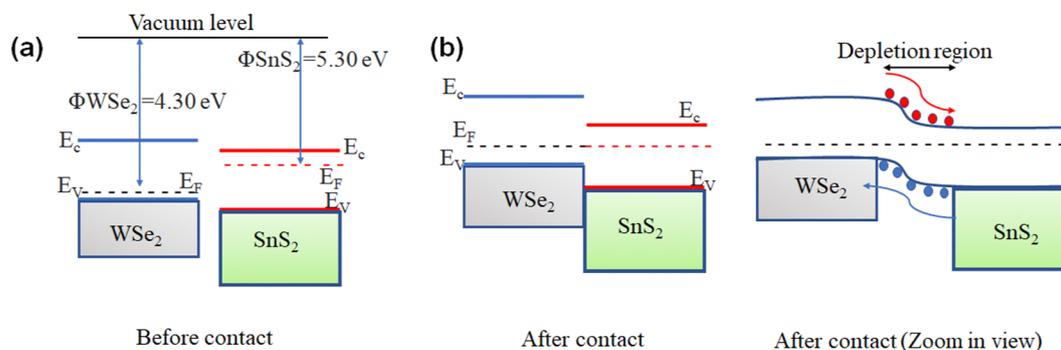

Fig. 5 Band diagram of a p-WSe$_2$/n-SnS$_2$ diode at $V_{bg} = 0$ V. (a) The band diagram of a p-WSe$_2$/n-SnS$_2$ diode before contact and (b) The diode after contact.

power are displayed at V_{ds} = 0.3 V and 0.5 V in Fig. 6(b). The photocurrent (I_{ph}) change measured was around 65 nA at V_{ds} = 0.5. At room temperature, this device represented a short circuit current (I_{sc}) of −8.72 nA and an open circuit voltage (V_{oc}) of 0.15 V when V_{bg} = 0 as presented in Fig. 6(c). A photodetector's responsivity is a metric that measures how well it can transform incoming light into an electrical signal. It shows the connection between the photodetector's optical power input and the consequent electrical output. Responsivity (R) is computed as:

$$R = \frac{I_{ph}}{PA} \qquad (2)$$

where I_{ph} is referred to as the photocurrent, P is the radiant light power density, and A is the operational area of the channel in the device. The device's responsivity may achieve 1.31 × 10^5 mA W^{-1} (P = 11 mW cm^{-2}). The EQE of the device is calculated using the following equation, which is about 7.3 × 10^4 (%).

$$EQE = R\frac{hc}{e\lambda}\% \qquad (3)$$

This equation has the following metrics: the wavelength of light (λ), the charge of an electron (e), the speed of light (c), and Plank's constant (h). The EQE value is defined by light absorption and the build-up of photo-generated carriers. Detectivity (D^*) is a measure of a photodetector's sensitivity, which may be calculated as $D^* = RA^{1/2}/(2e^*I_{dark})^{1/2}$, where R denotes responsivity, "A" is an operational area, e denotes the charge of electron, and I_{dark} is the dark current.[44,45] The detectivity (D^*) is about 3.13 × 10^{10} Jones. Understanding noise mechanisms is

crucial when working with photodetectors, and three major sources of noise are thermal noise, shot noise, and 1/f noise (flicker noise). Thermal noise, which is especially significant in room-temperature 2D photodetectors, is caused by the irregular thermal mobility of carriers inside the device's resistance. Shot noise is a common noise mechanism in low-light situations and arises from the discrete nature of carriers. It follows the Poisson process. Conversely, 1/f noise, often known as flicker noise, introduces random variations in the power spectral density that are inversely proportional to frequency. While its source is still up for debate, flicker noise can provide valuable information about the internal quality and reliability of a device. It is important to recognize that shot noise and heat noise appear primarily at higher frequencies.[46,47]

The rising and decay times were observed by fitting the data obtained through the photocurrent. The rise and decay time values are 0.52 s and 0.63 s, and the specified calculation and formula are represented in Fig. S4(a) and (b) (ESI†).

The photoresponse of the device at various wavelengths, as depicted in Fig. 6(d), reveals a decrease in the photocurrent as the wavelength of radiant light is increased. In a photodetector material, electron–hole pairs are generated when photons with sufficient energy are absorbed. The energy of photons is inversely proportional to their wavelength, as described by the equation $E = hc/\lambda$. As the wavelength increases, the energy of the incident photons decreases. For the efficient generation of electron–hole pairs and subsequent participation in the photocurrent, the energy of incident photons must be higher than the bandgap energy. When the incident photon energy is
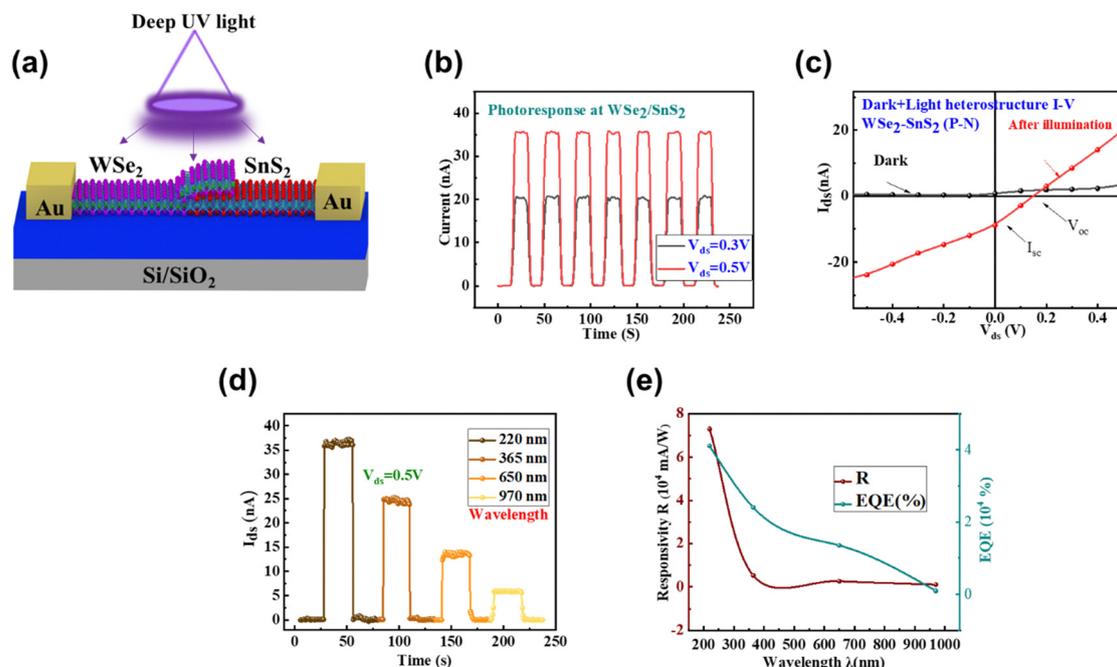
Fig. 6 (a) Schematic representation of the photocurrent measurement. (b) Time-dependent photoresponse of the WSe$_2$/SnS$_2$ p−n junction at fixed V_{ds} = 0.3 and 0.5 V. The light is on and off after a constant interval and the photoresponse is recorded. (c) I−V curves of the WSe$_2$/SnS$_2$ p−n junction in the dark and under light of 220 nm at zero gate voltage. (d) Photocurrent of the device at different wavelengths of incident light. (e) Variation in R and EQE at various wavelengths of radiant light.

lower than the bandgap energy, fewer electron–hole pairs are formed, leading to a reduction in the photocurrent. Therefore, the observed decrease in the photocurrent with an increase in the wavelength can be attributed to the diminishing capability of photons to overcome the bandgap energy barrier and generate electron–hole pairs. This clarification aligns with the observed variations in photoresponsivity (R) and EQE, as presented in Fig. 6(e). We will incorporate this improved explanation in our revised manuscript. The logarithmic plot of the photocurrent shown in Fig. 6(b) and (d) is also presented in Fig. S5 (ESI†) to see the on and off states clearly. Consequently, the 2D-based WSe_2/SnS_2 heterojunction broadband photodetector developed showed tremendous promise for fast and weak signal recognition applications in integrated optoelectronics.

4 Conclusions

In conclusion, this study successfully demonstrated the fabrication of high-quality WSe_2/SnS_2 vdW p–n junctions on a Si/SiO_2 substrate using the mechanical exfoliation technique. The resulting p–n junction exhibited an atomically sharp interface, which allows for reliable switching behavior, as demonstrated by a suitable rectification ratio (RR) of 2.9×10^4. The devices also displayed a low leakage current and a rapid photo response, making them well-suited for use in optoelectronic applications. We observed the photoresponse of the device in a broadband range with radiant light which is illuminated at various wavelengths. Under λ = 220 nm (illumination), the devices exhibited high sensitivity to incident light, as demonstrated by the measured photocurrent (I_{ph}) change of approximately 65 nA. The rise and decay time values are 0.52 s and 0.63 s, respectively. Additionally, the devices showed a high responsivity (R) of 1.31×10^5 mA W^{-1} and an external quantum efficiency (EQE) of 7.3×10^4 (%), indicating their capability of converting a high percentage of incident photons into electrical current. These excellent electrical and optoelectronic properties of the WSe_2/SnS_2 van der Waals p–n junction make it a promising candidate for use in energy-harvesting applications. Moreover, the successful development of these vdW heterostructures represents a significant step towards the design of high-performance integrated optoelectronic systems and products.

Data availability

Data are available on reasonable request.

Conflicts of interest

The authors declare no conflicts of interest.

Acknowledgements

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