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## PAPER

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### Introduction

Semiconductor nanowires have been considered to be the key components for future devices and systems due to their quantum confinement effect, large surface-to-volume ratio, and large absorption cross-section. Significant progress in nanowire-based devices such as solar cells, $1,2$  lasers, $3-5$ photodetectors, $6$  integrated photonic circuits, etc.<sup>7,8</sup> has been achieved in the past few decades. In particular, GaAs nanowires, which are representative of III–V semiconductor materials, have shown great applications in the fields of communication and near-infrared detection. $6,9-11$  However, unlike their bulk counterparts which exhibit only stable zinc blende (ZB) phases, metastable wurtzite (WZ) phases often appear in lowdimensional III-V materials.<sup>12</sup> In GaAs nanowires, the intermixing of ZB and WZ phases easily leads to structural defects that alter the band structure and reduce the mobility of charge carriers.<sup>13</sup> Therefore, such crystal phase intermixing in GaAs nanowires affects their optoelectronic properties, resulting in



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Semiconductor nanowires play a very important role in optoelectronic devices due to their excellent photoelectric properties. However, the intermixing of zinc blende and wurtzite crystal phases limits the development of GaAs nanowires, and how to obtain pure phase GaAs nanowires has become a research hotspot. In this study, the Si substrate is pre-etched and pure ZB phase GaAs nanowires are obtained by changing the effective V/III flux ratio through the shadowing effect. A series of nanowires with different morphologies and optical properties were obtained by pre-etching the oxide layer on the Si substrate at different times. We observed that pure ZB phase GaAs nanowires with good verticality were obtained when the etching time was 3 s. The principles of crystal phase control and materials properties were discussed in detail. These results suggest that the growth method of pure phase nanowires reported herein can be applied to other low-dimensional materials, which could pave the way for future nanowire devices. PAPER<br> **EXECUTE:**<br> **Choose the updates**<br> **Choose the control in self-catalyzed GaAs**<br> **Choose the updates**<br> **Choose the control in self-catalyzed GaAs**<br> **Choose the updates**<br> **Show the control in the simulation of any \theta** 

low emission efficiency and optical gain. To improve the crystal quality of GaAs nanowires, much effort has been devoted to the growth of materials by metal–organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) by optimizing the growth temperature, V/III flux ratio and catalyst.<sup>14-20</sup> Although the ZB and WZ phases in nanowires could be controlled by precisely tuning the growth parameters, the realization of pure phase GaAs nanowires by simple methods has always been a hot topic.

GaAs nanowires are usually grown based on the vapor– liquid–solid (VLS) mechanism, and using Au-catalytic or selfcatalytic methods. The Au-catalytic method utilizes Au droplets as the catalyst, while the self-catalytic method uses a group III element, such as Ga for GaAs nanowires, as the catalyst.<sup>21</sup> In comparison, the self-catalytic method is more widely used for growing nanowires due to the better growth quality, cleaner vacuum chamber and friendliness of Si-based integration. However, the growth of pure phase GaAs nanowires by the self-catalytic method is more challenging. With the development of research in this field, a nucleation-based model has been proposed to describe the surface energy and the formation energy. In this model, nucleation at the triple phase line (TPL) is typically used to solve the problem of WZ phase formation.<sup>12</sup> The results show that the higher cohesive energy of the WZ phase can be compensated by the lower surface energy when nucleation occurs at the TPL. Since then, the nucleation theory of nanowire growth has been further developed to include additional effects such as particle surface area,<sup>22</sup> Kashchiev renormalization,<sup>23</sup> polynucleate,<sup>24</sup> droplet morphology<sup>19,21</sup> and droplet depletion.<sup>25</sup>



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A recent study by Spirkoska et  $al^{13}$  showed that increasing the V/III flux ratio while holding other parameters constant results in an increase in the fraction of the ZB structure. This is in contrast to previous predictions using the highly approximate classical two-dimensional (2D) nucleation theory,<sup>12,22,26</sup> which has been used to describe the phase transition at the growth interface for Au-assisted NWs. Spirkoska et al.<sup>13</sup> argued that a possible reason for their findings could be that the vapor pressure has a large effect on the effective edge energies of the 2D nucleus, which could affect the WZ and ZB nucleation rates and therefore possibly favor ZB at large V/III flux ratio. They also pointed out the possibility of a relatively larger area for ZB nucleation events than WZ due to the critical nuclei becoming smaller with increasing supersaturation, since ZB is favored for nucleation away from the triple phase line (TPL) and WZ at the TPL.

In the MBE growth of self-catalytic GaAs nanowires on a Si substrate, most studies have focused on growth conditions (V/ III flux ratio, temperature, and Ga droplet pre-deposition), mainly to increase the nanowire growth yield.<sup>27-29</sup> However, several important features in the manipulation of substrate design have received little attention. In particular, the influence of substrate etching on the growth kinetics, the crystal phase, and ultimately the resulting nanowire properties has been underexplored. Although there are reports of self-catalyzed growth of GaAs nanowires on Si substrates, $17,30,31$  the growth mechanism of pure phase nanowires is not clear. In the research on patterned substrates, the main purpose is to control the position of the nanowires.<sup>32,33</sup>

In this work, it is shown that crystal phase control for GaAs nanowires can be achieved based on a simple but effective substrate pre-etching process. Our use of only the Si native oxide as a masking layer for MBE growth is simpler for GaAs. A previous study has proposed the growth of In(As)P nanowires by in situ deposition of In droplets on silicon substrates with natural oxides by metal–organic vapor phase epitaxy without a catalyst.<sup>34</sup> However, a considerable part of the nanowires are curved and of different lengths, and no completely vertical nanowires can be observed. According to the VLS growth mechanism of this work, we have obtained GaAs nanowires with high optical quality and good verticality. The density and size of the etched pinholes on the substrate determine the catalyst density, which in turn affects the equivalent V/III flux ratio during growth, and further affects the crystal phase of GaAs nanowires. Morphological and optical characterization was performed and the mechanism of crystal phase control was discussed in detail. These results suggest that the growth method proposed here can be applied to the growth of other semiconductor nanowires, which will be beneficial for research and application of nanoscale devices.

### Experimental

Prior to the growth of nanowires, the Si substrate was preetched. Si(111) substrates were immersed into a 10%

hydrofluoric acid (HF) solution. After this etching process, modification of the native oxide layer on the Si(111) substrate will result in pores with different densities for Ga droplets.<sup>16</sup> Then, according to the self-catalytic methods, GaAs nanowires were grown on the pre-etched substrate using an MBE system (DCA P600). The growth temperature was maintained at 620  $^{\circ}$ C, and the V/III flux ratio was fixed at 26 (the  $As<sub>4</sub>$  beam equivalent pressure was around 1.6  $\times$  10 $^{-6}$  torr and the Ga beam flow rate was 6.2  $\times$  10<sup>-8</sup> torr). The total growth time was 30 min. Immediately after the growth was completed, the Ga shutter was closed while the  $As<sub>4</sub>$  beam was maintained until the temperature cooled down to 400 °C.

The morphological properties of the samples were analyzed using a Hitachi S-4800 field emission scanning electron microscope (SEM). Transmission electron microscopy (TEM) measurements were performed using a FEI Tecnai G2 F20 microscope operated at 200 kV. X-ray diffraction (XRD) measurements were carried out using a diffractometer (model ULTIMA IV, Rigaku, Japan) with a  $2\theta$  range of  $25-30^\circ$  using Cu K $\alpha$  radiation ( $\lambda$  = 1.5418 Å) operating at 40 kV and 20 mA to determine the crystal phase of the samples. To discuss the optical properties of the samples, a 655 nm semiconductor diode laser was used as the excitation source. The emission from the samples was collected and dispersed using a HORIBA iHR550, and an InGaAs detector was used to detect the signal. A laser with an excitation power of 90 mW and a spot size of about 0.4  $\text{cm}^2$  was used for the temperature-dependent photoluminescence (PL) measurements, while the temperature was fixed at 10 K for the power-dependent PL measurements. Confocal µ-Raman spectra were recorded using a WITec Alpha 300R Raman spectroscope (WITec, Ulm, Germany) equipped with a 532 nm laser. The laser excitation power was adjusted to approximately 3 mW. Puper<br>
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### Results and discussion

We fabricated a series of samples with different substrate etching times. GaAs nanowires were simultaneously grown on the Si wafers covered with silicon dioxide. The morphology of the as-grown GaAs nanowires was characterized and their optical images are shown in Fig. 1(a). Regions A, B, C and D correspond to the GaAs nanowires grown on the substrates with etching times of 0, 3, 6 and 9 s, respectively. The boundaries of different regions can be clearly seen, and the samples with different etching times show different colors under light illumination, which is due to the differences in nanowire density, diameter and orientation. From the following measurements, it is known that nanowire arrays with high density, large diameter and good verticality appear white in the optical image. We have measured different positions and found that the nanowires in the same region have similar properties.

Fig. 1(b)–(e) show the top and cross-sectional SEM images of regions A, B, C and D shown in Fig. 1(a). In order to observe the overall verticality and growth density of the nanowires, we did not enlarge them with higher magnification. It can be seen





Fig. 1 (a) Optical image of GaAs nanowires grown on different regions (half of a 2-inch Si wafer) classified by etching time. Regions A, B, C and D correspond to the GaAs nanowires grown on the substrates with etching times of 0, 3, 6 and 9 s, respectively. The V/III flux ratio of the samples is all fixed at 26. (b)–(e) SEM images of region A–D. (f) Diameter and density statistics of GaAs nanowires grown on the different regions.

intuitively that the perpendicularity of the nanowires in region A is poor. However, the nanowire perpendicularity in regions B and C has been improved, while the nanowire arrays in region B grow almost vertically. These phenomena are consistent with the previous research result, which proposed that for thicker oxides, the orientation of nanowires with respect to the substrate is random. $35$  In contrast, in region D, the perpendicularity of the nanowires is found to be worse again. The reasons for this phenomenon will be explained later. According to the literature,<sup>36</sup> for Si(111) substrates, nanowires grown along the  $[011]$  direction are considered as vertical ones. The yields of vertical GaAs nanowires in four regions have been calculated, and the values were 25%, 95%, 89% and 60%, respectively. These results show that the orientation of the nanowires is improved after the substrate is etched. To describe the morphology of the nanowires more intuitively, the diameter and density of the nanowires in different regions were counted, and the statistical results are plotted in Fig. 1(f). During the etching time from 0 to 6 s, the density of the nanowires shows an

increasing trend, while the diameter of the nanowires gradually decreases. When the etching time is 6 s, the density and diameter reach their maximum and minimum values, respectively. When the etching time is further increased to 9 s, the density and diameter of the nanowires no longer follow the above trend, but show the opposite trend.

To explain the different orientations of the GaAs nanowires grown on substrates with different etching times as shown in Fig. 1, the evolution of the substrate with different etching times is shown in Fig. 2(a). During the self-catalytic growth, we have found that the interaction of the reactive gallium with the  $SiO<sub>2</sub>$  pinholes induces the formation of nanocraters, which is an important prerequisite for the nucleation of the nanowires.<sup>37,38</sup> Ga droplets are formed inside the etched pinholes, and the growth direction of the nanowires is related to the contact angle between the catalysts and the substrate.<sup>19</sup> The natural oxide layer on top of the Si substrate has poor uniformity.<sup>38</sup> Previous scanning tunneling microscopy studies confirm that Ga atoms tend to accumulate in existing defects



Fig. 2 (a) Schematic diagrams of the substrates etched for 0, 3, 6, and 9 s, respectively. (b) Schematic diagram of single GaAs nanowire growth. (c) and (d) Schematic diagrams of the self-catalytic growth of GaAs nanowires without and with shadowing effect, respectively. Light green areas indicate that there is no competition among adatoms, while dark green areas indicate that there is competition among them.

on  $SiO<sub>2</sub>$  surfaces, leading to the formation of larger nanocavities.<sup>39</sup> When Ga droplets are deposited directly on the untreated Si substrate, the larger and sparser holes on the surface of the oxide layer become the attachment points for the Ga droplets. The droplet will not completely fill these holes resulting in a contact angle between the droplet and the substrate of less than  $90^\circ$ . In this case, the nanowires tend to grow parallel to the substrate after nucleation at the TPL.<sup>19,40</sup> Therefore, the nanowires grown in region A have poor perpendicularity, large diameter and low density. When the substrate is etched for 3 and 6 s, HF removes some of the natural oxide layer, which changes the size and density of the original holes. The holes created by the etched substrate are called pinholes. Previous studies have shown that gallium atoms interact with  $SiO<sub>2</sub>$  to form sparse nanocraters on pre-existing subnanometer pinholes. As the oxide layer on the surface of the substrate thins, the nanocraters reach the underlying Si surface and form an epitaxial relationship with the GaAs nanowires. Similar to the situation reported in the literature, when nanowires grow in contact with the substrate, they tend to grow vertically in  $Si(111).$ <sup>38,41,42</sup> In addition, the contact angle between the droplet and the substrate decreases with decreasing pinhole size, and the nanowires prefer to grow more vertically. This is consistent with the results observed in Fig. 1. When the etching time is 9 s, the natural oxide layer on the substrate is almost etched away. At this point, the natural oxide layer is so thin that some of the etched pinholes disappear. Under the same growth conditions, a shallower depth will cause the droplet to overflow from the etched pinhole and merge with the surrounding ones, increasing the size and the contact angle between the droplet and the substrate. In this case, the shape of the droplet will be asymmetric, and the nanowires may grow outside the etched pinhole. Vertical growth of the nanowires is then not guaranteed due to the poor confinement. A. Fontcuberta i Morral et al.<sup>38</sup> concluded that growth directly on a GaAs surface under the same conditions did not result in the formation of nanowires. Mattila et  $al^{34}$  also came to a similar conclusion. In our study, the silicon dioxide layer in region D has been partially removed, which may reduce the growth of nanowires and lead to a decrease in nanowire density. Paper Maccess Articles. Leading to the formation of larger nano-<br>Adense Articles Artic

The size and density of the etched pinholes will also affect the effective V/III flux ratio during the growth due to the shadowing effect. $43-45$  To explain the growth mechanism, schematic diagrams have been drawn and are shown in Fig. 2(b)– (d). At the very beginning of the nanowire growth, the catalyst is formed inside the etching pinhole. Once the droplet is oversaturated with the group V flux, the nanowire starts to grow along the axis. At the same time, the group III flux should be maintained to prevent the droplet from being consumed. During the growth of the GaAs nanowires, there are three different sources of elements, $44,46$  namely, the direct impingement on the droplet surface, adsorption on the substrate surface and the nanowire sidewalls. Fig. 2(b) illustrates the growth of a single GaAs nanowire based on the model of Peter Krogstrup.<sup>17</sup> The adsorbed atoms would diffuse into the droplet along the substrate surface and the nanowires'

sidewalls. There are two distinct growth regimes in the nanowire growth, i.e., a diffusion-limited and competitive regime, as previously reported for NW growth in other III–V material systems. $47,48$  For the adsorption of atoms from the substrate, the average migration distance prior to incorporation is defined as the diffusion length, and denoted by  $R$ . The circular area formed with a radius of  $R$  is called the diffusion area. When multiple catalysts are formed simultaneously, as long as their diffusion areas do not overlap, that is, the diffusion length is shorter than the distance between adjacent etched pinholes, the effective diffusion area will still be determined by the diffusion length, as shown in Fig. 2(c). The Ga flux is limited by substrate surface diffusion alone, which is called the diffusion-limited growth regime. In this regime, the supplied Ga outside the diffusion region of the nanowires hits the  $SiO<sub>2</sub>/$ Si(111) substrate too far away from the NW, and thus, cannot be collected in the NW but rather desorbs or nucleates in the form of parasitic GaAs clusters.<sup>43</sup> Since the catalyst droplets formed are dense on the substrate, the collection of Ga adatoms is obviously strongly governed by the distance between adjacent NWs, as shown in Fig. 2(d). In this competitive regime, Ga adatom flux to the NW growth front is limited by two mechanisms: In the early growth stage, when growth is mainly controlled by surface diffusion on the  $SiO<sub>2</sub>$  mask, Ga collection is limited by material competition. With increasing growth time also the collection of adatoms impinging on the GaAs NW sidewalls also becomes important. Here, the arrival rate of directly impinging Ga adatoms and the subsequent sidewall diffusion to the Ga droplet becomes increasingly shadowed by the high density of neighboring NWs. Thus, a reduction in the effective Ga flux at the growth front is expected.<sup>43</sup> It is important to note that the distance between nanowires primarily affects the local Ga flux, and hardly affects the As flux. Arsenic contributes to NW growth mainly by direct impingement on the Ga droplet and not via surface diffusion.<sup>35,49</sup> This effect, hereafter referred to as the shadowing effect, will limit the Ga flux into the Ga droplets and increase the V/III flux ratio. According to the previous introduction, this will be more favorable for the growth of pure-phase GaAs nanowires.

In order to intuitively characterize the crystal phase in the GaAs nanowires grown on the substrate with different etching times, TEM characterization of the GaAs nanowires in regions A and B was performed and the results are shown in Fig. 3. Fig. 3(a) shows the TEM image of GaAs nanowires grown in region A. In the magnified TEM as shown in the inset of Fig. 3(a), the yellow circles mark the ZB phases and the white triangles mark the WZ phases. It can be seen that there is severe phase intermixing formed as stacking faults along the nanowires. This observation is also supported by the diffraction pattern of the nanowires in region A shown in Fig. 3(b). Fig. 3(c) shows the GaAs nanowires grown in region B. The inset shows the TEM magnification of a small section of the GaAs nanowire. It can be seen that the diameter of the nanowires is reduced and no distinct phase intermixing can be observed. The diffraction pattern in Fig. 3(d) also suggests that the crystal phase of the GaAs nanowires is pure ZB.



Fig. 3 (a) TEM image of GaAs nanowires grown in region A. The filled yellow circles mark the ZB phase while filled white triangles indicate the WZ phase in the inset. (b) Diffraction pattern of GaAs nanowires grown in region A. (c) TEM image of the GaAs nanowires grown in region B. (d) Diffraction pattern of GaAs nanowires grown in region B.

Based on different as-grown nanowires with variable substrate etching time, we clearly show the existence of different crystal phases, which strongly depend on the size and density of etched pinholes and which further lead to distinct differences in the physical properties, such as the PL characteristics. To further verify the regular changes in the energy band structure and carrier distribution of nanowires grown in different regions, the optical properties of the entire array were characterized. Fig.  $4(a)$  shows the low temperature  $(10 K)$  PL from GaAs nanowires grown in different regions. Before performing PL experiments on the samples, we used the mechanical method to transfer nanowires out of the substrate and performed luminescence experiments on the substrate parasites. The experimental results excluded the possibility of PL from



Fig. 4 (a) Low temperature (10 K) normalized PL emission of GaAs nanowires grown on substrates with different etching times. (b) Powerdependent PL emission of GaAs nanowires grown on region A at low temperature (10 K). (c) Temperature-dependent PL spectra of GaAs nanowires grown on region D. (d) Normalized PL emission of regions A, B and C at low temperature (10 K).

these parasites and ensured that the PL experiment data were derived from nanowires. It can be seen that all samples exhibited the GaAs excitonic emission at 1.515 eV due to the presence of ZB crystal phases.<sup>13</sup> For easier comparison, all spectra have been normalized to this peak. It can be seen that all samples have another emission with a photon energy of 1.492 eV. Considering the metastable WZ crystal phase, the emission at 1.492 eV is then considered to be related to the coexistence of the WZ and ZB phases in the GaAs nanowires.<sup>50</sup> The band gap of the WZ and ZB phases in GaAs nanowires is different. The conduction band and the valence band of the WZ crystal phase of GaAs are higher than those of ZB. Therefore, a type II band structure will be formed at the interface. In this structure, electrons are confined in the conduction band of the ZB phases, and holes are confined in the valence band of the WZ phases. Therefore, electrons and holes recombine and give rise to emission with a photon energy of 1.492  $eV<sup>13</sup>$  It is interesting to note that this peak exhibits a slight blueshift with the increase in excitation power, as shown in Fig. 4(b), which is a characteristic of the type II band structure.<sup>51,52</sup> **Examples Articles.** And the september 2023. The common access Article is license to the september 2023. The september 2023. The september 2023. The september 2023. The september 3.1:29 AM. The september 3.1:29 AM. The sep

In addition, a closer look reveals that there is a high-energy band tail of the emission from samples in region C. Considering that the band gap of the GaAs WZ crystal phase is larger than that of  $\text{ZB},^{53,54}$  we further perform peak fitting for the PL data of region C (results are not included in this paper), the high energy emission peak is located in 1.525 eV, which is consistent with that of the low-temperature WZ phase. It is believed that the high-energy band tail originates from the exciton recombination of the WZ crystal phase. The photon energy of the dominant peak for nanowires in region D is low (1.457 eV), and this emission peak is absent for other samples. During the temperature-dependent PL measurement, this peak rapidly disappears with the increase in temperature, as shown in Fig. 4(c). Therefore, this low-energy emission is considered to be from defects. Chen et al. observed a similar peak, which they attributed to a related recombination with an unknown deeper residual acceptor level.<sup>55</sup> It is worth noting that a weak broad emission at 1.35–1.4 eV was observed in both samples A and B. First of all, Spirkoska et  $al.^{13}$  proposed that when the proportion of ZB phase in nanowires is reduced from 100% to 30%, the type II peak lies between 1.43 eV and 1.515 eV, so the correlation between the above luminescence peak and type II luminescence is excluded. Then, we analyze the PL with variable power, and we do not find that this peak follows the characteristic of type II luminescence, that is, the blue shift occurs with the increase in power. Then, by consulting the literature, it is found that the luminescence peak at 1.35–1.4 eV may be probably related to a transition involving the gallium vacancy level.<sup>56,57</sup> Based on the above analysis, the intensity ratio of the emission at 1.515 to 1.492 eV can be used to describe the existence of WZ and ZB phases in different regions. The spectra of the three regions A, B and C are normalized as shown in Fig. 4(d). From the results of optical characterization, it can be inferred that the nanowires in the region B are dominated by the ZB crystal phase.



Fig. 5 (a) and (b)  $\mu$ -Raman spectra of single GaAs nanowires grown in regions B and C, respectively. XRD spectra of (c) Region B and (d) Region C.

To further discuss the crystal phase of the materials,  $\mu$ -Raman measurements were performed on a single nanowire which was mechanically transferred to a new Si substrate after ultrasonic cleaning. The Raman spectra of the GaAs nanowires grown in regions B and C are shown in Fig. 5(a) and (b), respectively. Compared to the nanowire grown in region B, four distinct scattering peaks can be observed in region C. To better discuss the origin of the diffraction peaks, a Lorentzian fitting was performed and the corresponding Raman scattering peaks are found to be around 256.9, 266.9–267.9, 288.2 and 291.5  $\text{cm}^{-1}$ , respectively. The diffraction peaks are correspondingly assigned to E2, TO, SO and LO, which are consistent with previous reports in the literature.<sup>58,59</sup> Due to the small diameter of the nanowires, the peaks in the first-order Raman spectrum with frequencies between the TO and LO modes have been previously observed in several III-V nanowires and were identified as surface optical (SO) modes.<sup>60</sup> Therefore, different from the ZB phase, the Raman spectrum of the WZ phase exhibits a unique scattering peak of the E2 mode. The XRD results of the corresponding nanowires are shown in Fig. 5(c) and (d), respectively. It can be seen that a GaAs-related diffraction peak appears on the left side of the Si(111) signal. For nanowires grown in region B, only the GaAs(111) peak can be found, and the corresponding peak position is  $27.33^{\circ}$  with a full-width half maximum (FWHM) of  $0.145^{\circ}$ . Two diffraction peaks, GaAs(002) and GaAs(111), can be observed in nanowires grown in region C, and the corresponding peak positions are  $27.19$  and  $27.33^{\circ}$ , and their FWHMs are 0.12 and 0.15 $^{\circ}$ , respectively. Therefore, it can be confirmed that the WZ and ZB crystal phases coexist in the nanowires grown in region  $C<sup>61</sup>$ 

### **Conclusions**

In conclusion, we have obtained pure ZB phase GaAs nanowires by a simple substrate etching method. A series of GaAs nanowires with different densities and diameters were obtained.

SEM, TEM, PL, Raman and XRD were used to characterize the nanowires grown on the substrate with different etching times under the same growth conditions. Analysis of the experimental results shows that the crystal phase in GaAs nanowires can be controlled by adjusting the size and density of the etched pinholes, combined with the shadowing effect to adjust the equivalent V/III flux ratio during the growth process. This work demonstrates the dynamics of the crystal phases in GaAs nanowires by simple substrate etching, which can be applied to other semiconductor nanowires, and facilitates the study of nanoscale devices.

### Author contributions

X. H. Wang, R. Chen and Z. P. Wei are responsible for the original conception of this work. The manuscript was prepared based on the research contributions from all the authors, namely J. L. Tang and Y. B. Kang are responsible for sample preparation, and S. Wang and H. L. Li performed the sample testing, data analysis, and the writing of the manuscript.

### Conflicts of interest

There are no conflicts to declare.

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