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Dielectric ceramics/TiO_2/single-crystalline silicon nanomembrane heterostructure for high performance flexible thin-film transistors on plastic substrates

Guoxuan Qin, *[ab] Zhihui Pei,[ab] Yibo Zhang,[ab] Kuibo Lan,[ab] Quanning Li,[c] Lingxia Li,[a] Shihui Yu [a] and Xuejiao Chen*[c]

A dielectric ceramics/TiO_2/single-crystalline silicon nanomembrane (SiNM) heterostructure is designed and fabricated for high performance flexible thin-film transistors (TFTs). Both the dielectric ceramics (Nb_2O_3–Bi_2O_3–MgO) and TiO_2 are deposited by radio frequency (RF) magnetron sputtering at room temperature, which is compatible with flexible plastic substrates. And the single-crystalline SiNM is transferred and attached to the dielectric ceramics/TiO_2 layers to form the heterostructure. The experimental results demonstrate that the room temperature processed heterostructure has high quality because: (1) the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure has a high dielectric constant (~76.6) and low leakage current. (2) The TiO_2/single-crystalline SiNM structure has a relatively low interface trap density. (3) The band gap of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure is wider than TiO_2, which increases the conduction band offset between Si and TiO_2, lowering the leakage current. Flexible TFTs have been fabricated with the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure on plastic substrates and show a current on/off ratio over 10^4, threshold voltage of ~1.2 V, subthreshold swing (*SS*) as low as ~0.2 V dec^{-1}, and interface trap density of ~10^{12} eV^{-1} cm^{-2}. The results indicate that the dielectric ceramics/TiO_2/SiNM heterostructure has great potential for high performance TFTs.

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Introduction

Flexible electronics have drawn more and more interest and have been applied in a variety of applications including flexible displays, wearable devices, flexible photosensors, *etc.*[1–6] Single-crystalline silicon is considered to be the best candidate semiconductor material for flexible devices, for the advantages of high carrier mobility and being compatible with the industrial complementary metal oxide semiconductor (CMOS) process. Single-crystalline silicon nanomembrane (SiNM) has been employed in many flexible devices and circuits, *e.g.* flexible diodes,[7] flexible photodetectors[8,9] and flexible microwave switches.[10] In particular, flexible thin-film transistors (TFTs) are one of the most essential and fundamental devices, and flexible TFTs based on single-crystalline SiNM show great potential for high performance applications.[11–15]

However, limitations still exist for high performance flexible single-crystalline Si TFTs, *i.e.* high quality gate dielectric materials and suitable structures designed for flexible devices. To date, the dielectric materials for flexible SiNM TFTs are mostly SiO_x by low-temperature chemical vapor deposition (CVD) or SiO by evaporating, and have relatively low dielectric constant and electrical properties.[16,17] High-*k* dielectrics have been already used for high performance TFTs on bulk substrates, among which metal oxides are common, such as ZrO_2, HfO_2 and La_2O_3 as gate dielectric layer of TFT for a high current on/off ratio, low operating voltage and low power consumption.[18–21] Investigations of high-*k* gate dielectrics on performance of CMOS and TFTs devices have been also conducted.[22–25] However, most of these high-*k* materials are deposited by solution process or sputtering including post-annealing (≥400 °C)[18,19] or atomic layer deposition (ALD) (≥300 °C)[20] which is incompatible with flexible substrates. Multilayer gate stacks with high-*k* and high band gap materials have been also investigated in recent years.[26–34] The fabricating methods mainly include ALD,[28,29] solution process[30,31] and sputtering.[32–34] However, these multilayer structures are still not suitable for flexible TFTs. For example, ALD deposited or solution-processed gates with processing temperature at least 300 °C (such as TiO_2/Al_2O_3 (ref. 28) and Al_2O_3/SiO_2 (ref. 29) by ALD, TiO_2/Al_2O_3/TiO_2/Al_2O_3/TiO_2 (TATAT)[30] and TiO_2/Al_2O_3 (ref. 31) by solution process) exceed the maximum process

[a]School of Microelectronics, Tianjin University, Tianjin, 300072, P. R. China. E-mail: gqin@tju.edu.cn
[b]Tianjin Key Laboratory of Imaging and Sensing Microelectronic Technology, Tianjin, 300072, P. R. China
[c]State Key Laboratory of Precision Measuring Technology and Instruments, Tianjin University, Tianjin, 300072, P. R. China. E-mail: chenxuejiao@tju.edu.cn

temperature that flexible substrates can withstand. On the other hand, lowering the processing temperature or room-temperature magnetron sputtering will significantly degrade the electrical properties of these dielectrics, such as high trap density, higher leakage current, higher subthreshold swing and thus poor subthreshold characteristics, *etc.*[32–34] In addition, these single-layer or stacked dielectrics are mostly fabricated and employed for oxide semiconductor TFTs rather than Si TFTs. As a result, it is necessary to find high quality dielectric materials and design the gate structure with low process temperature for high performance flexible single-crystalline silicon TFTs.

In this paper, a dielectric ceramics/TiO_2/single-crystalline SiNM heterostructure is designed and fabricated for high performance flexible TFT on plastic substrates. The dielectric ceramics Nb_2O_3–Bi_2O_3–MgO has relatively high dielectric constant and low leakage current. TiO_2 as a nontoxic and abundant ceramic material with high dielectric constant, high electrical properties and long-term stability has been applied in various optical and electrical fields, such as photocatalytic system, thin-film transistors and gas sensors.[35–38] In this work, both the dielectric ceramics Nb_2O_3–Bi_2O_3–MgO and TiO_2 are deposited by radio frequency (RF) magnetron sputtering at room temperature, which is compatible with the flexible plastic substrates. And the single-crystalline SiNM is transferred and attached to the dielectric ceramics/TiO_2 layers to form the heterostructure.

The flexible TFTs with dielectric ceramics Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure on plastic substrates are fabricated and characterized. The experimental results demonstrate that the room-temperature processed heterostructure has high quality including: (1) the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure has high dielectric constant and low leakage current. (2) The TiO_2/single-crystalline SiNM structure has relatively low interface trap density. (3) The band gap of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure is wider than TiO_2, which increases the conduction band offset between Si and TiO_2, lowering the leakage current. The flexible TFTs show a high current on/off ratio, low threshold voltage and subthreshold swing. The TFTs also indicate good performance stability under mechanical bending conditions. The results indicate that the dielectric ceramics/TiO_2/SiNM heterostructure has great potential for high performance flexible TFTs.

Experimental

The fabrication process schematic of the flexible TFTs is shown in Fig. 1. The bottom-gate electrode indium-tin-oxide (ITO) (∼100 nm) was first deposited on polyethylene terephthalate (PET) substrate (∼175 μm) by RF magnetron sputtering at room temperature. Then double gate dielectric layers Nb_2O_3–Bi_2O_3–MgO (∼50 nm) and TiO_2 (∼50 nm) were deposited from the Nb_2O_3–Bi_2O_3–MgO and TiO_2 ceramic targets by magnetron sputtering. The vacuum chamber was evacuated to 9.0×10^{-6} torr before sputtering. Then high-purity Ar and O_2 from separated gas flow controller were introduced and the ratio of Ar/O_2 is 17 : 3. During the process of sputtering, the total pressure was 10 mTorr and the deposited power was set to be 100 W. The deposition parameters were optimized to achieve the best electrical properties for Nb_2O_3–Bi_2O_3–MgO and TiO_2. The single-crystalline SiNM is the top template layer (∼200 nm) of silicon on insulator (SOI) with buried oxide layer (∼450 nm) and bottom Si handling substrate. The source and drain regions (N^+ regions) were first patterned on SOI by lithography process. Then phosphorus (P) ion implantation was carried out with 40 keV injection energy and 4×10^{15} cm^2 dose, followed by 45 min furnace annealing at 850 °C in N_2 atmosphere. Next, a 15 μm × 15 μm holes array with a pitch distance of 50 μm was etched on the top Si template layer by lithography and reactive iron etching (RIE). Afterward, SOI was put into diluted hydrofluoric acid (HF, 49% HF : water = 1 : 1) for 25 min to remove the buried oxide layer, after which the top SiNM was released from the handling substrate in deionized (DI) water, transferred and attached to Nb_2O_3–Bi_2O_3–MgO/TiO_2 gate dielectric layer on the plastic substrate. The source and drain electrodes with Cr (∼30 nm) and Au (∼70 nm) stack were then deposited by electron beam evaporation. The frequency–capacitance and capacitance–voltage characteristics of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 and Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructures, as well as the direct-current (dc) characteristics of the flexible TFTs were measured by a Keithley 4200 SCS semiconductor characterization system. The spectra and band gap of Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure were measured using a UV-3600Plus ultraviolet-visible spectrophotometer.

Results and discussion

Fig. 2 shows the interface morphologies of Nb_2O_3–Bi_2O_3–MgO/TiO_2 and the characteristics of Nb_2O_3–Bi_2O_3–MgO/TiO_2 and Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructures. The scanning electron microscope (SEM) images of interface morphologies of Nb_2O_3–Bi_2O_3–MgO/TiO_2 are shown in Fig. 2a and b, respectively. The AFM images of Nb_2O_3–Bi_2O_3–MgO and TiO_2 layers are displayed in Fig. 2c and d. The calculated RMS of Nb_2O_3–Bi_2O_3–MgO and TiO_2 is ∼4.13 nm and ∼2.45 nm, respectively. The AFM image and RMS values show consistent results to the SEM data, indicating that the surface of TiO_2 is much smoother than that of Nb_2O_3–Bi_2O_3–MgO and has improved surface roughness to Nb_2O_3–Bi_2O_3–MgO layer, which contributes to reducing the carrier scattering center and improving the interface quality with SiNM.

Fig. 2e shows the leakage current density of Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure with different thickness, indicating low leakage current density of the heterostructure. ∼100 nm dielectrics is chosen in this work. Fig. 2f shows the leakage current density of the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure, showing that the leakage current density is still very low even with the SiNM. The leakage current density of Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM is lightly higher than that of Nb_2O_3–Bi_2O_3–MgO/TiO_2, because SiNM is lightly P-doped in which there are carrier drift with applied voltage.[39] Frequency–capacitance and capacitance–voltage characteristic of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure at 1 kHz, 10 kHz, 100 kHz and 1 MHz are shown in Fig. 2g and h, respectively. The capacitance

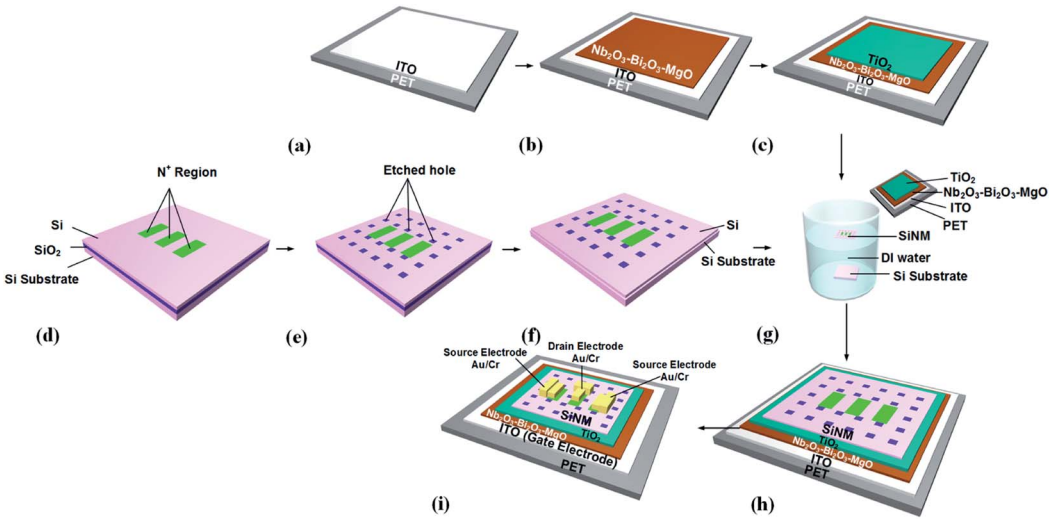

Fig. 1 Process flow schematic of the flexible TFTs (drawn not to scale): (a) ITO deposited on the PET flexible substrate. (b) Nb_2O_3–Bi_2O_3–MgO deposited on the ITO/PET. (c) TiO_2 deposited on the Nb_2O_3–Bi_2O_3–MgO/ITO/PET. (d) Source and drain active regions patterned and doped on SOI. (e) Hole array patterned and etched. (f) Buried oxide layer removed in HF. (g) The top SiNM released in DI water. (h) SiNM transferred onto the TiO_2/Nb_2O_3–Bi_2O_3–MgO/ITO/PET substrate. (i) Source and drain electrodes formed by evaporating Cr/Au (30 nm/70 nm).

slightly increases from ~0.655 μF cm^{-2} to ~0.75 μF cm^{-2} as frequency decreases from 1 MHz to 1 kHz, which indicates that the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure has low frequency sensitivity and the dielectric constant (ε_r) can be extracted from the following equation:

$$C_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}} \quad (1)$$

where C_{ox} is the unit capacitance of the heterostructure. ε_0 is vacuum dielectric constant, t_{ox} is thickness of the heterostructure (~100 nm). ε_r is calculated to be ~74.2 at 1 MHz, ~76.6 at 100 kHz, ~79.1 at 10 kHz and ~84.7 at 1 kHz, respectively. The dielectric constant of the heterostructure is much higher than those of SiO, SiO_x or most low-temperature processed dielectrics.

Frequency–capacitance and capacitance–voltage characteristic of the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure at 100 kHz and 1 MHz are shown in Fig. 2i and j, respectively. The capacitance of the heterostructure can be calculated as follows:

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_{Si}}\right)^{-1} \quad (2)$$

where C is the capacitance of the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure, C_{ox} is the capacitance of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure and C_{Si} is the capacitance of SiNM, which is influenced by the depletion region width and inversion layer charge in SiNM. The capacitance of the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure decreases from ~0.72 μF cm^{-2} to ~0.47 μF cm^{-2} with the frequency from 1 kHz to 1 MHz. The reason for this is that at low frequency, the mobile electrons accumulate in the surface of SiNM close to TiO_2 and the capacitance of the heterostructure is almost same as C_{ox}.

The capacitance–voltage curves consist of accumulation and inversion regions at high frequency of 100 kHz and 1 MHz. When a negative gate voltage is applied, the capacitance works in accumulation region and it equals to C_{ox}. When the applied gate voltage increases, the inversion layer is formed at the Si/TiO_2 interface and the capacitance of the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure is the series capacitances of C_{ox} and the depletion capacitance in SiNM. Therefore, the capacitance of the heterostructure decreases and eventually keep stable as the gate voltage increases.

The optical image, microscope image and structure schematic of the flexible TFTs with Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure fabricated on plastic substrates are shown in Fig. 3a–c, respectively. The transfer and I–V characteristics of TFT with channel width (W) and channel length (L) of 60 μm and 3 μm are shown in Fig. 3d and e, respectively, as an example, in which I_{ds} is the drain current, g_m is the transconductance, V_{ds} is the drain voltage and V_{gs} is the gate voltage. The threshold voltage (V_{th}) extracted from Fig. 3d is ~1.2 V, indicating that the flexible TFT has high drive capability. The saturation drain current of the flexible TFT is ~28 μA with only ~nA leakage current when the gate voltage is 2.5 V, and the current on/off ratio is over 10^4. The maximum transconductance of the flexible TFT reaches to ~40 μS when gate voltage is 2.1 V. The subthreshold swing (SS) is calculated to be ~0.2 V dec^{-1} by:

$$SS = \frac{\partial V_{gs}}{\partial(\lg\ (I_{ds}))} \quad (3)$$

The interfacial trap density (D_{it}) can be calculated based on the SS value as follows:[40]

$$D_{it} = \left(\frac{SS \times \lg\ e}{kT/q} - 1\right) \times \frac{C_{ox}}{q^2} \quad (4)$$

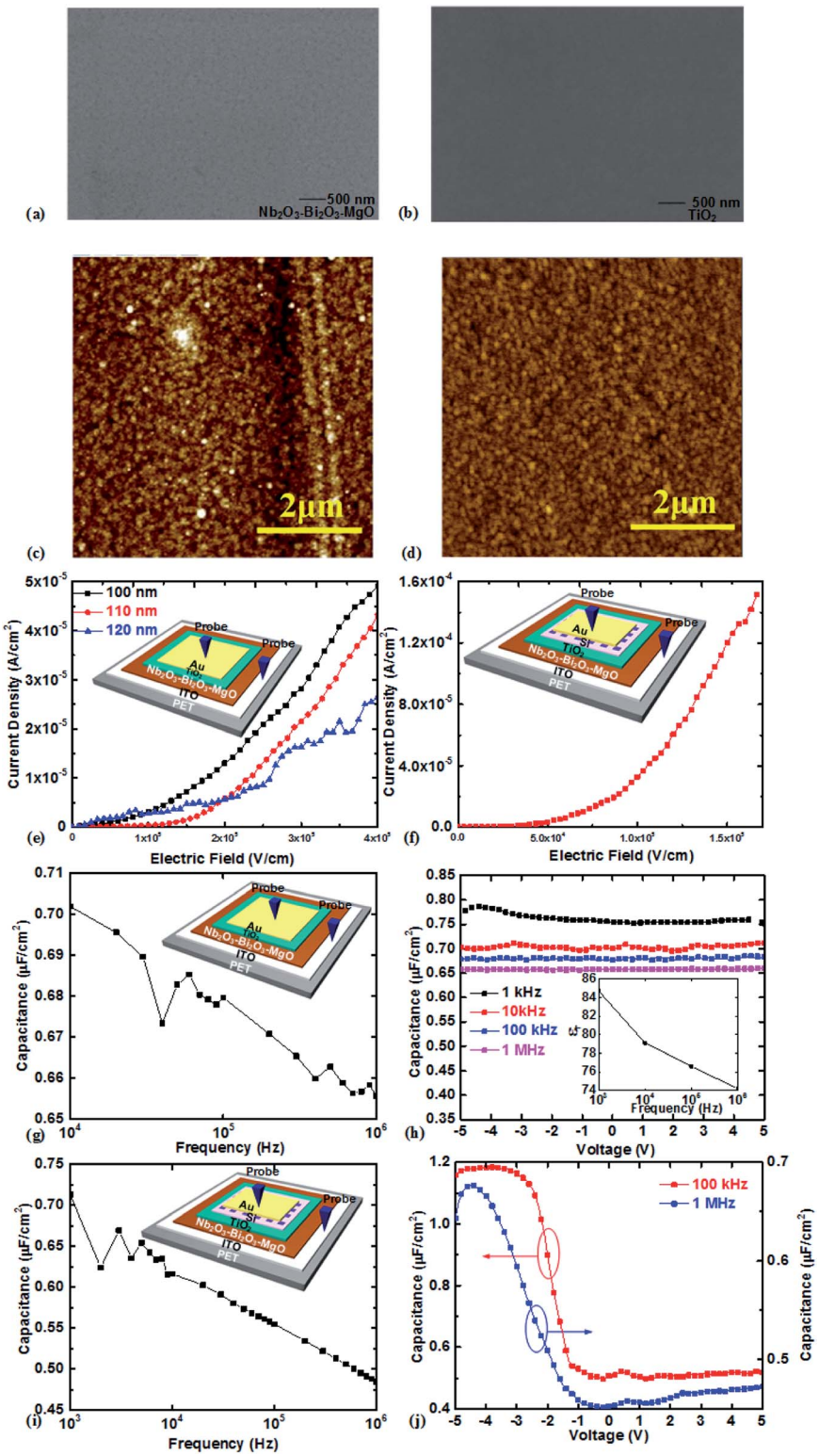

Fig. 2 Surface morphologies and characteristics of Nb_2O_3–Bi_2O_3–MgO/TiO_2 and Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructures: (a) SEM image of surface morphology of Nb_2O_3–Bi_2O_3–MgO. (b) SEM image of surface morphology of TiO_2. (c) AFM image of surface morphology of Nb_2O_3–Bi_2O_3–MgO. (d) AFM image of surface morphology of TiO_2. (e) Leakage current density of Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure with different thickness. (f) Leakage current density of Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure. (g) Frequency–capacitance characteristics of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure. (h) Capacitance–voltage characteristics of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure. (i) Frequency–capacitance characteristics of the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure. (j) Capacitance–voltage characteristics of the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure.

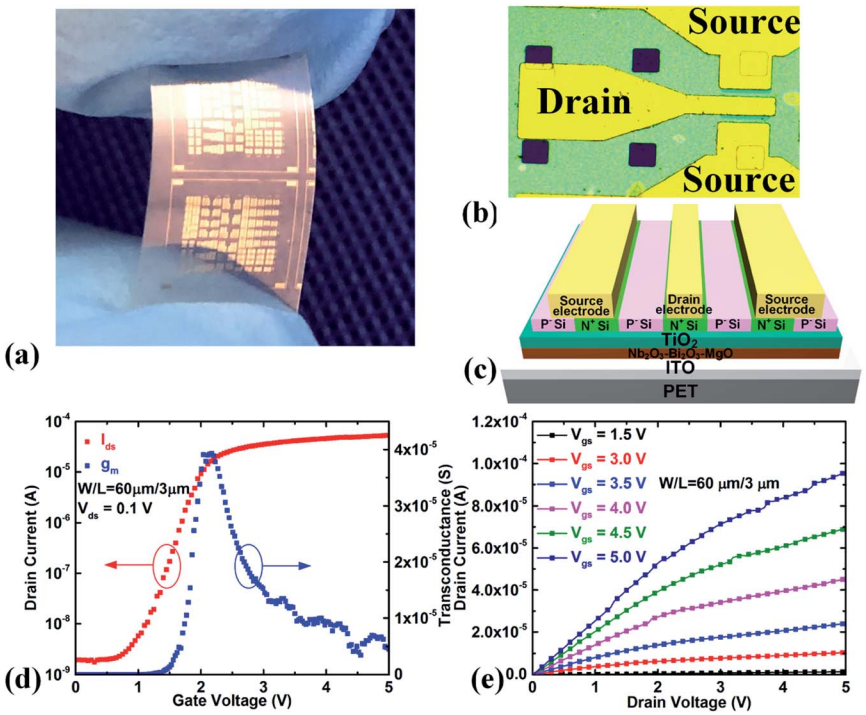

Fig. 3 The optical image, microscope image, structure schematic and dc characteristics of the fabricated flexible TFTs: (a) the optical image of the flexible TFTs on a plastic substrate. (b) The microscope image of an example flexible TFT with double channels. (c) Structure schematic of the flexible TFT (drawn not to scale). (d) The transfer characteristics of an example flexible TFT with $W/L = 60$ μm/3 μm. (e) The I–V characteristics of the flexible TFT with $W/L = 60$ μm/3 μm.

where k is the Boltzman constant and T is absolute temperature. q is unit electron charge and C_{ox} is the unit capacitance of Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure. The calculated D_{it} is $\sim 10^{12}$ eV^{-1} cm^{-2}, which is relatively low for flexible single-crystalline Si TFTs on plastic substrates.

Performance dependence of flexible TFTs on different dimensions are also investigated. Identical device structure is employed for the performance comparison.

Dependence on L

Fig. 4a and b show the transfer characteristics of flexible TFTs with different L (3 μm and 5 μm) and same W (60 μm) when V_{ds} is 0.1 V, respectively. The threshold voltage of flexible TFT with $W/L = 60$ μm/3 μm is ~1.2 V, which is slightly lower than that of TFT with $W/L = 60$ μm/5 μm (~1.3 V). This is because that when the depletion generated by applying gate voltage is partially overlapped with the source and drain depletion, the inversion layer charge in the Si and dielectric interface decreases, causing the threshold voltage to slightly decrease.

The drain current is observed to be inversely proportional to L. Quantitatively, the saturation drain current of flexible TFT of $L = 3$ μm (~53 μA) is ~1.6 times of that of flexible TFT of $L = 5$ μm (~33 μA), which is good agreement with theory calculation:

$$I_{ds} = \frac{W \times \mu_n \times C_{ox} \times \left[2\left(V_{gs} - V_{th}\right) \times V_{ds} - V_{ds}^2\right]}{2L}$$

$$0 < V_{ds} < V_{gs} - V_{th} \quad (5)$$

$$I_{ds} = \frac{W \times \mu_n \times C_{ox} \times \left(V_{gs} - V_{th}\right)^2}{2L} \quad 0 < V_{gs} - V_{th} < V_{ds} \quad (6)$$

The transconductance of flexible TFTs is extracted from the following equation:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \quad (7)$$

It is also consistent with the experiment results and the highest transconductance reaches to ~40 μS when the applied gate voltage is ~2.1 V.

Dependence on W

Fig. 4c and d show the transfer characteristics of flexible TFTs with different W (30 μm and 60 μm) and same L (3 μm) when V_{ds} is 0.1 V, respectively. The drain current is proportional to W.

The saturation drain current of flexible TFT of $W = 60$ μm (~53 μA) is 1.96 times of that of flexible TFT of $W = 30$ μm (~27 μA), which is also in good agreement with the theory calculation. The results show that the fabricated flexible TFTs with Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure have good performance consistency with different channel size.

Based on the experimental results, the advantages of the dielectric ceramics Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM

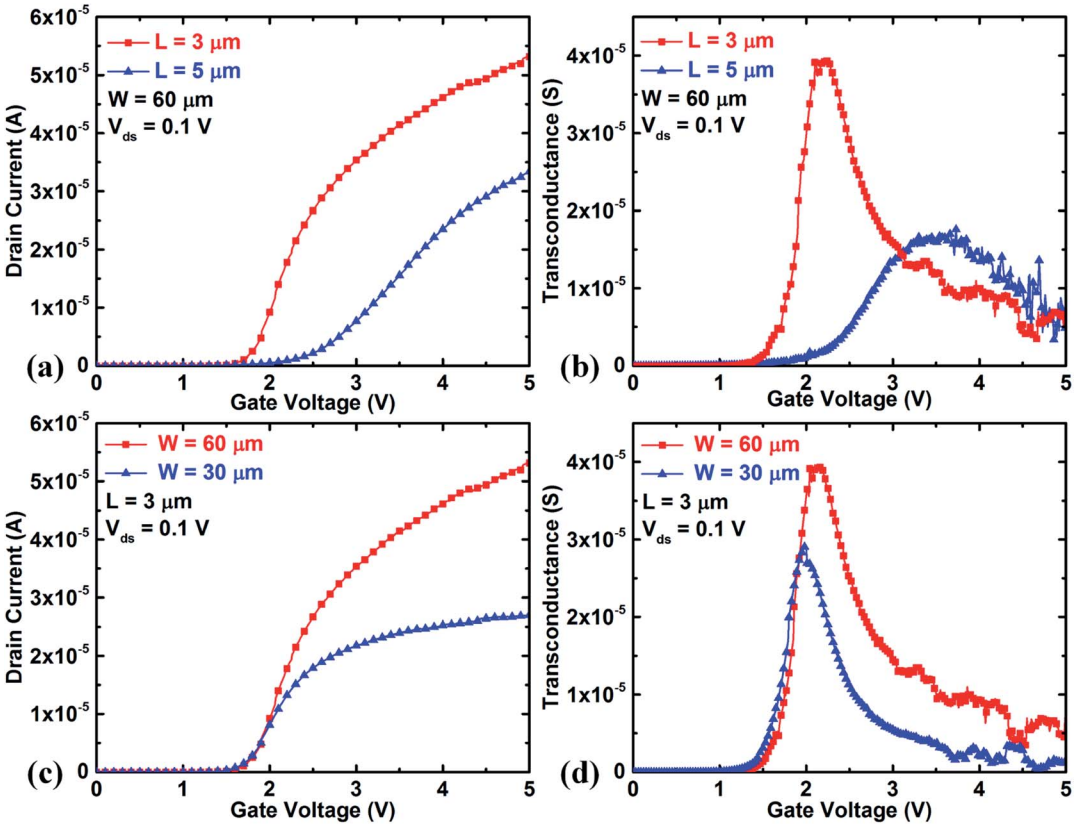

Fig. 4 The performance dependence of flexible TFTs on different dimensions: (a) I_{ds} and (b) transconductance comparisons of flexible TFTs with different L (3 μm and 5 μm). (c) I_{ds} and (d) transconductance comparisons of flexible TFTs with different W (30 μm and 60 μm).

heterostructure for flexible single-crystalline Si TFTs are analyzed and discussed as follows:

(1) The dielectric constant of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 dielectrics is extracted to be ~76.6 (Fig. 2). The number is lower than the dielectric constant of Nb_2O_3–Bi_2O_3–MgO and higher than that of TiO_2. Nevertheless, the dielectric constant of the heterostructure is much higher than those of SiO, SiO_x or most low-temperature processed dielectrics, thus demonstrating that the heterostructure can be used as high-k gate dielectric material for high performance flexible devices.

(2) The SEM images and AFM images show that the surface of TiO_2 is much smoother than that of Nb_2O_3–Bi_2O_3–MgO (Fig. 2) and the D_{it} of Si and dielectric (~10^{12} eV^{-1} cm^{-2}) is relatively low, which indicates that inserting TiO_2 between SiNM and Nb_2O_3–Bi_2O_3–MgO can improve the interface quality. Additionally, the leakage current of Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure is lower than that of TiO_2/SiNM heterostructure. The reason for this is that dielectric ceramics layer Nb_2O_3–Bi_2O_3–MgO increases the conduction band offset between SiNM and TiO_2, which can be explained from Fig. 5.

Fig. 5a shows the absorbance spectra of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure with wavelength from 365 nm to 1000 nm. Based on the absorbance (Abs), the optical absorption coefficient (α) for the heterostructure can be calculated as follows:[41]

$$\alpha = 2.303(\mathrm{Abs}/t_{ox}) \quad (8)$$

where t_{ox} is the thickness of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure (~100 nm).

The band gap of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure can be extracted by the following equation[42] as shown in the Fig. 5b:

$$\alpha h\nu = B(h\nu - E_g)^2 \quad (9)$$

where h is Planck's constant and ν is the light frequency, B is absorption constant and E_g is the band gap. The band gap of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure is extracted to be ~3.19 eV, which is higher than that of TiO_2,[43–45] proving that combing TiO_2 with high-k material Nb_2O_3–Bi_2O_3–MgO can improve the performance of TiO_2.

Mechanical bending tests have been conducted for the fabricated flexible TFTs. The drain currents of the flexible TFTs are measured by attaching the devices onto molds with various curvature radii (from ~77.5 mm to ~28.5 mm). The flexible single-crystalline Si TFTs with Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure on plastic substrates show slight performance variations, indicating good performance stability under mechanical bending conditions.

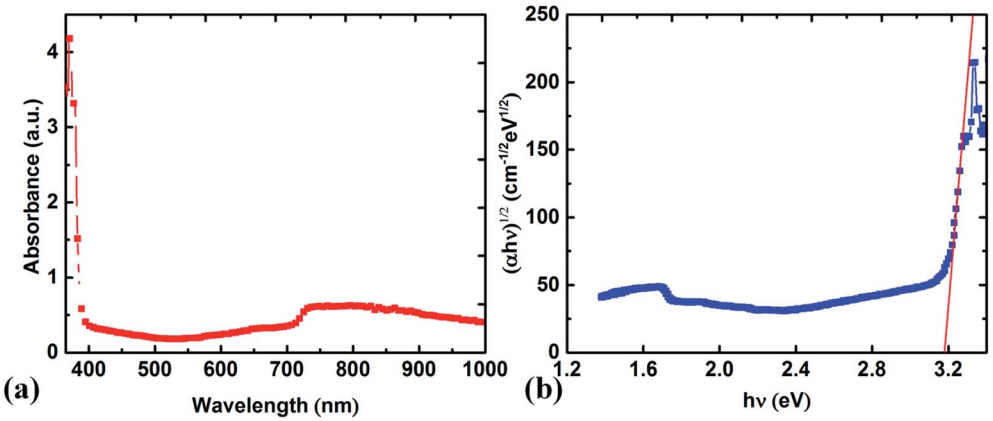

Fig. 5 The spectra and band gap of Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure: (a) the absorption spectra of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure with wavelength from 365 nm to 1000 nm. (b) The extracted band gap of the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure.

Conclusions

High performance flexible thin-film transistors (TFTs) with dielectric ceramics/TiO_2/single-crystalline silicon nanomembrane (SiNM) heterostructure is designed and fabricated in this paper. Both the dielectric ceramics (Nb_2O_3–Bi_2O_3–MgO) and TiO_2 are deposited by radio frequency (RF) magnetron sputtering at room temperature and the single-crystalline SiNM is transferred and attached to the dielectric ceramics/TiO_2 layers to form the heterostructure. The experimental results demonstrate that the Nb_2O_3–Bi_2O_3–MgO/TiO_2 heterostructure has high dielectric constant (~76.6) and wider band gap than TiO_2, which increases the conduction band offset between Si and TiO_2, lowering the leakage current. The TiO_2/single crystalline SiNM structure has relatively low interface trap density. Flexible TFTs fabricated with the Nb_2O_3–Bi_2O_3–MgO/TiO_2/SiNM heterostructure on plastic substrates show a current on/off ratio over 10^4, threshold voltage of ~1.2 V, subthreshold swing (SS) as low as ~0.2 V dec^{-1}, interface trap density of ~10^{12} eV^{-1} cm^{-2} and good performance stability under mechanical bending conditions. The results indicate that the dielectric ceramics/TiO_2/SiNM heterostructure has great potential for high performance TFTs.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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